Characterization of HYPRES' 4.5 $\mathrm{kA/cm^2}$ & 8 $\mathrm{kA/cm^2}$ $\mathrm{Nb/AlO_x/Nb}$ Fabrication Processes

Daniel Yohannes, Saad Sarwana, Sergey K. Tolpygo, Anubhav Sahu, Yuri A. Polyakov, and Vasili K. Semenov

***Abstract*—HYPRES has developed new fabrication processes for higher critical current density Josephson junctions (JJ's). These processes incorporate an additional anodization step for junction insulation, which enables fabrication of junctions down to submicron sizes. A set of new processing tools has been employed, including a high density (ICP) plasma etching of niobium and aluminum, and low temperature plasma-enhanced chemical vapor deposition of interlayer dielectric ($\mathrm{SiO_2}$) from a TEOS source. A set of new parametric control monitor (PCM) test chips has been designed and implemented. Results of electric and SEM characterization of JJ's, wiring, and contact-hole etching are presented. The critical current spreads and shunt resistance uniformity along with the effects of junction shape are discussed. The critical current 1σ spreads of 1.2% have been achieved for the 4.5 $\mathrm{kA/cm^2}$ process.**

***Index Terms*—Anodization, critical current, dielectric, etching, Josephson junction (JJ), lithography.**

I. Introduction

INCREASING the operating speed of digital superconducting integrated circuits (IC) requires higher critical current density Josephson junctions with proportionally smaller junction sizes, scaling as $a \sim 1/j_c^{1/2}$. To address this need, HYPRES, Inc. has developed a new process for 4.5 $\mathrm{kA/cm^2}$ and 8.0 $\mathrm{kA/cm^2}$ current densities [1]. In HYPRES' conventional 1 $\mathrm{kA/cm^2}$ process, the minimum junction size is limited by the sum of the minimum size contact hole to the junction and the contact hole alignment tolerance. With the currently employed photolithography tool (Perkin-Elmer full 150-mm-wafer projection aligner), the minimum size has been restricted to about 2 μm. This restriction was alleviated by implementing an anodization step right after the junction counter electrode definition by reactive ion etching, similarly to previous works [2]–[5]. The purpose of this paper is to give details of the new process control and to present results of junction characterization and device testing.

Manuscript received October 5, 2004. This work was supported in part by ONR.

D. Yohannes is with the Department of Physics and Astronomy, Stony Brook University, Stony Brook, NY 11794 USA and also with HYPRES, Inc. Elmsford, NY 10523 USA (e-mail: Daniel@hypres.com).

S. Sarwana and S. K. Tolpygo are with the HYPRES Inc., Elmsford, NY 10523 USA (e-mail: sarwana@hypres.com; stolpygo@hypres.com).

A. Sahu was with the Department of Physics and Astronomy, Stony Brook University, Stony Brook, NY 11794 USA. He is now with the HYPRES Inc., Elmsford, NY 10523 USA.

Y. A. Polyakov and V. K. Semenov are with the Department of Physics and Astronomy, Stony Brook, NY 11794 USA.

Digital Object Identifier 10.1109/TASC.2005.849701

II. Process Monitoring and Characterization

HYPRES uses a projection lithography tool having resolution of 0.8 μm measured on lines and spaces. The process control during the photolithography includes a critical dimension (CD) measurement on 1 μm–4 μm bars, using a 150X objective optical system. The exposure dose is controlled by monitoring lines and spaces of size from 1 μm to 2 μm. The tool is equipped with an Automatic Fine Alignment (AFA) providing alignment tolerance $3\sigma \sim 0.25$ μm. Scanning electron microscopy was also used for controlling the photoresist profile and CD during the process development phase.

Etching of metals and dielectric is done in two reactive ion etch systems in fluorine-based chemistries and one inductively-coupled plasma (ICP) etch system equipped with both fluorine and chlorine-based chemistries ($\mathrm{Cl_2}$, $\mathrm{BCl_3}$). An emission optical spectrometer is used for etch end-point detection for all wiring layers, resistors as well as contact hole etching. Since the anodization layer around the junctions is only ~60 nm thick, precise end-point detection is needed to minimize damage and formation of shorts. To ensure complete opening of contact holes, an extra process control is done by using a profilometer for step height measurement on test structures spread throughout the wafer. The typical etch uniformity is $\pm 2\%$ across 150-mm wafers. The same CD bars that were used for the lithography control are re-measured to determine metal over-etch.

HYPRES has implemented a Plasma Enhanced Chemical Vapor Deposition (PECVD) system to deposit $\mathrm{SiO_2}$ dielectric at low temperatures (100–150°C), using a tetra-ethoxysilane (TEOS) source. Step coverage was examined during process development using SEM pictures on cross-sections of chips and was found to be superior to the previously used ion-beam-sputtered $\mathrm{SiO_2}$. A combination of chemical and plasma cleaning is used for surface preparation to avoid pin-hole formation.

Standard HYPRES technology had predominantly been using square Josephson junctions with a minimum junction size of 3 μm. At the end of junction definition, i.e., after lithography and etching, these junctions retained a square shape with some corner rounding, resulting in the so-called missing area ds. With significant reduction in junction size in the new process, this diffraction-induced rounding became dominating, and the junction shape had to be optimized in order to minimize the missing area. Three types of junctions had been designed and tested for minimum bias—square, Manhattan-shaped and circular junctions, each having its own advantages and disadvantages. For instance, square shapes are easy to design and implement even on larger grid (> 0.25 μm) photo-masks. The circular shape

on the other hand can only be implemented with smaller grid (0.1 μm), and thus more expensive, photo-masks. The advantage is that after the processing they remain circular with some missing radius $\boldsymbol{dr}$. The Manhattan shape was designed to emulate circular shape in the 0.25 μm grid masks.

In general one can relate the critical current, $\boldsymbol{I_c}$ of a junction with design area $\boldsymbol{S}$, missing area $\boldsymbol{ds}$ and/or missing radius $\boldsymbol{dr}$ to the current density $\boldsymbol{J_c}$ by:

$$I_c = J_c \times \pi \left(\sqrt{\frac{S - ds}{\pi}} - dr \right)^2$$

In particular, for circular junctions $\boldsymbol{ds} = 0$ and the above equation reduces to:

$$I_c = J_c \times \pi (r - dr)^2$$

where $\boldsymbol{r}$ is the design radius. For square junctions bigger than 2 μm, $\boldsymbol{dr} = 0$ resulting in the conventional fitting equation:

$$I_c = J_c \times (S - ds)$$

For Manhattan-shaped as well as square junctions smaller than 2 μm, both $\boldsymbol{ds}$ and $\boldsymbol{dr}$ need to be included for fitting.

HYPRES' standard process uses Molybdenum as a resistive layer. For the new process, the sheet resistance was just scaled from 1 $\Omega/\square$ to 2.1 $\Omega/\square$ for 4.5 $\mathrm{kA/cm^2}$ process and 2.8 $\Omega/\square$ for 8 $\mathrm{kA/cm^2}$, according to $1/\mathrm{j_c^{1/2}}$ scaling in order to preserve the same junction damping factor (β_c) [6]. This required thinning of the resistor layer while still maintaining uniformity across 150-mm wafers.

III. Parametric Control Monitor (PCM) Test Chips

Diagnostic test chips have been designed in such a way that both the fabrication and the design parameters can be controlled. These include: a) arrays of shunted junctions of different sizes to determine critical current density ($\boldsymbol{J_c}$) and size bias ($\boldsymbol{dr}$ or $\boldsymbol{ds}$); b) arrays of un-shunted junctions to check trilayer quality, gap ($\boldsymbol{V_g}$), normal resistance ($\boldsymbol{R_N}$), sub-gap resistance ($\boldsymbol{R_{sg}}$), $\boldsymbol{I_cR_N}$ and $\boldsymbol{V_m}$. $\boldsymbol{J_c}$ and size bias can also be determined from the same set of arrays, though the data are less reliable since the switching current of small junctions is affected by equipment and thermal noise. Four-point probe structures of different width and length and Van der Pauw test structures [7] are used to control sheet resistance uniformity as well as the size bias (over-etch) of resistors and all superconducting layers. A set of symmetric interferometers is used to determine the inductance of superconducting layers and specific capacitance of junctions; comb structures to check the minimum line spacing; meanders and lines etched in different metal layers to check the dielectric integrity and critical current of lines in superconducting layers. Fig. 1 shows one of such diagnostic test chips.

IV. Test Results

SEM pictures of Josephson junctions were used to measure the spread in size and check the shape of the junctions after lithography and etching. Fig. 2 shows one of such comparisons for square and circular junctions of size 1.5 μm and less. As has been mentioned earlier, square junction of size 1.5 μm and 1.0 μm came out as circular with missing area of 0.6 $\mu\mathrm{m}^2$ on average, whereas circular-shaped junctions still remained circular with a missing radius of ~ 0.1 μm.

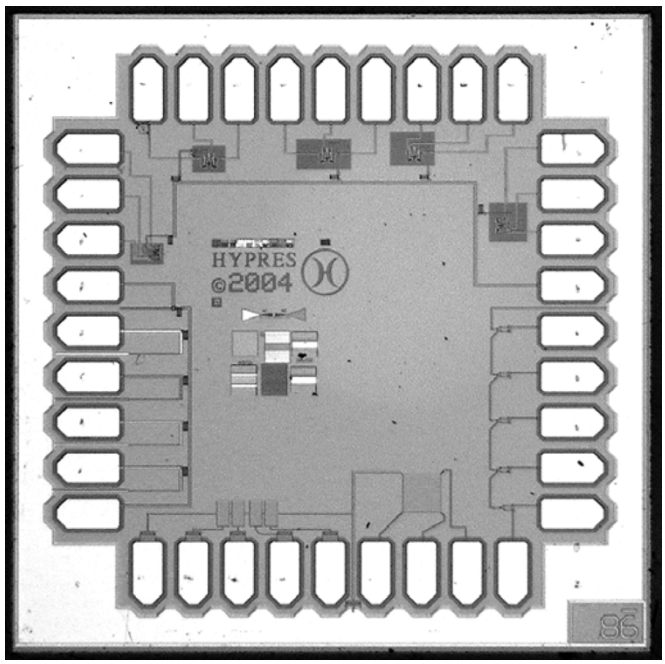

Fig. 1. The typical process monitoring chip for inductances, junction specific capacitance, sheet resistance and resistors over-etch.

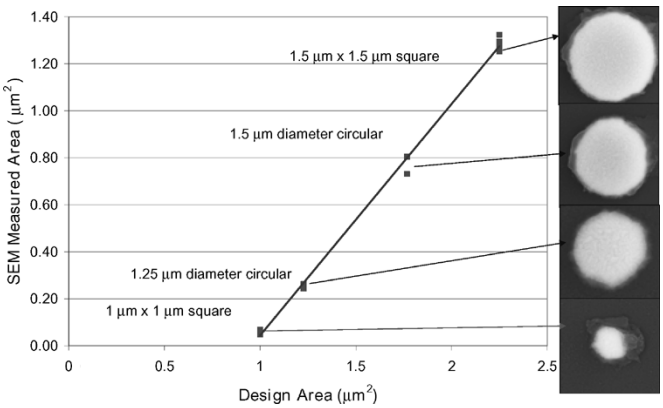

Fig. 2. SEM-measured area vs. design area for square and circular junctions of designed size of 1.5 μm and less, features patterned on 2000 Å of Nb.

All electrical measurements were done entirely by an automated measurement system OCTOPUX in a shielded room. One of the main parameters for making large superconducting integrated circuits (IC's) is the spread of JJs' critical current. Our goal was to achieve 1σ spread of less than 3%. This was done both by choosing the right anodization method and by optimizing anodization and etching parameters [1]. Fig. 3 shows the typical IV measurements of arrays of 100 circular unshunted Josephson junctions with on chip diameter ranging from 1.5 μm to 3.5 μm.

The $\boldsymbol{I_c}$ parameter spread on a 5 × 5 mm chip is best visualized by normalizing the IV curves with their normal resistance $\mathrm{R_N}$. Then, the junctions of different sizes can be easily compared, as shown in Fig. 4. This gives the total 1σ spread across a 5 mm

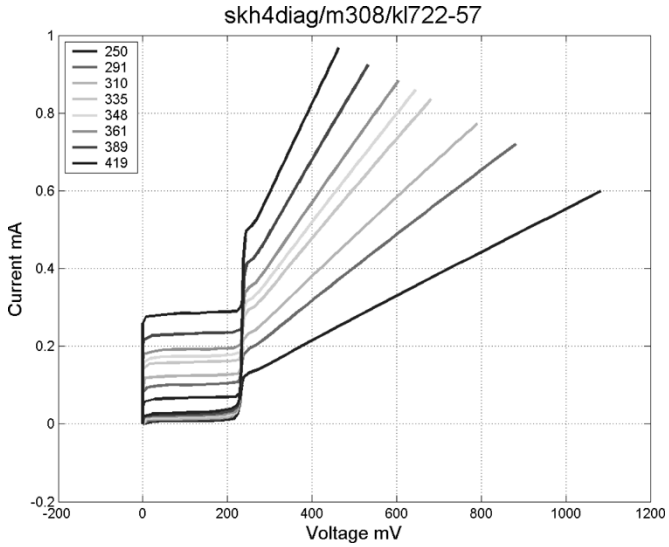

Fig. 3. The typical IV curves of 100-junction arrays of circular junctions. The on-chip diameter of the junctions is from 3.5 to 1.5 μm from top to bottom.

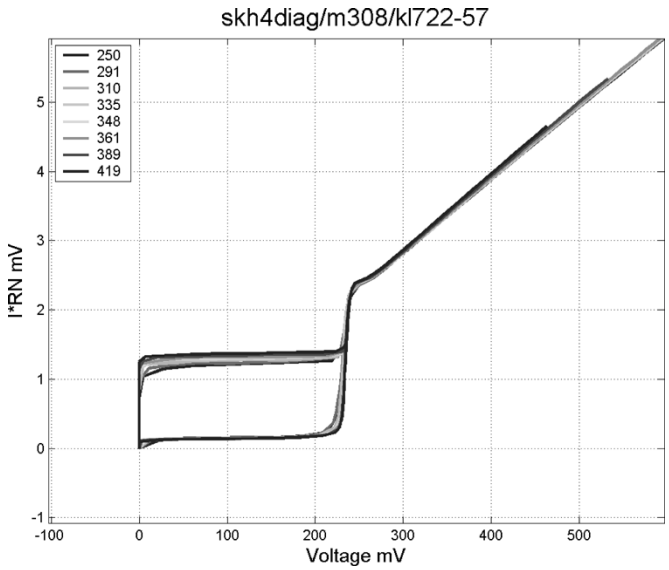

Fig. 4. Normalized IV curves for the same arrays as in Fig. 3. The critical current spread across the chip is about 2.4% as compared to the spread in individual arrays of less than 1.2%.

chip of 2.4%, whereas the spread inside individual arrays is less than 1.2%. However, the above given spreads of critical currents include both the thermal noise and the "fabrication" noise. Subtracting the thermal noise from the measured spreads of critical currents would result in yet lower fabrication spreads [8].

To insure uniformity of the resistive layer sheet resistance across 150-mm wafer, the whole 300 × 300 mm pallet was scanned for deposition uniformity. For the standard 1 $\mathrm{kA/cm^2}$ process, the average sheet resistance was $1.92 \pm 0.08\ \Omega/\square$ at room temperature, and the average layer thickness was 755 ± 22 Å as shown in Fig. 5. This gives very uniform sheet resistance of $1.0 \pm 0.1\ \Omega/\square$ at 4.2 K no matter where the wafer is placed on the pallet, enabling even two 150-mm wafers to be processed at the same time.

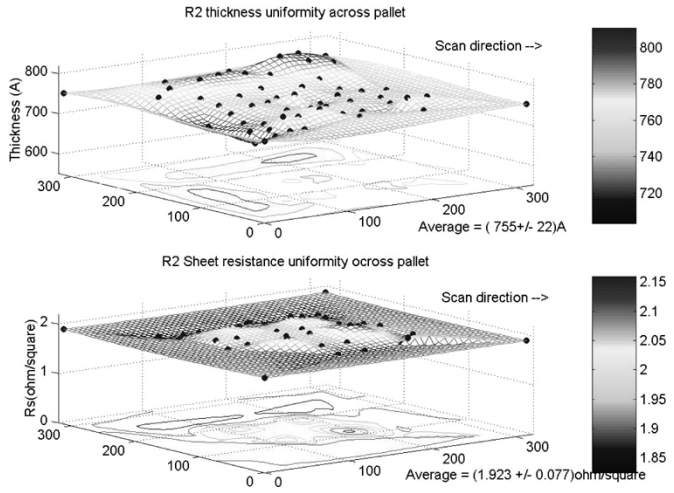

Fig. 5. The sheet resistance and resistor layer thickness uniformity across 300 × 300 mm pallet. The sheet resistance was measured using a 4-point resistance probe while thickness was measured using a stylus profilometer.

TABLE I
TYPICAL PARAMETERS OF HYPRES' NEW PROCESS

Circuit element	Parameter	Value
Junction	J_c	4.5 ± 0.5 kA/cm^2
	dr	0.37 ± 0.05 µm
	V_g	2.5 ± 0.1 mV
	IcR_N	1.3 ± 0.2 mV
	V_m	13 ± 2 mV
	R_{sg}/R_N	10 ± 1
Resistors	R_s	$2.1 \pm 0.2\ \Omega/\square$
	One side bias (over-etch)	0.15 ± 0.05 µm
Critical current of 3-µm wires of different superconducting layers	M0 (1000 Å)	80 ± 10 mA
	M1 (1500 Å)	90 ± 10 mA
	M2 (3000 Å)	120 ± 10 mA
	M3 (6000 Å)	> 200 mA
Critical current of 3µm x 3µm contact holes	I0	60 ± 10 mA *
	I1B	50 ± 20 mA
	I2	70 ± 20 mA

*With M1 crossing M0 edge 20 ± 10 mA.

For the new 4.5 $\mathrm{kA/cm^2}$ process, the sheet resistance at room temperature has to be around 3.85 $\Omega/\square$, and the average layer thickness around 330 Å. Now, in order to get the same level of uniformity resistors, the wafers need to be placed in the most uniform part of the deposition region (which happens to be the center of the pallet) and thus be processed one at a time.

Table I above summarizes the typical parameters of Josephson junctions in the new 4.5 $\mathrm{kA/cm^2}$ process. For circular junctions an average missing radius was found to be 0.37 μm. The current carrying capacity of 3-μm wires in the four superconducting layers is also given in Table I. The critical current of 3 μm × 3 μm contact holes is also summarized. Here, I0 contact hole is between the superconducting ground plane (M0) and the junction base electrode (M1), I1B contact hole is between junction counter electrode (I1A) and wiring layer M2, and I2 contact hole is between M2 wiring layer and the second wiring layer (M3).

V. Conclusion

The new fabrication process with junction anodization has successfully been developed for 4.5 $\mathrm{kA/cm^2}$ and 8 $\mathrm{kA/cm^2}$ current density Josephson junctions. It is now being implemented for the fabrication of complex digital circuits with 12 000–15 000 Josephson junctions. Design Rules for the 4.5 $\mathrm{kA/cm^2}$ process can be found athttp://www.hypres.com/ under the foundry section.

Acknowledgment

The authors gratefully acknowledge A. Kirichenko for the diagnostic chip design, J. Quinn for his help in taking SEM pictures, T. Filippov and S. Kaplan for help in design and useful discussions; and would like to thank R. Hunt, J. Vivalda, R. Patt, and D. Donnelly for their contribution in process development and help with processing.

References

[1] S. K. Tolpygo, D. A. Donnelly, R. T. Hunt, A. Kirichenko, R. Patt, S. Sarwana, J. A. Vivalda, and D. Yohannes, "HYPRES' New Fabrication Process for High-Speed Superconducting Microelectronics and Quantum Computing," presented at this conference.

[2] X. Meng and T. Van Duzer, "Light-anodization process for high-Jc micron and submicron superconducting junction and integrated circuit fabrication," *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 91–94, Jun. 2003.

[3] G. L. Kerber, L. A. Abelson, K. Edwards, R. Hu, M. W. Johnson, M. L. Leung, and J. Luine, "Fabrication of high current density Nb integrated circuits using a self-aligned junction anodization process," *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 82–86, Jun. 2003.

[4] D. Nakada, K. K. Berggren, E. Macedo, V. Liberman, and T. P. Orlando, "Improved critical-current-density uniformity by using anodization," *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 111–114, Jun. 2003.

[5] S. Nagasawa, K. Hinode, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, "Development of advanced Nb process for SFQ circuits," *Phys. C*, pt. 2, vol. 412, pp. 1429–1436, Oct. 2004.

[6] D. K. Brock, A. M. Kadin, A. F. Kirichenko, O. A. Mukhanov, S. Sarwana, J. A. Vivalda, W. Chen, and J. E. Lukens, "Retargeting RSFQ cells to a submicron fabrication process," *IEEE Trans. Appl. Supercond.*, vol. 11, pp. 369–372, Mar. 2001.

[7] L. J. Van der Pauw, "A method of measuring specific resistivity and Hall effect of discs and arbitrary shapes," Philips Res. Repts 13, 1958.

[8] V. K. Semenov, Y. A. Polyakov, and W. Chao, "Extraction of impacts of fabrication spread and thermal noise on operation of superconducting digital circuits," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 4030–4033, Jun. 1999.