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Process-Induced Variability of $\mathrm{Nb/Al/AlO_x/Nb}$ Junctions in Superconductor Integrated Circuits and Protection Against It

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***Abstract*—It is shown that the critical current density, j_c of $\mathrm{Nb/AlO_x/Nb}$ Josephson junctions in multilayered structures such as superconductor integrated circuits depends on the junction environment and on which wiring layers make contacts to the junction electrodes, and at which stage of the fabrication process. In particular, it is shown that contact holes between the junction base electrode layer and Nb ground plane layer in proximity to the junctions increase their j_c and degrade the junction quality. This effect alone may induce enough variation in the properties of Josephson junctions in superconductor integrated circuits to significantly reduce margin of operation and yield of complex circuits. Numerous test structures have been designed, fabricated at various technological regimes, and exhaustively tested in order to investigate various phenomena leading to damage of tunnel barrier or local variation of j_c in $\mathrm{Nb/Al/AlO_x/Nb}$ junctions. The results indicate that layer-dependent and local environment effects on j_c are mainly due to electromigration and interlayer diffusion of impurity (hydrogen) atoms around contacts between different layers and changes in hydrogen concentration brought about by wafer processing. Based on the gained insight into the materials science of the phenomenon, methods for minimization and prevention of process-induced changes to $\mathrm{Nb/Al/AlO_x/Nb}$ tunnel junctions have been developed.**

***Index Terms*—Hydrogen, Josephson device fabrication, Nb/AlOx/Nb tunnel junctions, superconducting integrated circuits.**

I. Introduction

SUPERCONDUCTOR integrated circuits (SICs) based on Rapid Single Flux Quantum (RSFQ) logic have a potential for sub-THz clock frequencies at ultra-low power dissipation. Relatively complex digital circuits with more than 10^4 Josephson junctions (JJs) operating at clock frequencies $\sim$30 GHz have already been demonstrated. Margins of operation and the maximum clock frequency of RSFQ circuits strongly depend on a process-induced deviation of circuit parameters, mainly critical currents of Josephson junctions (JJs) in logic cells, from the design values. Increasing SICs complexity to a VLSI level requires thorough and methodical minimization of the fabrication process-induced variability of the critical current (I_c) of JJs and, hence, necessitates understanding of mechanisms of this variability.

The most advanced fabrication technologies for SICs utilize resistively shunted Nb/Al/AlOx/Nb Josephson junctions interconnected by four or more layers or niobium, SiO_2 interlayer dielectric, molybdenum shunt and bias resistors, and Ti/Pd/Au multilayer metallization of contact pads for circuit biasing and I/O leads [1]–[3]. We have recently found that the critical currents of Josephson junctions in such multilayered structures depend on the type of wiring layers making contacts with the junctions [4]. For instance, it was found that junctions with the base electrode (BE) layer M1 directly connected to Nb ground plane layer M0 have higher I_c (and higher critical current density, j_c) than nominally identical junctions which have no contacts to the layer M0 [4]. It was also found that the I_c of nominally identical junctions interconnected by layer M2 may depend on the size and shape of wiring connected to the junction, and the critical currents of junctions connected to the ground plane depend on the area and shape of the ground plane [5]. In other words, j_c of a Nb/Al/AlOx/Nb junction depends on the junctions' environment, and nominally identical junctions placed into different surroundings may end up having different critical currents. We suggested that these environmental effects on I_c result from plasma processing steps of wafer fabrication due to plasma-induced currents causing tunnel barrier degradation. Recently, dc breakdown currents in Nb/Al/AlOx/Nb junctions with $j_c = 1.0$ and 4.5 $\mathrm{kA/cm^2}$, as well as tunnel barrier breakdown effect on junction quality, have been measured directly [6]–[8]. The results show, however, that reaching breakdown conditions simultaneously in many junctions on the wafer during plasma-processing is highly unlikely due to insufficient current supplied by processing plasmas used in the HYPRES process. The same conclusion was also reached in [4], [5] based on the estimates of the required breakdown currents.

On the other hand, it is well known that bulk Nb and Nb thin films can dissolve large amount of different process gases such as argon, oxygen, nitrogen and, especially, hydrogen. Hydrogen is highly mobile in Nb, having the activation energy of $\sim$0.11 eV, the lowest among other impurities and a factor of 10 less than

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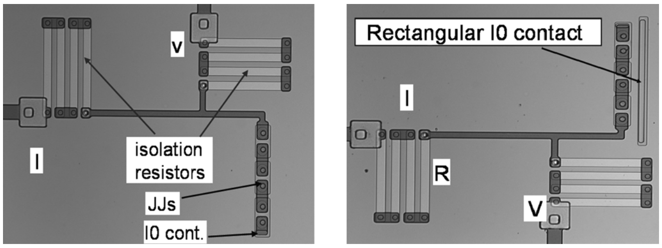

Fig. 1. Series array of Josephson junctions. The base electrode in the last JJ is connected to the ground plane through a contact hole in interlayer dielectric I0 (left panel). The same array in proximity to a large rectangular contact to the ground (right panel).

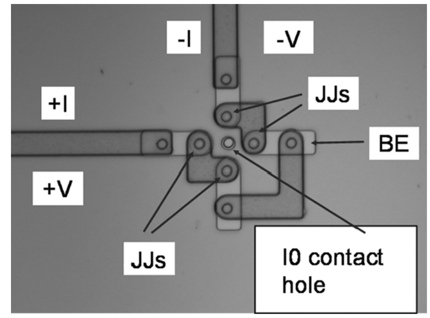

Fig. 2. Microphotograph of a 4-JJ array with junctions symmetrically located around the I0 contact hole of 1.6 $\mu\mathrm{m}$ in diameter. The JJs are circular, with the designed diameter of 1.98 $\mu\mathrm{m}$.

for oxygen migration in Nb [9]. It is also known that hydrogen content in Nb can be easily changed by processing steps such as chemical etching, polishing, reactive ion etching, ion milling, etc. [10], [11]. Physical properties of Nb such as lattice parameters, electric resistivity, T_{c}, etc. depend on the impurity (e.g., hydrogen) content. Therefore, it is possible that the layer-dependent and pattern-dependent effects on I_{c} of Nb-based junctions found in [4], [5] may result from changes in hydrogen content in the junction layers brought about by hydrogen diffusion or electromigration between different layers of the circuit and changes in hydrogen (or other impurities) content in Nb layers brought about by wafer fabrication (e.g., plasma processing). Recently, layer-dependent effects on I_{c} similar to those reported in [4], [5] have been observed for the SIC fabrication process used at ISTEC SRL, Japan [12] and explained as due to incorporation of hydrogen in Nb layers.

In order to study the mechanisms of Josephson critical current variability in Nb-based circuits and elucidate all pattern-dependent effects on I_{c} of Josephson junctions, we have designed, fabricated, and exhaustively tested numerous test chips containing $\mathrm{Nb/Al/AlO_x/Nb}$ junctions of different sizes, with various connections, environments, and surroundings. Our goal is to develop methods, both on the circuit fabrication and on the circuit design sides, enabling minimization or prevention of process-induced changes in the critical current and junction quality.

II. Test Chip Design and Fabrication Details

Test chips were placed in different locations on regular 150-mm process wafers, which were fabricated using 11-level HYPRES process [1], [2] with both 1.0 and 4.5 $\mathrm{kA/cm^2}$ Josephson critical current density. Series arrays of a few nominally identical junctions were used as a test vehicle to get an average I_{c} at each location by measuring the current-voltage $(I - V)$ characteristics. In these arrays, one junction (or a group of junctions) was intentionally placed in an environment different from the rest of the junctions in the array, so any abnormal behavior and deviations from the average can be revealed, as shown in Fig. 1.

A. Junctions With Grounded Base Electrode

The simplest test for the layer-dependent effects on j_{c} is the one used in [4], [5]. It presents an array of N junctions in which the first $N - 1$ JJs are interconnected by layers M1 (junctions' base electrode) and M2 (the first wiring layer) whereas the last JJ has the base electrode connected to the ground plane layer M0 through a contact hole in interlayer dielectric I0 (between layers M0 and M1). Such a JJ was called M1-grounded (M1-GND). A 5-JJ version of such an array is shown in Fig. 1 (left panel). The voltage and current leads to the first JJ in the array both have 50-Ω molybdenum resistors inserted in the leads close to the junction, which isolate the array from the chip contact pads. The current returns to the chip ground plane M0 and voltage is also measured with respect to the ground.

B. Proximity Effect of I0 Contact Holes on Junctions

Any M1-grounded junction described in Section II-A has two features which distinguish it from the rest of JJs in the array—the presence of a contact hole in I0 dielectric near the junction and that its BE contacts the ground plane through this hole. In order to investigate the effect of the contact hole alone, another set of series arrays was included. For 4-probe measurements, current and voltage leads to the arrays are connected on both ends to the chip contact pads by M2 wiring through 50-Ω molybdenum resistors. Four junctions in the arrays are arranged symmetrically around the contact hole between the ground plane and M1 layer (Fig. 2). The distance between the junctions and the contact hole was varied in different arrays from 2 to 50 $\mu\mathrm{m}$. A version of this test structure is an array of junctions having a rectangular contact hole in I0 running parallel to the entire array (see Fig. 1, right panel). The distance between the array and the contact is varied in the same fashion.

C. Contact Hole to a Ground Plane Island and Effect of Ground Plane Moats

In order to investigate the nature of I0 contact proximity affecting JJs, we have designed test arrays surrounded by a moat in M0 layer, forming an electrically isolated island in ground plane. The island was connected to the mainland ground plane via M2 wiring layer. In one case a long I0 contact hole was placed on the island in close proximity to the array, as shown in the left panel of Fig. 3. In the other case the contact hole was placed on the main ground plane just outside the island (Fig. 3, right panel). The main difference between the first and second cases is that, after the deposition, the trilayer makes contact with a small island of M0 in the first case while it contacts a much larger area $(\sim 0.25\ \mathrm{cm}^2)$ of the mainland M0 in the second. In order to study the possible dependence of the proximity effect

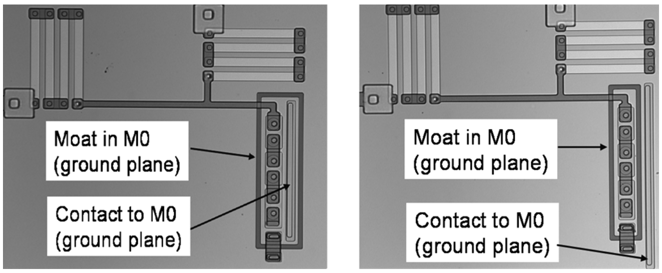

Fig. 3. Microphotographs of test arrays with JJs located parallel to a rectangular contact to the circuit ground plane, layer M0. The whole structure is surrounded by a moat in M0 forming an isolated island (left panel). This island becomes connected to the rest of the ground plane by M2 wire which can be seen at the very bottom of the picture as a rectangle crossing the moat in M0. On the right, the moat cuts only around the test array.

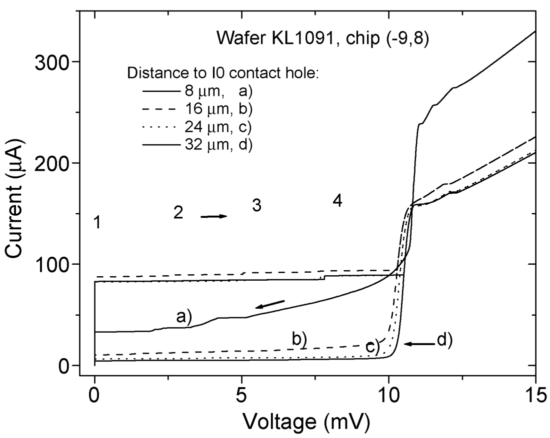

Fig. 4. $I-V$ characteristics of 4-JJ arrays shown in Fig. 2 at different distances from the I0 contact hole to the junctions. At short distances [e.g., curves *a*) and *b*)] I_c and subgap conductance are strongly enhanced and a large excess current can be seen, all manifesting defects in the barrier (regions with increased transparency). For a detailed analysis, see [5]–[8].

on the area of the object to which the contact is made, the area of M0 islands in the first case was varied in a wide range.

III. Test Results

The $I-V$ characteristics for the arrays shown in the left panel of Fig. 1 demonstrate a significant deviation of I_c of the junction connected to the ground plane from the other junctions in the array. The results are very similar to the previously reported [5], [6] and will not be repeated again here.

The typical $I-V$ curves of the 4-junction arrays surrounding a contact hole in I0 (Fig. 2) for different distances between the junctions and I0 contact hole are presented in Fig. 4.

The I_c and the subgap conductance are strongly enhanced in the junctions located at shorter distances, indicating an increased transparency and nonuniformity of the tunnel barrier (barrier damage) induced by a proximity to the contact hole. The effect of the contact hole on I_c becomes negligible at distances larger than $\sim 25\ \mu\mathrm{m}$. The I_c enhancement (i.e. the barrier degradation) is symmetrical around the contact hole.

For the long rectangular hole in I0 running parallel to the JJ array (Fig. 1, right panel) the effect is very similar. All the JJs are uniformly damaged and their I_c is enhanced when the distance between the JJs and the contact hole is small. The size of this effect is demonstrated in Fig. 5. As the distance to the

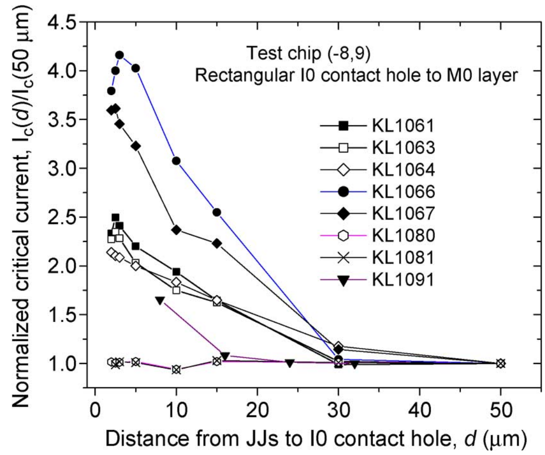

Fig. 5. Average I_c of JJs in a 5-junction array with a long I0 contact hole parallel to it as shown in Fig. 1 (right panel) vs. distance to the contact. The average I_c is normalized to the critical current in the array with the largest distance, $d = 50\ \mu\mathrm{m}$. The data are shown for seven sequential fabrication runs, indicated by trilayer labels KL1061 through KL1081, for the same test chip location. The data for wafer KL1091 are for the circular I0 contact (Figs. 2 and 4). Wafers KL1066 and KL1067 were fabricated by 1.0-kA/cm^2 process, all other wafers—by 4.5-kA/cm^2 process. The trilayer deposition and the junction definition processes were changed for wafers KL1080 and KL1081 with respect to the previous wafers in order to minimize the effect of I0 contact holes.

hole increases, the I_c decreases towards the normal, expected from the process j_c value, and the junction quality improves. At distances larger than $\sim 30\ \mu\mathrm{m}$ the junctions become unaffected by the contact hole proximity. These results indicate that contact holes connecting the base electrode of Nb/Al/AlOx/Nb trilayer to the ground plane during trilayer deposition and all steps of JJ definition degrade the quality of the tunnel barrier around the contact holes and make j_c position-dependent.

In order to see if the described effect of I0 contacts on the local j_c is reproducible, these tests have been run on 7 consecutively fabricated wafers shown in Fig. 5. It was found that the magnitude of the effect is reproducible for the identically processed wafers and depends also on the trilayer critical current density, being larger in lower-j_c trilayers. The influence of I0 contact holes was also found to be nonuniform across the process wafers, being the smallest in the central area of the wafers and increasing towards the periphery of wafers. The overall distribution was found to be similar to that measured in our previous work for the so-called M2-grounded junctions and shown in Fig. 6(b) in [4]. The number of diagnostic chips used in this work was not sufficient however to build the exact distribution maps.

It was also found that the effect of I0 contact holes on the local critical current density is process-dependent and is sensitive to the processes of trilayer deposition and junction definition. For instance, process modifications introduced for fabrication runs KL1080 and KL1081 resulted in complete elimination of the influence of contact holes on I_c of the junctions even at the shortest distances between the junctions and the contacts (see Fig. 5).

IV. Discussion

One could assume that the observed effect of I0 contacts on j_c is caused by a local mechanical stress in trilayers, appearing

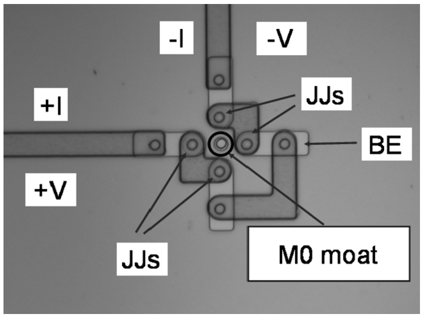

Fig. 6. The same structure as in Fig. 2, but the contact hole in the center is completely surrounded by a moat in M0. As a result, the contact is now made to a small island, electrically isolated from the rest of the circuit ground plane.

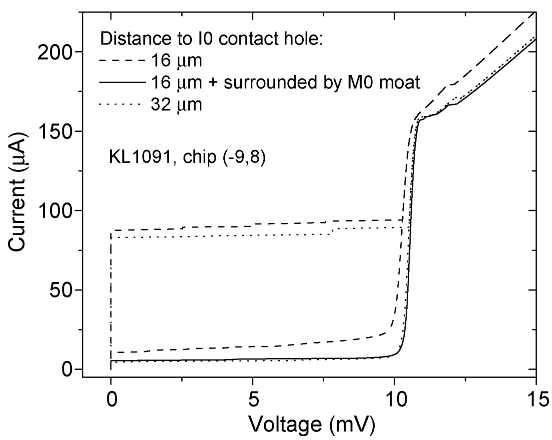

Fig. 7. $I - V$ characteristics of 4-JJ arrays with junctions in proximity to I0 contact hole (dash and dotted line) as shown in Fig. 2. Solid line is for the contact hole completely surrounded by M0 moat, as shown in Fig. 6.

around the contacts as a result of trilayer deposition on the dielectric layer with rich topography. To check this hypothesis, we surrounded the contact holes by a moat in M0, as shown in Fig. 3 (left panel) and Fig. 6. This moat can only enhance the dielectric layer topology near the prospective JJs and increase the height variations upon which the trilayer is deposited, and hence increase the local stress. Therefore, a larger proximity effect on local j_c could be expected. However, the experimentally observed effect was completely opposite to this expectation. Instead, the proximity effect of the contact hole on I_c of JJs was completely eliminated by surrounding the contact by M0 moat and thus electrically insulating the contact area from the rest of the ground plane, see Fig. 7.

The uniformity of I_c and the quality of junctions in the array isolated from I0 hole by M0 moat are even slightly better and the gap voltage is slightly higher than in the array located far away from the un-isolated hole, where the proximity effect of I0 hole is completely diminished (curve KL1091 in Fig. 5).

Similarly, for the test structure shown in the left panel of Fig. 3 (I0 contact inside the island) the junctions in the array were not affected by proximity to I0 hole, whereas a noticeable degradation of the junctions' quality and I_c enhancement were observed in the case shown on the right panel of Fig. 3. The topography in both cases is nearly the same, and the main difference is in the area of the ground plane to which the contact is being made.

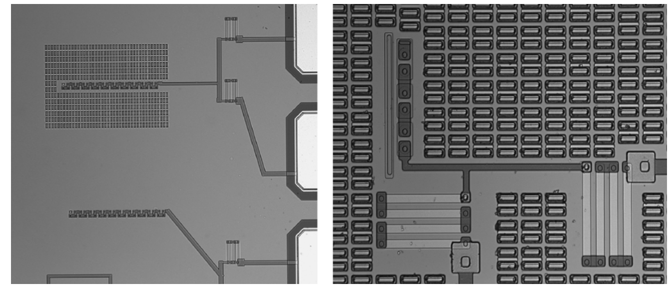

Fig. 8. Protective structures around the test arrays present a large number of small "universal shorts"—small islands of layers M1, M2, and M3 connected between each other and to the circuit ground plane.

Therefore, we conclude that the observed proximity effect is not caused by a simple mechanical stress in the trilayer, appearing during the deposition, but is rather electrical or electrochemical in nature. For instance, it is consistent with electromigration or diffusion of impurity atoms such as hydrogen (protons) between the ground plane layer and the junction layers during $\mathrm{Nb/Al/AlO_x/Nb}$ trilayer formation and/or junction definition steps of the process. In this case, local changes in Nb properties and lattice volume as well as potential reaction between hydrogen and oxide barrier may fully explain the whole spectrum of the observed phenomena and the previous results in [4], [5]. The presence of hydrogen in our Nb films and changes in its concentration caused by wafer processing have been confirmed by glow discharge emission spectroscopy, i.e. by observing hydrogen optical emission lines during reactive ion etching. These results will be presented elsewhere. The causes of hydrogen poisoning of Nb films could be water absorbed on the surface and solvent residue left after resist stripping and contact holes cleaning.

In order to separate interlayer diffusion from hydrogen electromigration caused by electric currents induced between the layers during plasma processing and ion milling, the following idea can be tested. If the phenomenon is electric in nature (such as electromigration) its effect should weaken with increasing the contact area. Paralleling current paths should reduce the local current density and the amount of impurity atoms transferred between the metal layers. On the other hand, creating additional contact areas should not stop the diffusion, and likely will enhance the effect. For this test, arrays with JJs in proximity to I0 contact holes were surrounded by a large number of redundant I0 contact holes as shown in Fig. 8 (left panel). In another test, the arrays were surrounded by small metal islands containing all Nb layers from M1 to M3 connected to each other and to the ground plane by contact holes (Fig. 8 right panel). The latter structure is more universal than the former because it should minimize the local current density around Josephson junctions during processing of any layer by increasing the total area of interlayer contact and by directing the total current into many channels between the metal layers.

The effect of such protective structures is demonstrated in Fig. 9 showing $I - V$ characteristics of the two arrays in the left panel of Fig. 8. The top array is surrounded by the dense array of I0 holes. The lower array has only one I0 contact hole that connects the base electrode of the last JJ to the ground. As can be

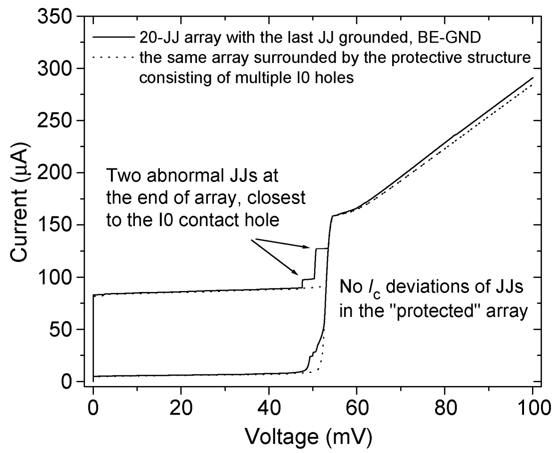

Fig. 9. The typical $I-V$ characteristics of 20-junction arrays (shown in Fig. 8) with the last JJ directly connected by BE to the ground plane through I0 contact hole near the last JJ. Two junctions show a significant deviation from the average—the grounded JJ and its nearest neighbor. They also show much higher return current (higher subgap conductance). These deviations do not exist in the array surrounded by a protective structure consisting of multiple I0 holes.

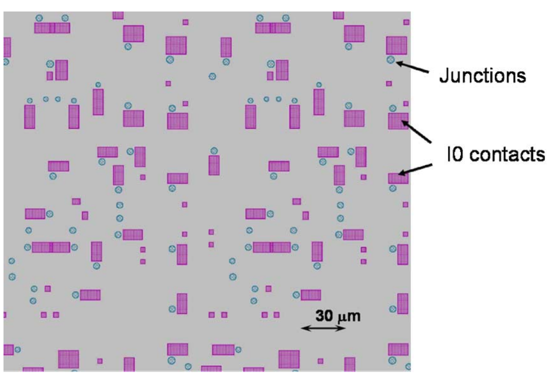

Fig. 10. A part of the typical RSFQ circuits showing only two layers—Josephson junctions (circles) and contacts in interlayer dielectric I0 between the ground plane layer M0 and base electrode layer M1.

seen, this simple protective structure around the test array completely eliminated the effect of proximity to the ground contact observed in [4], [5]. So, be it as paradoxical as it may, it turns out that, in order to prevent trilayer degradation around the contact to the ground plane, one needs to put more of such contacts.

The discovered proximity effect of contact holes on the I_c of junctions in multilayered structures is very important for integrated circuits. For instance, Fig. 10 presents a small part of a digital circuit showing only I0 contacts (dark rectangular shapes) and JJs (lighter circular shapes). It can be seen that the distances between I0 contacts and junctions are more or less random and any junction experiences the proximity effect of multiple contact holes. Therefore, the critical current of these junctions might significantly deviate from the expected (designed) value due to the local distortions of the current density and barrier quality created by a "random potential" of contact holes.

There are two possibilities. If the local distortions are long-range, the effects of different contacts overlap. In this case, the overall j_c in the circuit will be increased but the local variations can be relatively small. Such a circuit may have a chance to work after reducing the average j_c by, e.g., annealing the fabricated chip at elevated temperatures. However, if the local fields around the contacts are short-range, large quasi-random deviations of the critical currents from the design values can occur and render the circuit un-operational.

V. Conclusion

We have found a strong proximity effect of contact holes between the base electrode layer of Nb/Al/AlOx/Nb trilayers and the ground plane layer on the tunnel barrier quality and the local critical current density. The observed effects are consistent with migration of hydrogen between junction electrodes and the ground plane and wiring layers of superconductor integrated circuits and changes in hydrogen concentration caused by wafer processing. We developed a number of protective structures for use in superconductor integrated circuits, which minimize or completely eliminate process-induced variability of Nb-based Josephson junctions.

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