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Plasma process-induced damage to Josephson tunnel junctions in superconducting integrated circuits

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Abstract
It has been found that the critical current of Josephson junctions in superconducting integrated circuits may depend on the environment surrounding the junctions and on how a particular junction is connected (wired) to other junctions and circuit elements. This may cause large, pattern-dependent deviations of the junctions' critical currents from design values and ultimately limit the yield and performance of superconducting digital integrated circuits. In particular, we have found a difference in the critical current of grounded and floating junctions, and a dependence of the critical current on the size of metal structures connected to the junction—the 'antenna' effect. Experimental data were obtained for Nb/AlO_x/Nb Josephson junctions fabricated on 150 mm wafers by an 11-layer process for superconducting integrated circuits. The results are explained by plasma process-induced damage to ultra-thin tunnel barriers. The most damaging plasma processing fabrication steps are discussed.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Superconducting digital integrated circuits (ICs) based on the rapid single flux quantum (RSFQ) logic provide unparalleled advantages in circuit speed and power consumption but require accurate mutual relationships between critical currents, I_c, of the Josephson junctions (JJs) comprising the logic cells. Any deviations of I_cs in the fabricated circuits from the design values reduce yield, performance and margins of circuit operation. The design I_c value is simply given by j_cA, where j_c is the Josephson critical current density and A is the design junction area. Common wisdom has been that the sources of I_c deviations are mainly (a) variations of the area of fabricated junctions coming from the lithographic and etch processes of junction definition and (b) fluctuations of j_c resulting from fluctuations of the tunnel barrier transparency. Large deviations of I_c from the design value are thought to be due to gross fabrication defects whereas systematic shifts are usually attributed to an error in j_c targeting (e.g. some deviations in the process of junction barrier formation).

A prevailing method of Josephson junction fabrication for superconducting ICs (SICs) is based on the whole-wafer Nb/Al/AlO_x/Nb trilayer process [1]. In this *in situ* process, a tunnel barrier (AlO_x) is formed by thermal oxidation of aluminum deposited over a Nb base electrode (BE). If all the deposition parameters and the oxidation temperature are fixed, the barrier transparency is believed to be uniquely determined by oxygen exposure, which is the product of oxygen pressure and oxidation time [2]. It has been shown recently that tunnel barrier formation is completed only after the counter electrode (CE) is deposited because this deposition finalizes the oxygen content in the barrier by affecting a weakly bound chemisorbed oxygen layer remaining on the oxide surface after the oxidation [3]. Therefore, the Josephson critical current density (j_c target) on the wafer is believed to be set when the trilayer deposition has been completed. However,

the formation of a useful Josephson junction requires many more fabrication steps in order to define the junction area and form electrical connections to the BE and CE. In SFQ digital integrated circuits, Josephson junctions also need to be shunted by resistors and interconnected with other junctions and circuit elements (inductors, bias resistors, etc). It is known that these processing steps can potentially degrade the quality of Josephson junctions, especially when the thin tunnel barrier around the perimeter of the junction is exposed to processing chemicals. This problem is usually solved by anodizing the Al/AlO_x layer around the junctions and Nb sidewalls of the junction CE in a process often referred to as light anodization [4]. This is essentially a very light modification of the original selective Nb anodization (SNAP) and selective Nb etch (SNEP) processes employed for Josephson junction fabrication many years ago [5, 1] but performed at a lower voltage.

In this paper we would like to show that there is another mechanism for potentially large, systematic deviations of the critical currents of Josephson junctions in SICs from the design values. We have found that the Josephson critical current may depend on the junction environment, circuit patterns and on how the junction is connected to other circuit elements and superconducting layers. For instance, we have found that the critical current of the junctions having their base electrode connected to the circuit ground plane may be significantly higher than the critical current of the same size junctions but with the BE floating over the ground plane. We have also found that the critical current of the junctions connected to large metal structures may increase with the structure area. This 'antenna' effect has statistical character and depends on the junction location on the process wafers. We will show that the above-described pattern-dependent enhancement in the critical current of specific junctions is caused by an increase in transparency of the tunnel barrier. We suggest that this happens as a result of particular plasma processing steps at which a voltage develops across some of the junctions that is sufficient to cause soft breakdown of the tunnel barrier.

In many respects the observed phenomena resemble the phenomena of gate oxide damage by plasma-induced charging in semiconductor integrated circuit manufacturing (see, e.g., [6–8]). For instance, the SiO_2 gate oxide in metal–oxide–semiconductor field effect transistors (MOSFETs) can be significantly damaged (up to complete breakdown) as a result of global interactions between the wafer and processing plasmas. This damage is one of the main sources of the yield loss in semiconductor manufacturing, and there have been numerous publications and international conferences devoted to this subject. For a comprehensive review of the subject up to the year 2000 see [9]. The oxide barrier in Nb/Al/AlO_x/Nb Josephson junctions is of course much thinner than the typical SiO_2 gate oxide in MOSFETs, and the charge transport is dominated by direct tunneling contrary to the Fowler–Nordheim tunneling in gate oxides. However, the signatures of the oxide barrier damage are somewhat similar. In both cases there is an increase in the barrier transparency and electrical stress-induced leakage that can be viewed as a soft breakdown. It is interesting to note that the damage to ultra-thin gate oxides is usually very difficult to detect and characterize [9] whereas the Josephson critical current in structures with superconducting electrodes can serve as an extremely sensitive detector of the slightest changes in the barrier properties caused by wafer processing.

2. Fabrication process for superconducting integrated circuits

In this work we have used the standard fabrication process for superconducting integrated circuits developed at HYPRES, Inc. A detailed description of the process flow is given in [10, 11]. We will present only the sequence of the physical layers and other important details for understanding how the Josephson junctions are formed and interconnected. The fabrication is performed on thermally oxidized 150 mm Si wafers. The sequence of layers in the process from bottom (wafer surface) to top is the following:

(1) Nb superconducting ground plane; layer name M0.
(2) SiO_2 interlayer dielectric; layer I0.
(3) Nb base electrode; layer M1.
(4) Al/AlOx barrier.
(5) Nb counter electrode; layer I1A.
(6) Anodized layer of NbO_x/AlO_x (only on the surface of BE around the junctions); layer A1.
(7) SiO_2 interlayer dielectric; layer I1B-1.
(8) Mo resistor layer; layer R2.
(9) SiO_2 interlayer dielectric; layer I1B-2.
(10) First Nb wiring layer; layer M2.
(11) SiO_2 interlayer dielectric; layer I2.
(12) Second Nb wiring layer; layer M3.
(13) Contact pads metallization multilayer of Ti/Pd/Au; layer R3.

All metal layers, except R3, are deposited by dc magnetron sputtering; the R3 layer is e-beam evaporated. All layers of SiO_2 are deposited by plasma-enhanced chemical vapor deposition (PECVD) in a TEOS/O_2 plasma. All the layers are patterned by photolithography and reactive ion etching (RIE), except layer R3 for which a lift-off process is used. RIE of the metal layers is done in SF_6 plasma at 4 Pa and 40 W. RIE of SiO_2 layers is done in CHF_3/O_2 plasma at 13.3 Pa and 150 W. After etching the junction counter electrode layer, the exposed metal surface is anodically oxidized in ammonium pentaborate solution in ethylene glycol to form a protective anodic oxide layer that seals perimeters of the junctions (layer A1). The junction CE etch mask serves here as the anodization mask protecting the top surface of the counter electrodes from anodizing. The anodized layer is then removed everywhere but the 1 μm-wide disk around the junctions by another photolithography step and argon ion milling.

Overall, after the trilayer deposition, there are 17 plasma processing steps. These include seven steps involving RIE of metal and interlayer dielectric (ILD) layers: JJ counter electrode (layer I1C), JJ base electrode (M1), resistor layer R2, wiring layers M2 and M3, and contact holes in ILDs (layers I1B and I2). There are also three steps of PECVD of SiO_2 ILD (I1B-1, I1B-2, and I2), four steps of RF-sputter cleaning in Ar plasma and three metal layer depositions (R2, M2, and M3). Each of these plasma processing steps can be potentially damaging to an ultra-thin AlO_x tunnel barrier if a sufficient voltage can develop across the junction or if a sufficient amount

of electric charge can pass through the junction to cause an irreversible change in the barrier properties (soft breakdown). Since the barrier is only ∼1 nm thick, the breakdown voltage is less than 1 V [12]. Although the total charge to breakdown should be very large for the thin barrier due to the direct tunneling nature of charge transport, the amount of charge passing through the junction can be amplified by the junction wiring to other metal structures which may serve as charge collecting antennas. The potential difference that can develop across the junction during the plasma exposure may depend on the uniformity of the plasma potential and pattern-dependent charging caused by electron shading and other effects of wafer–plasma interactions [6–9, 13, 14]. In some cases processing plasmas can cause damage even to Nb superconducting films, as was observed in [15].

3. Experiment and results

3.1. Design of test structures

In superconducting integrated circuits, Josephson junctions can be connected in many ways to each other and to other circuit elements in order to create a digital circuit. Except in a very limited number of simple circuits, there is no experimental way of determining the critical currents of individual junctions after the circuit has been made. The success of the fabrication can only be judged by the circuit performance. If a circuit does not work there is usually no way to determine the reasons for failure. Therefore, in this work we used a set of diagnostic test structures that mimic all possible connections between the junctions and circuit elements, and allow for an easy measurement of the critical current of the junctions. These test structures were grouped into special diagnostic chips with an area of 5×5 mm^2 and placed in many locations on process wafers containing about 200 various digital circuits on 5×5 mm^2 and 10×10 mm^2 chips.

The simplest diagnostic structure which allows simultaneous testing of multiple Josephson junctions is a series array of unshunted junctions shown in figure 1(a). The first test chip contained multiple 20-junction arrays of circular junctions of different radii, as shown in figure 1(b). This chip was used as a process control monitor for extracting the critical current density. Other test chips contain arrays of unshunted circular JJs of the same radius but connected in many possible ways to other circuit layers and structures in order to test pattern-dependent effects on Josephson critical current.

In all superconducting digital circuits, the electrical biasing scheme is such that electrical currents in logic cells return to the common superconducting ground plane M0. In addition, in many complex circuits the currents can also be returned to the common superconducting 'sky' plane (formed by parts of the second wiring layer M3) that also has a superconducting connection to the ground plane. As a result, Josephson junctions in circuits fall into two categories—those connected directly to the ground plane (let us call them 'grounded') and those connected to other junctions, inductors, bias resistors, etc (let us call them 'floating'). The grounded junctions can also be divided into several subcategories based on how the ground connection is made. From the standpoint of circuit design the ground connections of interest are those

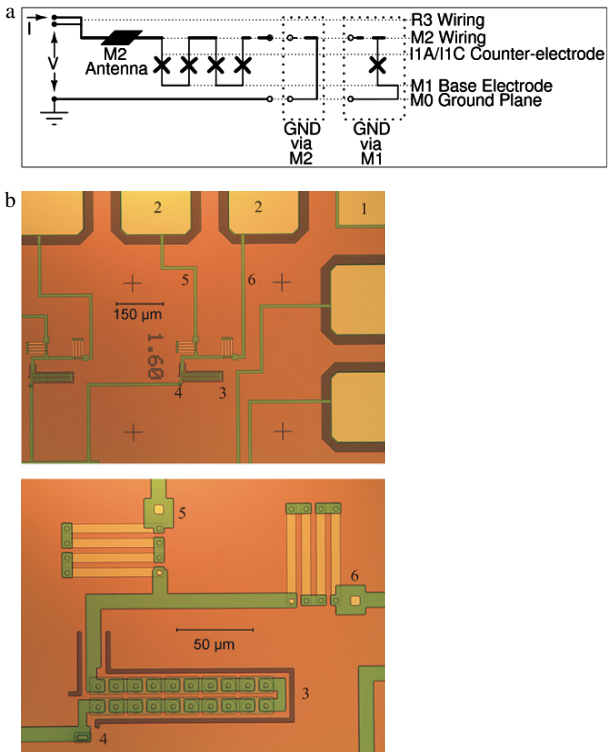

Figure 1. (a) Circuit diagram of a series array of Josephson junctions showing two possible connections of the last junction to the ground: M1-GND and M2-GND (see also figure 2). Superconducting layers are shown by solid horizontal lines, connections between the layers through contact holes in the interlayer dielectrics are shown by solid vertical lines, Josephson junctions are shown by crosses **x**. (b) Upper panel: fragment of the test chip containing arrays of circular junctions of different radii: (1) contact to the chip ground plane (ground pad) around the border of the chip; (2) signal contact pads around the chip edges make connections to the arrays; (3) arrays of Josephson junctions. Lower panel: blow-up of the junction array showing (4) connection to the ground plane, (5) voltage lead and isolation resistor (50 Ω), (6) current lead and isolation resistor (50 Ω).

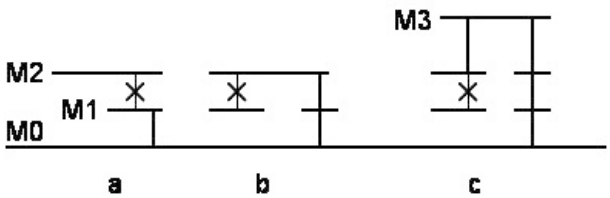

Figure 2. Schematic representation of Josephson junctions with different connections to the circuit ground plane (layer M0): (a) grounded base electrode (M1-GND); (b) grounded counter electrode (M2-GND); (c) connection through the 'sky' plane (M3-GND). All metal layers are separated by SiO_2 dielectric layers in which contact holes are etched to make the connections shown.

that have low inductance. First of all, it is a connection to M0 ground plane by the junction base electrode M1 through a contact hole in layer I0, as shown in figure 2(a). We will refer to such junctions as M1-grounded (M1-GND). The second is a connection of the junction counter electrode I1A to a grounded patch of layer M1 by a short piece of M2 wiring, as shown in

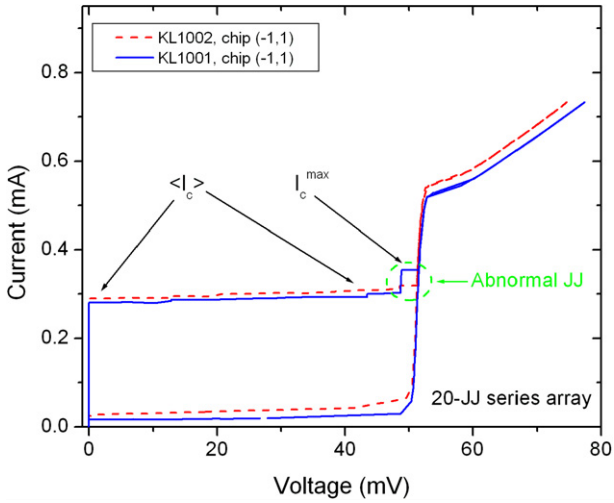

Figure 3. Current–voltage characteristics of a 20-junction array of circular junctions fabricated in two different fabrication runs. Both test chips have the same location (−1, 1) on the wafers. Arrays from wafer KL1002 show the usual I–V characteristics, arrays from wafer KL1001 show abnormal I–V characteristics with one junction in the array significantly deviating from the average. The abnormal junction is denoted as I_c^{max}. The average critical current $\langle I_c \rangle$ was calculated by excluding the abnormal junction.

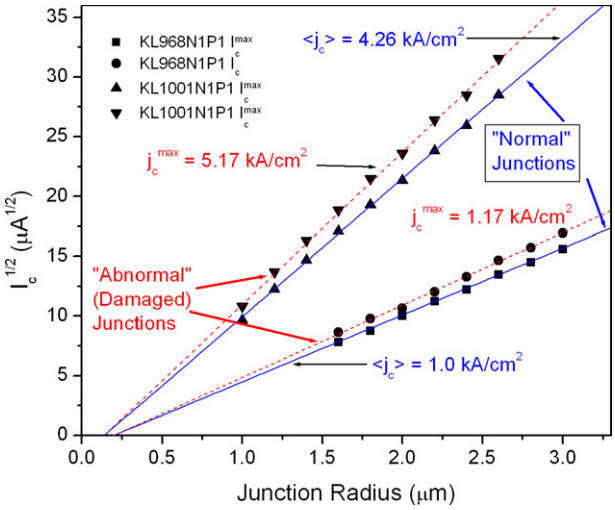

Figure 4. Dependences of the Josephson critical current on the junction radius, r, for two test chips with different target critical current density of trilayers. Both the average critical current $\langle I_c \rangle$ and the critical current of the abnormal junction I_c^{max} follow the same scaling dependence $I_c = j_c\pi(r - dr)^2$ shown by the solid and dashed lines, respectively, where dr is the junction radius deviation from the design value. The critical current density of abnormal (grounded) junctions is systematically higher than the critical current density of the floating junctions in the arrays.

figure 2(b). In this case the M1 patch is grounded through the I0 contact hole and the M2 wire connects through contact holes in interlayer dielectric (layers I1B-1 and I1B-2). We will refer to such junctions as M2-grounded (M2-GND). The third is a connection of junction CE to the M3 'sky' plane, as shown in figure 2(c). It requires a contact hole in the I1B layers, a patch of layer M2 and a contact hole in the I2 dielectric layer. This type will be referred to as M3-grounded (M3-GND).

3.2. Experimental procedure

Many full fabrication runs were done using trilayers with target critical current densities of 1.0, 4.5 and 20 kA cm^{-2}. Each fabrication run has a unique identification number which will be used below, e.g. KL1001. Locations of the centers of test chips on the wafers are given in Cartesian coordinates, e.g. $(-1, -1)$ in units of 5 mm. The fabricated chips were tested in liquid helium using an automated test setup Octopux [16] by performing four-probe current–voltage (I–V) characteristics measurements on each array.

3.3. Anomalous I–V curves of series arrays with grounded junction

Figure 3 presents the typical I–V characteristics of a 20-junction array measured on two chips of the same location (near the center of the wafer) on two wafers fabricated in sequential processing runs. The type of ground connection is M2-GND. The chip from wafer KL1002 shows what we consider to be the usual I–V characteristics showing a normal spread of junction critical currents typical for small random fluctuations. The chip from wafer KL1001 shows an abnormal behavior where one junction in the array significantly deviates from the average. The appearance of such abnormal I–V characteristics shows some statistical behavior; overall it has been observed in more than 50% of ∼100 wafers fabricated during the last 4 years. We find that only one junction in the array (or two in some special cases) shows this abnormal deviation. The deviation is always toward the higher I_c and, hence, cannot be explained by magnetic flux trapping near the junction because the latter can only reduce the I_c. Although the amplitude varies from run to run, the deviation is many times larger than the 1σ standard I_c deviation in the normal case. Hence, it cannot be explained by a random fluctuation of the junction size or the barrier transparency. The amplitude of the deviation does not depend on the number of junctions in the array. The appearance of the abnormal I–V characteristics is independent of the average trilayer j_c. The abnormal I–V curves have been observed from time to time for all the studied j_cs between 30 A cm^{-2} and 20 kA cm^{-2}.

We define the average critical current of the array $\langle I_c \rangle$ by excluding the abnormal junction with its critical current denoted as I_c^{max}. Figure 4 shows the dependence of the average critical current $\langle I_c \rangle$ and the I_c^{max} on the JJ radius on the photomask (design size) for all arrays on the test chip from two wafers with different trilayer critical current densities. Clearly, the abnormal junction I_c scales with the junction area in the same manner as the rest of the junctions, $I_c = \pi j_c(r - dr)^2$, and fitting gives the same junction size bias dr in both cases. This fitting parameter describes the difference between the junction radius on the photomask and on the wafer. The same value of dr means that the abnormal junction does not differ in size from the rest of the junctions in the arrays, i.e. there is no giant fluctuation in the junction size. The main difference is that all abnormal junctions in different arrays on the same chip have higher j_c than the rest of the junctions on the chip. Moreover, they all have the same j_c. That is there was something, some physical phenomenon during the wafer

fabrication, that caused a cooperative change in the critical current density of 18 particular junctions (one per array) on the test chips.

How do these JJs separated by ∼200–300 μm know about each other's existence and what allows them to change j_c cooperatively? What do they have in common? The only plausible answer is that they are all connected to the ground plane (M0) as shown in figure 1(a). That is, the abnormal JJ is the last, connected to the ground, junction in the array. This assumption was verified by testing a single JJ connected in the same way as the last (grounded) junction in the test array. Whenever the arrays show the abnormal I–V curve, the single junction also exhibits a critical current that is higher than expected from the designed j_cA value. All these facts indicate that there is a difference in the critical current of the floating and grounded junctions. This difference is fabrication dependent and has statistical behavior. We suggest that this phenomenon is a result of plasma process-induced damage to the thin oxide barrier in grounded junctions that is amplified by the 'antenna' effect. That is, for grounded JJs a ∼5 × 5 mm^2 metal ground plane acts as a charge-collecting antenna that amplifies the total current that can be channeled through the JJ at the later plasma processing steps. Floating junctions are not connected to this metal antenna and do not have charging currents flowing through them during the fabrication, and hence are not damaged. This will be discussed in more detail in section 4.

3.4. Antenna effect of the junction wiring and ground plane

In order to study the antenna effect on I_c of JJs, we used series arrays of 10 circular JJs with a metal structure (antenna) in layer M2 connected to the first JJ as shown in figure 1(a). The size and shape of the antenna were unique for each array. The last junction in the array had M2-GND connection. It was observed that one or two JJs in each array significantly deviate from the average. The average critical current $\langle I_c \rangle$ was calculated by excluding the two highest and two lowest critical currents in the array in order to minimize the possible effect of trapped magnetic flux. The highest I_c (the most damaged JJ$_c$) normalized to the average, $I_c^{max}/\langle I_c \rangle$, is plotted in figure 5 as a function of the M2 antenna area. It is seen that the amplitude of deviation from the average has a clear tendency to increase with the area of antenna M2, though there is a big scattering of the data points, indicating that the damage has statistical (probabilistic) character. For a comparison, the data are presented for an identical array that does not have an M2 antenna but has an M1-GND type of connection of the last junction to the ground. It can be seen that the damage effect is much stronger in this case, indicating that a large (∼5 × 5 mm^2) metal structure (the chip ground plane) that gets connected to the junction at the trilayer deposition step acts as a charge collecting antenna that amplifies the total current that can be channeled through the JJ at later plasma processing steps.

3.5. Spatial distribution of plasma-induced damage on wafers

In order to characterize the spatial distribution of the observed damage effect across process wafers, we used a test chip with 20-junction arrays of circular junctions of the same radius which have M1-GND grounding of the last junction, because

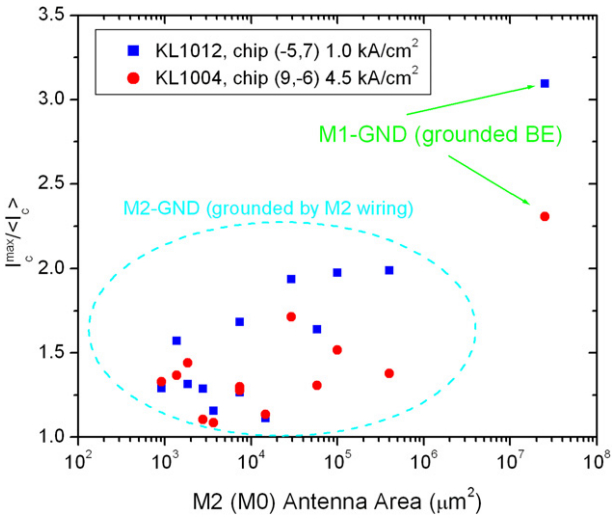

Figure 5. Dependences of the maximum critical current in 10-junction test arrays on the size of the metal structure (antenna) connected to the array (as shown schematically in figure 1(a)). The junction size r is 2 and 1 μm for the wafers with 1.0 and 4.5 kA cm^{-2} critical current density, respectively. The last junction in the arrays is grounded as M2-GND, except one array with M1-GND connection and no antenna in the M2 layer. In this case, the area of the M0 ground plane was taken as the antenna area.

such junctions demonstrate the largest, and hence more easily detected, deviation (see figure 5). The ratio $I_c^{max}/\langle I_c \rangle$ was used as the damage metric. The typical distributions are shown in figures 6(a) and (b). It can be seen that the damage is very small or nonexistent in the center of wafers and strongly increases toward the edges.

4. Discussion of the results

4.1. Damage to M1-gounded junction

As has already been mentioned, we suggest that the cause of the critical current enhancement in some particular (e.g. grounded) junctions or junctions connected to metal antennas is plasma-induced electrical stress (charging damage) to the tunnel barrier. Let us consider how this damage may occur in the simplest case of an M1-grounded junction and why it occurs only in M1-grounded junctions in the array.

For electrical stress (plasma-induced damage) to occur, two events must happen. A sufficiently high voltage must develop across the junction and electric current must be able to flow through the junction. For these to happen, both the junction counter electrode and the base electrode must be exposed to plasma at the same time. There are two processing steps when this happens and only for M1-GND junctions. The first is at the end of the contact hole etching to the junctions and during the overetching. In the HYPRES process, contact holes to the junction CE are etched simultaneously with contact holes to the M1 (base electrode) layer and with contact holes to the ground plane at the chip edges, as shown in figure 7. At the end of the contact hole etching, the counter electrodes of all junctions in the array are in electric contact with the plasma but only the M1-GND junction also has the electrical contact between its base electrode and plasma through the ground

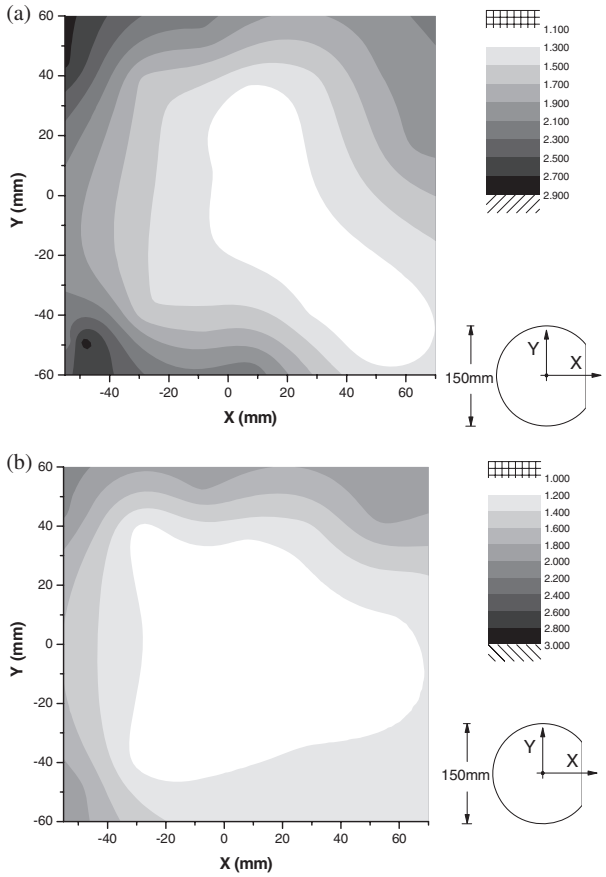

Figure 6. The typical distribution (in grey scale) of the normalized critical current in damaged junctions $I_c^{max}/\langle I_c \rangle$ over a 150 mm wafer: (a) the last JJ in the test arrays is M1-GND, (b) the last junction is M2-GND. Both types of array are located close to each other on the test chips and are identical in all other respects. The darker the shade of the area the larger the deviation of one junction in the test arrays from the average.

plane. Base electrodes of all other junctions in the array are electrically floating and no current can flow through them. If the plasma potential is nonuniform [13] or an electron shading effect [8] exists because the contact hole to the junction is small whereas ground contacts present very large open areas, a voltage can develop across the M1-GND junction and electric current can flow from the plasma through the ground plane to junction BE, through the junction and back to the plasma. The ground plane in this case works as a charge collecting antenna of very large area. The amount of damage should depend on the etch parameters and the time of overetching that is needed to clear the Nb surface from SiO_2 because of the difference in SiO_2 etch rate in small contact holes to junctions and large open areas of ground contacts. Exactly the same electrical situation happens during the RF-sputter cleaning in Ar plasma prior to the deposition of the first wiring layer (M2). The sputter cleaning is needed to remove a thin layer of natural oxide and adsorbed gases from all exposed surfaces of Nb in order to make good superconducting contacts with the M2 wiring layer. We should stress again that the situation is unique for M1-grounded junctions that are connected to a large antenna and have both electrodes connected to plasma at the same time. We are still collecting experimental data in order to determine if

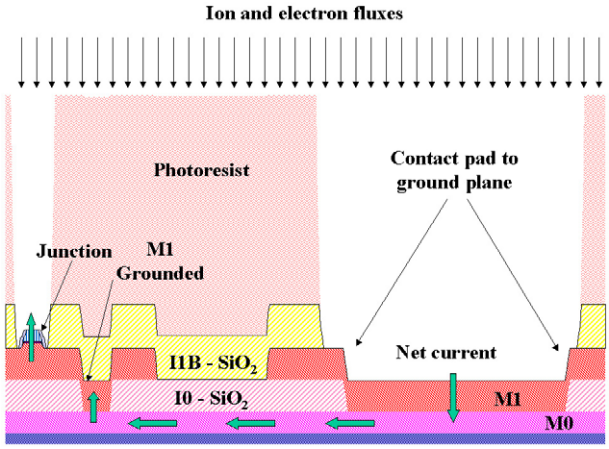

Figure 7. Cross-sectional representation of M1-grounded junction at the end of contact hole etching or at RF-sputter cleaning before deposition of layer M2. The contact holes are etched simultaneously to the junction counter electrode and to large ground pads (labeled 1 in figure 1(b)). If there is plasma nonuniformity or feature-dependent charging, current can flow through the junction due to its M1-GND connection. No current can flow if the junction is floating.

these processing steps indeed cause damage and how it can be reduced or completely eliminated.

4.2. Damage to M2-grounded junction

It is more difficult to propose a model explaining damage to M2-grounded junctions. In this case all junctions in the array are floating during the contact hole etch and RF-sputter cleaning discussed above. So no current can flow and no damage should occur at these steps. In order to cause damage, a voltage should develop either between the M1 islands of the junctions and the ground plane or between two parts of the array. The problem with the former is that M1 islands are covered by the dielectric SiO_2 layer. The latter could happen, e.g. during the M2 etching due to etch nonuniformity caused by the difference in the etch rate in dense circuit areas covered by many islands of photoresist and open areas, the so-called RIE lag. A model of gate oxide damage in MOSFETs and MOS capacitors during the metal (or polysilicone) gate etching based on the RIE lag was proposed in [14]. A qualitative picture modified for our case is as follows. After the deposition, the M2 layer shorts all junctions in the array and connects them to the ground plane at the edges of the chip and near the array. Almost up to the end of etching the M2 layer remains continuous and shorts all the junctions. At the end of etching the M2 layer breaks into several metal islands. One island is around the junction array (dense structure) and other islands cover large metal contact pads to the ground plane and the signal contact pads. All these contact pads are located at the border of the chip (see figure 1(b)) and covered by photoresist during the etching. The metal in open areas between large islands is etched away as shown in figure 8, upper panel. In the so-called overetching step, the metal in dense areas between small features covered by photoresist will be etched away. At some point in time, a thin layer of M2 remaining between a pair of junctions sharing the same pieces of the base electrode will lose continuity at some location between junctions i and $i + 1$ while all junctions from number 1 to

i and from $i + 1$ to N (N is the total number of JJs in the array) may still remain shorted by the unetched M2 layer as shown in figure 8, lower panel. At this moment, there will be a current transient flowing through junctions i and $i + 1$ that can potentially cause damage to these two junctions. The charges are collected by the halo around the perimeter of incompletely etched structures [14] forming a perimeter antenna. Usually, the overetching progresses from an open area towards the dense photoresist area. Therefore, it is likely that junction $i + 1$ is either the last junction in the array or junction i is the first junction in the array because both are the closest to the open area. As overetching continues, more and more junctions become separated and serially connected. The source of damage gradually diminishes because both the flowing current drops (due to decreasing antenna size and increasing resistance of the serially connected junctions and wiring) and the voltage across each junction also decreases (because the same potential difference is now applied to a progressively increasing number of serially connected junctions). So, depending on the details of the array design, damage to more than one junction could be observed in this case.

4.3. Possible damage during PECVD of the I2 interlayer dielectric

During the wafer plasma cleaning and the initial few seconds of SiO_2 PECVD there is a contact between the ends of the junction array and the plasma. So, current could flow if there is a potential difference between the ends due to the plasma nonuniformity. However, this process should uniformly damage all junctions in the arrays because they would share the same current. We did not observe such uniform damage to all junctions.

4.4. Possible mechanism of damage

First, for damage to occur a high enough voltage should develop across the junction. This voltage must be supplied by the plasma. Second, the plasma must also supply enough current through the junction to maintain this voltage because the junction is highly conductive due to the direct tunneling nature of the barrier. It is known from the plasma charging damage to MOSFETs that etching plasma can be viewed as a current limited voltage source. Although the potential nonuniformities can be quite large (tens of volts), the plasma currents are limited [13]. Let us estimate these parameters. The hard breakdown voltage, V_b, for Nb/Al/AlO_x/Nb junctions prepared by the same method as in this work but with much lower j_cs was measured by the V-ramp method in [12]. In the range of barrier oxidation exposures from 2×10^5 to 2×10^9 Pa s, the breakdown voltage was found to increase from 0.8 to 1.65 V. The tunnel barrier thickness was determined to be ~1 nm from the junction conductance–voltage measurements in the wide range of voltages [12, 17]. By extrapolating the breakdown voltage data to the range of oxygen exposures used in this work ($\sim 2 \times 10^4$ Pa s) we can estimate V_b in our junctions as ~0.6 V. This gives an estimate of the breakdown electric field of ~6 MV cm^{-1}. The irreversible changes to the barrier (soft breakdown) may start to occur at voltages three to four times lower. Also, a hysteresis in the junction conductance was observed at positive voltages on the counter electrode starting at ~0.4 V [12]. This feature was more pronounced in the thinner barriers. Note also that, strictly speaking, soft breakdown has statistical behavior and the voltage at which irreversible changes in the conductance become detectable depends on the measuring procedure, e.g. temperature, the voltage sweep rate, the total charge passing through the junction, etc. Therefore we can assume that the damaging level of voltages across the junction starts at $V_d \sim 0.1$ V, corresponding to an electric field of ~1 MV cm^{-1}.

For the typical M1-GND junction used in this work (figures 5 and 6) $I_c = 120$ μA and normal state resistance is $R_N \sim 12.5$ Ω. So the minimum current that must be supplied by the plasma in order to maintain a damaging level of voltage across the junction is $I_p \sim V_d/R_N \sim 8$ mA. There are ~20 grounded JJs on the test chip. So the total current supplied by the plasma to the chip should be at least ~160 mA. We have found here tens of damaged chips on the wafer. So the total current to the wafer should be much larger. For the typical RIE etching conditions used in this work the saturated ion current density from plasma to the wafer is ~1 mA cm^{-2}. So in the steady state the required current cannot be supplied by the ion current. The electron current density from the plasma can be many times larger than the ion current density. However, the total charge on the wafer is balanced over the RF power cycle. So the excess ion flux coming to some parts of the wafers where the plasma potential is high should be balanced by an electron current to other parts of the wafer where the plasma potential is low. Even if the entire wafer collects ion current and channels it through a single test chip, the resulting current is not sufficient to cause damage to many junctions.

Therefore we are left to conclude that the observed damage cannot result from a steady state process, but can only occur as a result of some fast transients when large currents are generated due to a high derivative dQ/dt (where Q is accumulated charge) or very large plasma instabilities such as arcing. At the power levels used in our etching processes (40–150 W) plasma arcing is very unlikely. Moreover, we constantly monitor the plasma optical emission intensity during the etching and never observed any spikes in the light emission that would be signatures of arcing. Higher power levels (250–300 W) are used for RF sputter cleaning in Ar plasma before depositing metal layers. So this processing step is more likely to be a source of damage than etching.

A much higher power of 2250 W is used for dc magnetron sputtering of all metal layers. The magnetron plasma is known to be very intense and nonuniform. Whereas etchers operate in the glow discharge regime, magnetron sputtering occurs in the superglow discharge close to the arcing instability where large variations in plasma intensity may take place. Also, since dc power is used, there is no blocking capacitor between the wafer and the system ground (as in the RIE case), preventing large dc currents from flowing through the wafer to the ground. For most of the deposition time the wafer is covered by a conducting metal layer that connects all the junctions together (e.g. during the M2 deposition) and is expected to safely channel all small charging currents to the conducting wafer holder (pallet). It would be interesting to investigate if plasma damage could happen in the very beginning of metal sputtering before a continuous layer of metal is formed over the wafer.

On the other hand, if a large plasma instability (e.g. arcing) happens during the M2 deposition when the entire wafer is

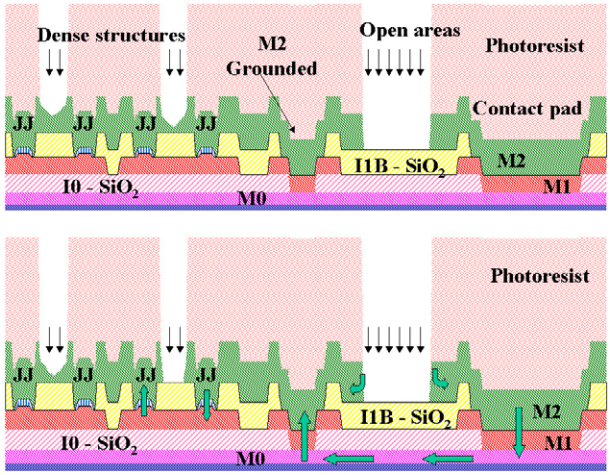

Figure 8. Cross-sectional representation of the M2-grounded junctions (fourth from the left) at the end of M2 etching (upper panel) when large contact pads have separated from the dense area of the array, while the Josephson junctions are still connected by an incompletely etched Nb layer between small islands of photoresist (PR) in the dense area due to the RIE lag. The lower panel shows a moment of separation of the last JJ (M2-GND) in the array from the rest of the junctions. A current transient may occur at this moment, with current flowing between the islands as shown by the arrows.

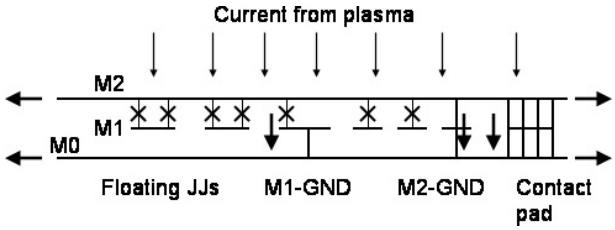

Figure 9. A schematic representation of the current passes if charging occurs in the presence of a continuous layer of M2 metal (e.g. during M2 deposition by dc magnetron sputtering). Since all metal films and contacts are resistive at room temperature, a resistive divider forms allowing part of the charging current to flow through M1-GND junctions. No large currents can flow through the floating junctions if the I0 dielectric layer under their base electrodes maintains electric integrity.

covered by a thin conducting metal, a very large current burst (a few amps for a few microseconds) could flow to the metal surface. A resistive divider exists between three current paths, as shown in figure 9. A part of the current can flow along the M2 surface to the wafer edges. The other part can reach the ground plane M0 through the contacts between the M2 layer and the ground plane and flow along M0 mostly toward the wafer edges (thermal oxide under M0 and on the back side of the wafer impedes the current flow through wafer to the pallet). And finally, the third part of the current will flow through M1-grounded junctions to M0 and again toward the wafer edges. This current component may cause electrical damage to the junctions. The size of this current (and hence the degree of damage) will depend on the distances between the grounded junctions and contact holes, the size of contact holes, the size and number of grounded junctions and other circuit design parameters. Since all the currents are flowing toward the edges of the wafer, the current through the junctions at the edges of the wafer will be larger than in the center. The last two observations are in full agreement with our experiments.

5. Conclusions

In conclusion, we have studied the current–voltage characteristics of the arrays of Nb/Al/AlO_x/Nb Josephson junctions fabricated on 150 mm wafers by an 11-level process for superconducting digital integrated circuits. We have found that the critical current of Josephson tunnel junctions can significantly depend on whether the junctions' base electrode is floating or grounded during the fabrication process. We have also found that the critical current of floating junctions can depend on the junction environment such as connections to other metal structures, layers and circuit elements. The critical current increases with the size of metal antenna connected to the junction. The observed phenomena have statistical character and depend on the location of the junctions on process wafers. We proposed an explanation of the observed phenomena based on plasma process-induced electric stress to ultrathin tunnel barriers. We identified the potentially most damaging plasma processing steps at which a sufficient voltage can develop across the tunnel barrier and the plasma can support enough current. We estimated that the observed damage of many Josephson junctions is unlikely to happen during the RIE processes due to plasma current limitations. We suggested that large plasma instabilities, e.g. during dc magnetron sputtering of the wiring layers, are a more likely source of damage due to much larger dc plasma current and power. We explain how this damage could happen based on the resistive division of the current between the grounded junctions and the wiring layers. Additional experiments are needed in order to detect the assumed plasma instabilities and, if confirmed, eliminate them. More experiments are needed in order to explain the damage to M2-grounded junctions.

The observed pattern-dependent effects on the Josephson critical current are crucially important for superconducting digital electronics that relies on accurate and predictable values of the Josephson critical currents in logic cells. Therefore, the observed plasma process-induced variations of Josephson critical currents in superconducting integrated circuits are probably the most important root cause of low circuit yield, reduced margins of operation and degradation of high frequency performance in superconducting microelectronics. The problem can be alleviated by introducing design rules restricting the size of metal antennas connected to the junctions and appropriate software tools for finding and eliminating large antennas as well as by advancing the fabrication process towards minimizing the plasma process-induced damage.

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