20 kA/cm^2 Process Development for Superconducting Integrated Circuits With 80 GHz Clock Frequency

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***Abstract*—Results of the development of an advanced fabrication process for superconductor integrated circuits (ICs) with 20 $\mathrm{kA/cm^2}$ $\mathrm{Nb/AlO_x/Nb}$ Josephson junctions is presented. The process has 4 niobium superconducting layers, one $\mathrm{MoN_x}$ resistor layer with 4.0 Ohm per square sheet resistance for the junction shunting and circuit biasing, and employs circular Josephson junctions with the minimum diameter of 1 μm; total 11 photolithography levels. The goal of this process development is the demonstration of the feasibility of 80 GHz clock speeds in superconducting ICs for digital signal processing (DSP) and high performance computing. Basic components of Rapid Single Flux Quantum (RSFQ) logic such as DC/SFQ, SFQ/DC converters, Josephson transmission lines (JTLs), and simple digital circuits such as T-flip-flops and 4-bit digital counters have been fabricated and tested. The T-flip-flops were shown to operate up to 400 GHz with the widest margin of operation of $\pm$13% at 325 GHz. Digital testing results on the 4-bit counters as well as the junctions, resistors, and other process parameters are also presented. Prospects for yet higher speeds and very large scale integration are discussed.**

***Index Terms*—Digital integrated circuits, Josephson device fabrication, Josephson junctions, molybdenum nitride, superconducting integrated circuits, toggle-flip-flop.**

I. Introduction

SINCE the development of manufacturable $\mathrm{Nb/AlO_x/Nb}$ Josephson junctions over 20 years ago, the operating (clock) speed and integration level of digital superconducting integrated circuits (SICs) have been slowly increasing and recently approached ~15–18 GHz for relatively complex circuits containing ~6,000 Josephson junctions such as analog-to-digital converters (ADCs) [1], [2] and other digital signal processing (DSP) and computing circuits [3]. The progress in SICs has been basically limited by the fabrication processes with a few micrometers minimum Josephson junction (JJ) size and modest Josephson critical current density, j_c of 1 and 2.5 $\mathrm{kA/cm^2}$ [4]–[6]. With clock speeds of desktop computers approaching now 4 GHz and still growing, such speeds of superconducting ICs do not make the use of superconductor digital electronics easily justifiable. On the other hand, it is well known that the ultimate speed of single Josephson junctions as well as very simple digital circuits (containing a few JJs) is limited by the junction I_cR_n product or the gap frequency of the junction electrodes, and can be as high as ~770 GHz for Nb-based technology [7], [8]. For complex SICs this could translate into ~100–120 GHz clock frequencies.

In order to shrink this gap in performance, early in 2004 we upgraded the existing 1.0 $\mathrm{kA/cm^2}$ fabrication process and launched a more advanced process with JJs of 1.5 μm minimum size and $j_c = 4.5\ \mathrm{kA/cm^2}$ [9], [10]. This process was aimed at enabling ~40 GHz clock frequencies. Since then, a large number of complex digital superconducting circuits have been fabricated at HYPRES Inc., and the significant improvement in the speed, integration level, and performance has been achieved. Among them are digital mixers with 43 GHz clock [11], low-pass (LP) ADCs (~5,100 JJs) with ~34 GHz clock [12], multi-rate LP ADC with up to 25.6 GHz clock [12], I&Q channel receivers (channelizers) with ~16.6 GHz clock and ~10,000 JJs [13], band-pass ADCs, etc.

Another process with 8 $\mathrm{kA/cm^2}$ JJs was developed at NGST [14]. Unfortunately, this superconductor foundry was shut down.

Yet a more advanced planarized process with 1-μm JJs and 10 $\mathrm{kA/cm^2}$ j_c is being developed in SRL, ISTEC, Japan [15] with the goal of 75 GHz clock speeds. Although not quite there yet, a significant boost in circuits' performance is expected to be reported at this Conference.

Since the speed of RSFQ circuits scales roughly as $j_c^{1/2}$, the natural path of process development is to further increase the critical current density of Josephson junctions and continue shrinking the junction size. Therefore, in this paper we present the results of our new advanced process with 20 $\mathrm{kA/cm^2}$ $\mathrm{Nb/AlO_x/Nb}$ Josephson junctions and 1 μm minimum junction size that is being developed at HYPRES with the goal of enabling 80 GHz clock speeds in digital superconducting circuits containing $> 10^4$ JJs for applications in DSP and high performance computing. The process development and circuit re-design costs caused by the transitions to newer fabrication processes can be minimized by using the scaling approach present in Section II. The process details are given in Section III and Section IV, and the digital test results are presented in Section V.

II. Scaling the Junctions and Resistors

A significant part of the cost of establishing any new fabrication process is the cost of IC designs conversion (and process

Manuscript received August 22, 2006. This work was supported in part by the US Office of Naval Research Grant N00014-06-1-0021.

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Digital Object Identifier 10.1109/TASC.2007.898571

diagnostics) from an old process to the new one and associated cost of new photomasks. In order to minimize these costs and design labor, we implemented the following scaling approach. At transition from a process with the critical current density j_c^{old} (e.g., 1 $\mathrm{kA/cm^2}$) to a new process with higher critical current density j_c^{new} (e.g., 4.5 $\mathrm{kA/cm^2}$ or 20 $\mathrm{kA/cm^2}$), the critical currents of the junctions, I_{ci} are kept the same in order to preserve the same inductances in the logic cells. Therefore, the junction areas scale as $A_i^{new} = A_i^{old} \cdot (j_c^{old}/j_c^{new})$. Next, in order to preserve the proper shunting of the junctions $\beta_{ci} \sim 1$, (where $\beta_{ci} = 2\pi I_{ci} R_{si}^2 C_i/\Phi_0$ and R_{si} and C_i are the shunt resistance and capacitance of the i-th junction, Φ_0 is the flux quantum) and preserve the full shunt resistor design including the location of contact holes, the sheet resistance of the resistive layer in the new process is scaled, accordingly, as $\mathrm{R_{sq}^{new}} = \mathrm{R_{sq}^{old}}(j_c^{new}/j_c^{old})^{1/2} \cdot (C_s^{old}/C_s^{new})^{1/2}$, where C_s is the junction specific capacitance. For example, for the transition from the HYPRES' 1 $\mathrm{kA/m^2}$ process to 4.5 $\mathrm{kA/cm^2}$ process, the $\mathrm{R_{sq}}$ of molybdenum resistors was increased from 1 to 2.1 Ohm/sq [9], [16]. When this approach is adopted, only two new photomasks are required—one for the junction counter electrode (CE) layer (I1A) and another one for the wiring layer to the junctions CE (M2). (This one is needed only to adjust the length of the bias resistors and, hence, preserve the original circuit bias voltages.) The remaining 9 photolithography layers can be kept unchanged. Another advantage of this approach is that any circuit on the single set of photomasks can be fabricated by either the old or new process or both and hence the performance increase can be easily evaluated. Design conversion errors can also be minimized.

The disadvantage of the above approach is that the circuit density remains unchanged. Also the parasitic capacitance of wiring layers increases with respect to the junction capacitance. We believe that the advantages of our approach on the research and development stages of superconductor microelectronics outweigh the disadvantages. Some circuits re-optimization involving other layers (e.g., M2) may be required in the future commercialization stages.

III. $\mathrm{MoN_x}$ Resistors

It follows from the above discussion that for the 20 $\mathrm{kA/cm^2}$ process it would be convenient to have the resistor material with $\mathrm{R_{sq}} \sim \sqrt{20}\,\mathrm{Ohm/sq}$ if one neglects the increase in C_s. Since no exact data on the C_s are available yet (and the estimates give $\sim 85\,\mathrm{fF}/\mu\mathrm{m}^2$), the target $\mathrm{R_{sq}}$ for the process was set at 4.0 Ohm/sq at 4.2 K. In the existing HYPRES' processes, molybdenum films are used as the resistor material, with thicknesses of 70 nm and 40 nm for 1.0 and 2.1 Ohm/sq, respectively. The desired, two times higher sheet resistance could not be achieved by further decreasing the thickness of Mo films without compromising the resistors uniformity across 150-mm wafers. Therefore, a new resistor material, $\mathrm{MoN_x}$ was implemented.

Thin films of $\mathrm{MoN_x}$ were deposited by reactive dc magnetron sputtering of a molybdenum target in a mixture of Ar and $\mathrm{N_2}$. During the deposition, a pallet with two 150-mm wafers was scanned at a constant speed under the sputtering target. A Materials Research Corp. sputtering system was used. The film thickness was varied by varying the pallet scan speed; the film composition was varied by varying the $\mathrm{N_2/Ar}$ flow ratio. The deposition power was fixed at 2280 W. Fig. 1 shows the dependence of the sheet resistance at room temperature on the nitrogen content in the sputtering mixture.

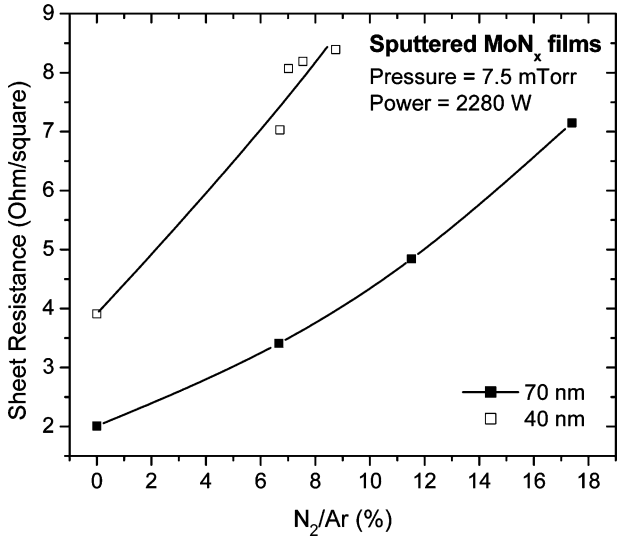

Fig. 1. Average sheet resistance of MoNx films at room temperature as a function of $\mathrm{N_2/Ar}$ ratio in the sputtering mixture. The pallet scan speed was adjusted to provide the $\mathrm{MoN_x}$ film thicknesses of 70 nm and 40 nm. Data points are connected to guide the eye.

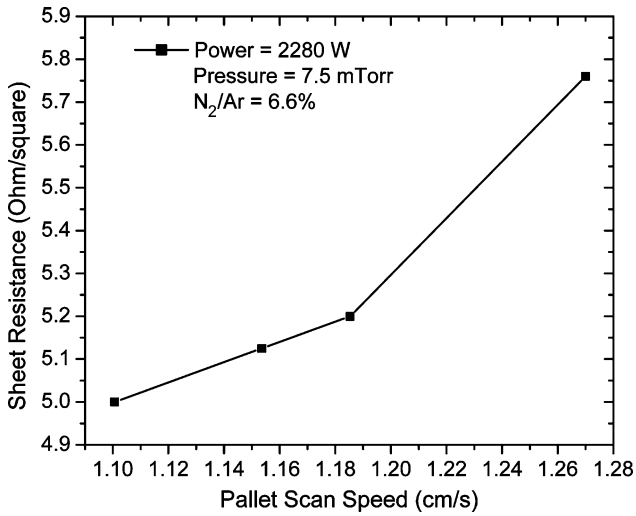

Fig. 2. Average sheet resistance of $\mathrm{MoN_x}$ films at room temperature as a function of the pallet sacn speed during reactive sputtering in $\mathrm{N_2 + Ar}$ mixture. The thickness of the films changes from 55 nm to 46 nm and scales inversely with the pallet speed. Data points are connected to guide the eye.

It was found that the residual resistivity ratio $R_{300\ \mathrm{K}}/R_{4.2\ \mathrm{K}}$ for $\mathrm{MoN_x}$ films rapidly decreases from 1.85 when no $\mathrm{N_2}$ is added to 1.27–1.30 at $\mathrm{N_2/Ar} > 5\%$. Therefore, the target $\mathrm{R_{sq}}$ at room temperature was set at 5.2 Ohm/sq. To achieve the best reproducibility of the process, the deposition power and $\mathrm{N_2/Ar}$ ratio were fixed, and the fine $\mathrm{R_{sq}}$ adjustments were made by varying the film thickness through the pallet scan speed as shown in Fig. 2.

The $\mathrm{MoN_x}$ films were patterned using photolithography and reactive ion etching (RIE) in $\mathrm{SF_6}$ at 4.0 Pa and 40 W RF power. This produced an etch rate of about 25 nm/min with excellent se-

lectivity to the photoresist and underlying SiO_2. The uniformity of the thickness and the sheet resistance across 150-mm wafers were measured using, respectively, a profilometer and patterned 4-probe configurations. It was found to be within $\pm 10\%$ (from min to max), acceptable for complex IC fabrication.

IV. Josephson Junctions and Process Details

The process flow was kept exactly the same as the existing HYPRES' processes (see also the *Design Rules* in [16]). It is as follows:

1) Nb ground plane (100 nm) deposition on thermally oxidized 150-mm Si wafers, layer M0.
2) M0 photolithography and RIE.
3) SiO_2 interlayer insulator (150 nm) deposition, layer I0.
4) I0 photolithography and RIE to open contact holes to M0.
5) $Nb/AlO_x/Nb$ trilayer deposition. Base electrode (BE) thickness is 150 nm, CE is 50 nm. Al layer is 8 to 10 nm. Oxygen exposure for 20 kA/cm^2 trilayers is 56 $mTorr \cdot min$.
6) CE (I1A layer) photolithography and RIE to form JJs.
7) BE anodization at 30 V in ammonium pentaborate solution forming Al_2O_3/Nb_2O_5 insulating bilayer (layer A1) over the entire wafer.
8) A1 photolithography and ion milling to remove the anodized layer everywhere but around the JJs.
9) BE electrode (M1) photolithography and RIE.
10) SiO_2 interlayer dielectric deposition (100 nm).
11) Resistive layer (Mo or MoN_x) deposition, layer R2.
12) R2 photolithography and RIE to form the resistors.
13) SiO_2 interlayer dielectric deposition (100 nm). Steps #10 and #13 form layer I1B.
14) I1B photolithography and RIE to open contact holes to JJs (I1A), resistors (R2), and BE (M1).
15) Nb wiring layer deposition (300 nm), layer M2.
16) M2 photolithography and RIE.
17) SiO_2 interlayer deposition (500 nm), layer I2.
18) I2 photolithography and RIE to open contact holes to M2 layer.
19) Second Nb wiring layer deposition (600 nm), layer M3.
20) M3 photolithography and RIE.
21) Multilayer Ti/Pd/Au contact pad metallization deposition, layer R3. Patterning by either lift-off process or ion milling.

The process has a total of 11 photolithography levels. The photolithography was done using $1\times$ full wafer projection. We achieved the theoretical resolution limit with the minimum feature size of 1 μm for lines and spaces, $a_{min} = k_1\lambda/NA$, where $\lambda = 320$ nm is the average exposure wavelength, $NA = 0.16$ is the numerical aperture of our exposure tool, and k_1 is the process-dependent parameter. Since no optical proximity correction or phase shifting masks was used, $k_1 \sim 0.5$ and a_{min} is 1 μm. By carefully controlling the aligner focusing, exposure and resist development parameters, 0.8 μm single lines and 1 μm in diameter circular JJs were produced.

Due to the presence of an anodization oxide bilayer around the junctions, contact holes to JJs can be made larger than the JJs themselves. The typical contact holes used were 2 μm in diameter. A summary of all minimum sizes, layer spacings and overlaps is given in [16].

Etching of all Nb layers and resistor layer was done using RIE in an SF_6 plasma at 4.0 Pa pressure and 40 W RF power. Etching of contact holes was done using RIE in CHF_3/O_2 plasma at 150 W RF power. The O_2 content in the mixture was adjusted to achieve the slope of the contact hole walls that provides good Nb step coverage. An optical emission end-point detector was implemented both for Nb and SiO_2 etching to minimize the overetching and potential plasma damage.

SiO_2 interlayer dielectric was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) using tetra-ethyl-orthosilicate (TEOS) $vapor/O_2$ plasma at 100–150°C. The typical deposition rate of 3 nm/s was used.

The process is easily scalable to submicron dimensions on all the layers if a more advanced lithography tool becomes available. Also the process can easily incorporate an electron beam writing tool for deep submicron junctions (and I1B contact holes) whereas all other layers are done by optical lithography.

A set of process control monitors (PCMs) with arrays of un-shunted and shunted junctions, and other diagnostic test structures was implemented as described in details in [9], [17]. $I-V$ characteristics of the 20 kA/cm^2 JJs of different sizes were measured, showing R_{subgap} to R_n ratio ~4. The critical current of the junctions can be well described by $I_c = \pi j_c(r-dr)^2$ in the range of sizes of interest, where r is the junction radius and dr is the process bias; typically 0.2 μm [17]. For the digital circuits presented in the next section, compensation for the dr was done in the designs. The alternative is to compensate for the junction bias on the photomask. It is a standard approach in our 4.5 kA/cm^2 process [16]. JJ statistics is given in [17].

V. T-Flip Flop and Digital Counter

Several basic components of the RSFQ logic circuits have been fabricated by the new process. They include DC/SFQ and SFQ/DC converters, JTLs, toggle flip-flops (TFFs), and 4-bit counters. All the circuits use circular JJs with diameters ranging from 0.9 μm to 1.5 μm.

It became a custom to characterize the maximum operating speed of superconducting circuits using the maximum frequency of the divide by two operation of the static frequency divider based on the TFF gate [7], [8], [14], [18]. Our test circuit contains 20 JJs. The circuit diagram and layout will be shown elsewhere. The analog testing was based on comparing the input voltage and twice the output voltage (both related to the input and output frequency by the Josephson relation $hf = 2$ eV), and is similar to that reported in [7], [8], [14], [18]. The maximum input voltage (frequency) was measured as a function of the circuit bias current using an automated test set-up *Octopux* [19]. Contrary to the experimental procedures in [7], [8] where 4 independent current sources were used to bias a total of 8 Josephson junctions in the circuit, a single main bias was used in this work for the JTL and TFF as it is more appropriate for digital circuits. The second current source was used to control the DC/SFQ converter and vary the input frequency. The typical dependences of the input frequency applied to the divider (converted from the input voltage using $hf = 2$ eV) and the output frequency of the divider as a function of the bias current of the DC/SFQ converter are shown

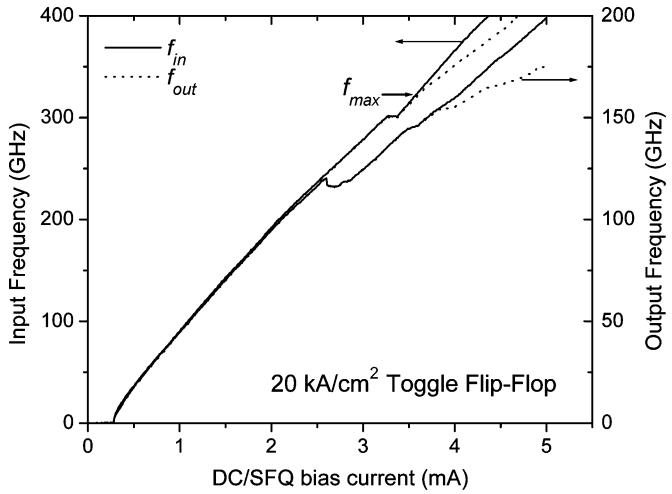

Fig. 3. Input frequency of the TFF (solid curves, left scale as indicated by arrow) and output frequency (dotted curves, right scale as indicated by arrow) as a function of the input bias current. The upper and the lower pair of curves correspond to the main TFF biases of 4.06 mA and 3.10 mA, respectively. The maximum operating frequency at a given bias, f_{max} corresponds to the point where $2 \cdot f_{out}$ starts to deviate from f_{in} (divide by two operation fails).

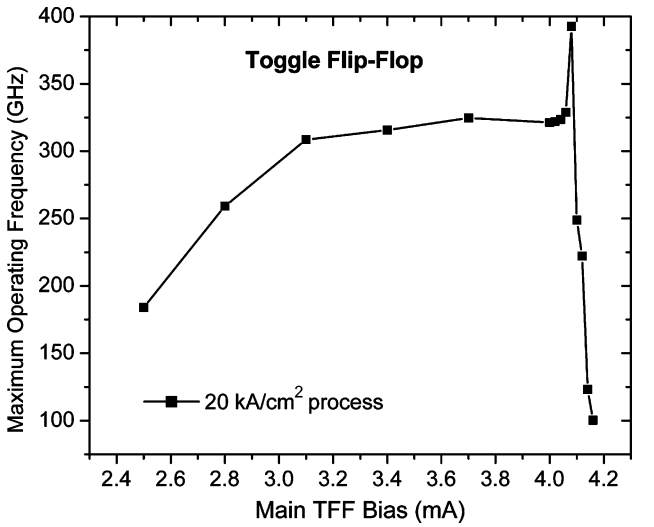

Fig. 4. Maximum operating frequency f_{max}, of the Toggle Flip-Flop (static frequency divider) as a function of the circuit's main bias. The absolute maximum corresponds to $f_{max} = 393$ GHz, whereas the widest margins of operation correspond to ~325 GHz input frequency.

in Fig. 3. Different curves correspond to the different main biases applied to the circuit. The frequency where $2f_{out}$ starts to deviate from f_{in} is the maximum operating speed, f_{max} at a given bias. This maximum frequency is shown in Fig. 4. It can be seen that the margins of the circuit operation are very wide. For instance, at 325 GHz input frequency, the margins on the main bias current are $\pm 13\%$. The margins shrink to zero at ~400 GHz. Please note that at this point the circuit is still not limited by the TFF speed but rather by the generation in the JTL. We conducted an additional experiment where the extra current source was used to separately bias the JTL between the DC/SFQ and the TFF. In this case the maximum operating frequency was found to be ~500 GHz.

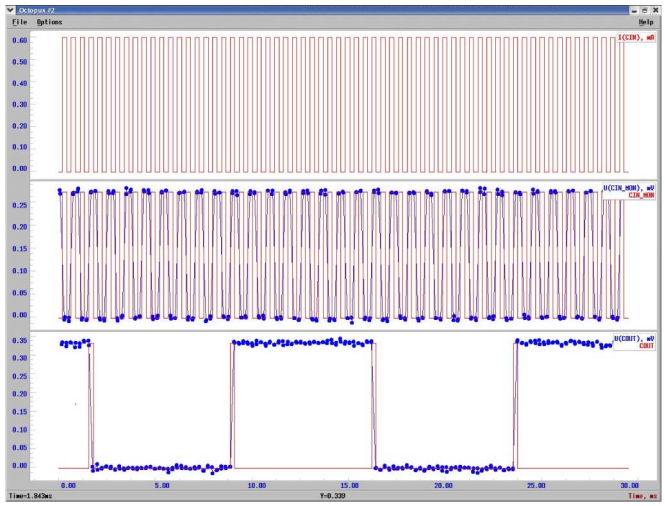

Fig. 5. Digital low-speed testing of the 20 $\mathrm{kA/cm^2}$ 4-bit digital counter. The panels show from top to bottom the applied pattern, the input SFQ/DC monitor, and the counter output, respectively. Bias margins are $\pm 27\%$.

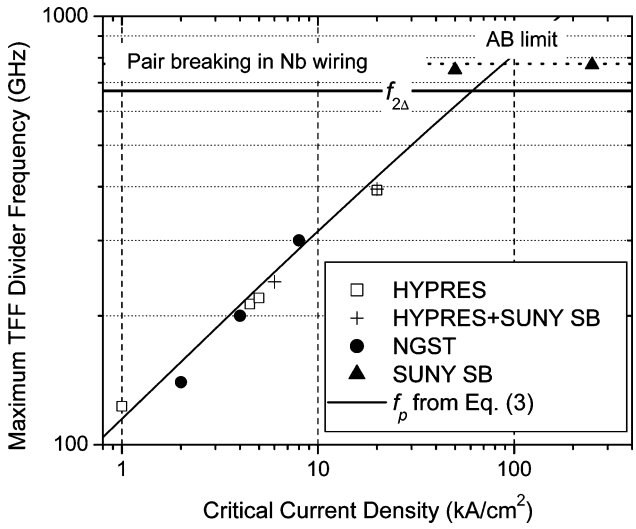

Fig. 6. Maximum frequency of operation of TFF-based frequency dividers fabricated in various Nb-based processes. HYPRES data are from the present work and [18]; HYPRES+SUNY SB data are from [18]; NGST data are from [14]; SUNY SB data are from [7], [8]. Above the gap frequency of Nb (~670 GHz) strong attenuation of SFQ pulses in Nb wiring and JJ electrodes should set in. The JJ plasma frequency f_p (3) is shown as a solid curve, AB limit as a dotted line.

The 60-JJs 4-bit digital counters were tested at a low speed using *Octopux* to verify the divide by 16 operation, evaluate the margins of operation, and the bit error rate (BER). The test results are shown in Fig. 5. The testing was performed over an 8-hour period. No bit errors were detected, setting the upper limit on BER at 10^{-6}.

VI. Discussion: Speed

The maximum TFF divider frequency, f_{max} has become the benchmark characteristic of SICs fabrication processes. For a comparison, the same TFFs as in Section V were also fabricated in 1 $\mathrm{kA/cm^2}$ and 4.5 $\mathrm{kA/cm^2}$ processes. A summary of the obtained and published data for various Nb-based processes is shown in Fig. 6.

The f_{max} should scale proportionally to the characteristic frequency of the Josephson junctions $f_c = I_c R_s/\Phi_0$ up to the plasma frequency $f_p = 1/(2\pi L_J C)^{1/2}$, above which Josephson oscillations become progressively shorted by the junction capacitance. Here L_J is the Josephson inductance, R_s, in general, is a parallel combination of the shunt resistance and the junction sub-gap resistance. If the junctions are critically damped ($\beta c = 1$), then

$$f_c = f_p = (1/2\pi\Phi_0)^{1/2} \cdot (j_c/C_s)^{1/2}. \quad (1)$$

In the simplest model, j_c decays exponentially whereas capacitance decreases inversely with the tunnel barrier thickness. This leads to an expression $1/C_s = P_1 - P_2 \cdot \log_{10}(j_c)$. Fitting to the C_s data obtained from SQUID LC resonances and plasma resonance measurements [16], [17] gives $P_1 = 1.72 \cdot 10^{-2}$ and $P_2 = 4.3 \cdot 10^{-3}$ when j_c is in units of $\mathrm{kA/cm^2}$ and C_s is in $\mathrm{fF}/\mu\mathrm{m}^2$. Substituting this into (1) we get

$$f_p = \left[j_c^{1/2}/(2\pi\Phi_0)^{1/2}\right] \cdot [0.0172 - 0.0043 \log_{10}(j_c)]^{1/2}. \quad (2)$$

For j_c in $\mathrm{kA/cm^2}$, this becomes

$$f_p = 877.5 \cdot j_c^{1/2} \cdot [0.0172 - 0.0043 \log_{10}(j_c)]^{1/2} \quad (\mathrm{GHz}). \quad (3)$$

It can be seen from Fig. 6 that all the available data fall onto the f_p vs j_c dependence (3). Interestingly, in order to achieve the ultimate performance, TFFs in [14] were optimized for β_c values higher than 1 (up to 2.5) whereas no such optimization was done in this work and [18]. It is clear from Fig. 6 that this optimization does not offer any real speed improvement.

It is also clear from Fig. 6 that increasing the process current density above $\sim 60 - 70\ \mathrm{kA/cm^2}$ does not offer any advantages in the circuit speed even though the junctions eventually become self-shunted and no external shunts are required. Here, the $I_c R_s$ product is limited by the Ambegaokar-Baratoff (AB) relationship $I_c R_n = \pi\Delta/2e$ (2.1–2.2 mV for Nb) and, most often, for $\mathrm{Nb/AlO_x/Nb}$ junctions does not exceed 1.5–1.6 mV at 4.2 K due to strong coupling and proximity effect corrections. This translates into 725–775 GHz maximum frequency for Nb technology.

Worth noting is that the f_{max} of TFFs in [7], [8] is higher than the gap frequency $\mathrm{f_{2\Delta}} = 2\Delta/h$ (Δ is the energy gap) in Nb above which strong dissipation in the junction electrodes and Nb wiring is expected to set in due to pair breaking by Josephson oscillations. In this case the SFQ pulses should strongly attenuate if the distance between JJs in JTLs and logic cells is larger than the decay length. It is possible that double-SQUID TFFs in [7], [8] operated above $\mathrm{f_{2\Delta}}$ in some phase-locked mode that was achieved by using many bias sources, and also due to the Riedel's peak in the intensity of Josephson oscillations at 2Δ.

VII. Discussion: Integration Level

It is interesting to see how the maximum frequency of operation (maximum clock speed f_{cl}^{max}) scales with circuit complexity (level of integration). It is shown in Fig. 7. Unfortunately, experimental data are very scarce, especially for circuits with $> 10^4$ JJs. This limits the accuracy of our analysis.

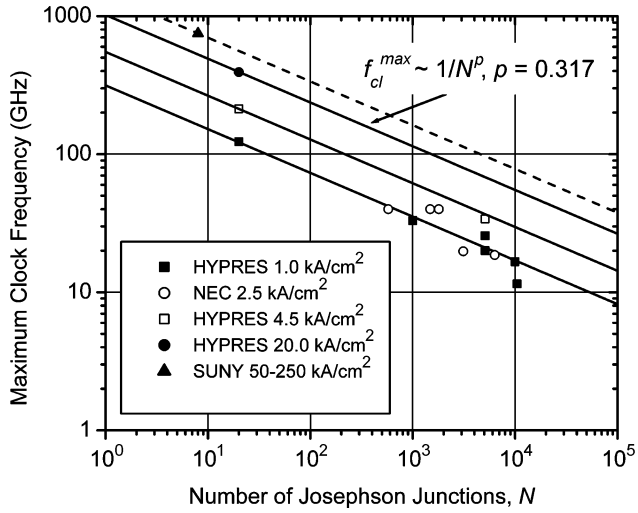

Fig. 7. Dependences of the maximum clock speed of RSFQ digital circuits on the number of Josephson junctions for the existing and projected Nb fabrication processes. The experimental data are from this work and [7], [8], [11]–[13]. The data for NEC process are from [3], [20]–[23]. Solid lines show the best fit to the data on 1 and 4.5 $\mathrm{kA/cm^2}$ processes, and projections for the 20 and a hypothetical 250 $\mathrm{kA/cm^2}$ (dash line) processes.

Though circuit dependent, the general tendency is that the f_{cl}^{max} decreases strongly with the circuit complexity that we characterized by the number of JJs, N. We find that, however limited, the data can be described by the power law decay $f_{cl}^{max} \sim 1/N^p$ with $p = 0.317$ for both the 1.0 and 4.5 $\mathrm{kA/cm^2}$ processes. By assuming that this dependence holds for other j_cs as well, we draw the projected speed dependences for the 20 $\mathrm{kA/cm^2}$ and for future 50–250 $\mathrm{kA/cm^2}$ processes. For a hypothetical circuit with 10^5 JJs that is, perhaps, the scale relevant to the most DSP and computing applications, the projected clock frequencies are 8 GHz, 15 GHz, and 27 GHz for 1.0, 4.5, and 20 $\mathrm{kA/cm^2}$ processes, respectively. For a hypothetical, yet to be developed, 250 $\mathrm{kA/cm^2}$ process, the same scaling gives 38 GHz maximum clock frequency. It is a factor of 3 less than the best expectations in the field of superconducting electronics, but still a factor of 10 better than the existing Si chips. (Note, that for a hypothetical $5 \cdot 10^7$ JJs circuit comparable to the current Si-based processor chips, the maximum projected frequency is only ~5 GHz, that is about the same as for the most advanced Si technology existing already today).

From the design point of view, it is not clear exactly why the circuit speed should significantly drop with the level of integration because, usually, only a small fraction of the circuit works at the highest frequency. From the data/clock timing consideration this highest frequency is $\sim f_c/7 \sim f_p/7$. Therefore, the data in Fig. 7 could be possibly explained by accumulation of timing errors due to jitter and random delays caused by variations of the circuit parameters as the circuit complexity grows. Computer simulations of some of these effects were presented in [24]. It may well be that more advanced chip architectures will be required in the future to address this performance vs. complexity issue. Also, for a complex circuit to operate, margins

of operation of the individual logic cells comprising the circuit should overlap. Since the margins of operation of all individual cells shrink with frequency and because of random variation of the parameters, the probability of finding this common overlap diminishes as the circuit complexity grows. Therefore, the observed decrease of the maximum clock speed with the number of JJs could well be also the fab/yield issue, and the question of how the random fluctuations of the circuit parameters could be eliminated by improving the fabrication processes and to what extent.

VIII. Conclusion

We developed an advanced fabrication process that enables superconducting digital circuits with clock frequency approaching 80 GHz. Benchmark test circuit shows maximum frequency of operation of ~400 GHz. Realization of the full 80 GHz speed potential in complex superconducting digital integrated circuits with more than 10^4 Josepshon junctions may require more advanced design architectures and further process innovations.

Acknowledgment

The authors would like to thank Mr. Anubhav Sahu and Mr. Saad Sarwana for helping us with some of digital testing, Prof. Vasili Semenov and Dr. Timur Filippov for useful discussions, and Dr. Deborah Van Vechten for support and encouragement.

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