Dual-Band ADC Utilizing Switch Matrix

Saad Sarwana, Dmitri Kirichenko, Deepnarayan Gupta, and Alex F. Kirichenko

***Abstract*—We have designed a multi-bit switch matrix for routing of digitized data streams from analog-to-digital converters (ADCs) to digital signal processors. A 2 × 2 version of the two-bit switch was designed and fabricated at HYPRES's standard 4.5 $\mathrm{kA/cm^2}$ fabrication process. The switch was successfully tested and demonstrated at high speed. The switch has been used as a part of a multi-band ADC system, routing data streams from two modulators to two DSPs.**

***Index Terms*—ADC, ADR, DSP, network switch, RSFQ.**

I. Introduction

A multi-band RF communication system consists of an antenna subsystem to capture electromagnetic energy in different RF bands and a transceiver subsystem to transmit and receive information from each RF band through a variety of signal processing steps (e.g., up/down-conversion, filtering, modulation, demodulation, coding, decoding). The antenna and transceiver subsystems interact through an RF distribution unit, which for all current systems resides in the analog domain. The goal for truly flexible operations is to dynamically distribute the available signal processing resources among the input bands to fulfill changing communication needs. This requires programmable RF distribution and routing [1].

This approach is well matched to the current level of maturity of superconductor electronics, featuring very fast (up to 40 GHz) digital circuits of modest complexity (10–20,000 Josephson junctions per chip). The receive side of a multi-band, multi-channel digital-RF communication system is depicted in Fig. 1.

II. The Switch

A. Design

The general switch architecture was described in [1]. For the purpose of this demonstration, we have designed its 2 × 2 2-bit version.

The block-diagram of the switch matrix is shown in Fig. 2. The routed data bus comprises a clock line and 2 data lines (one for each bit). Only the clock line is routed through a Non-Destructive Read-Out element (NDRO) [1], which stores the control information. All data lines go through the set of latches (RS flip-flops) [1] driven by the clock. Thus, if clock signal did not pass through the NDRO, the latches block data propagation (Fig. 3). Besides the obvious advantage in hardware saving, this simple approach allows to keep data in sync, thus increasing coherent throughput. The minor drawback of this approach is the necessity to clear the contents of RS flip-flops after every reprogramming of the routing table of the switch. It occurs automatically with the first clock pulse sent to all input ports preceding the data stream. Obviously, the output produced by this pulse has to be discarded. For most DSP applications (including the one described in this paper) this is not a relevant issue.

The block-diagram and layout of a single node of the 2-bit switch matrix is shown in Fig. 3. The data bus was designed in such way, so it can be easily extended to a higher number of

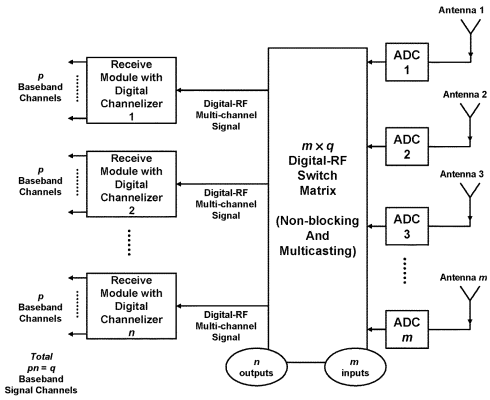

Fig. 1. The switch routes one or more of m digitized antenna outputs to each output port that is connected to a multi-channel receive module.

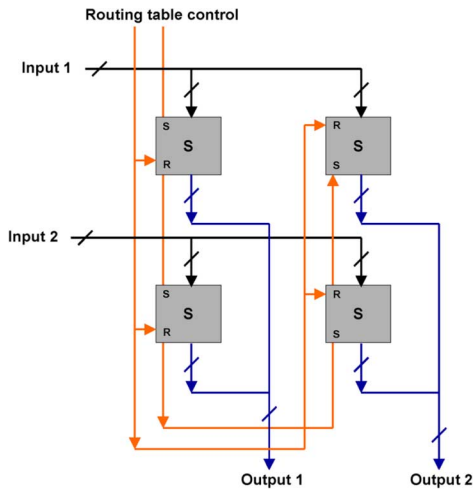

Fig. 2. Block diagram of the 2 × 2 2-bit switch matrix, comprising four 2-bit switch cells (S) and associated routing and control. The routing table is been loaded serially through a single data port.

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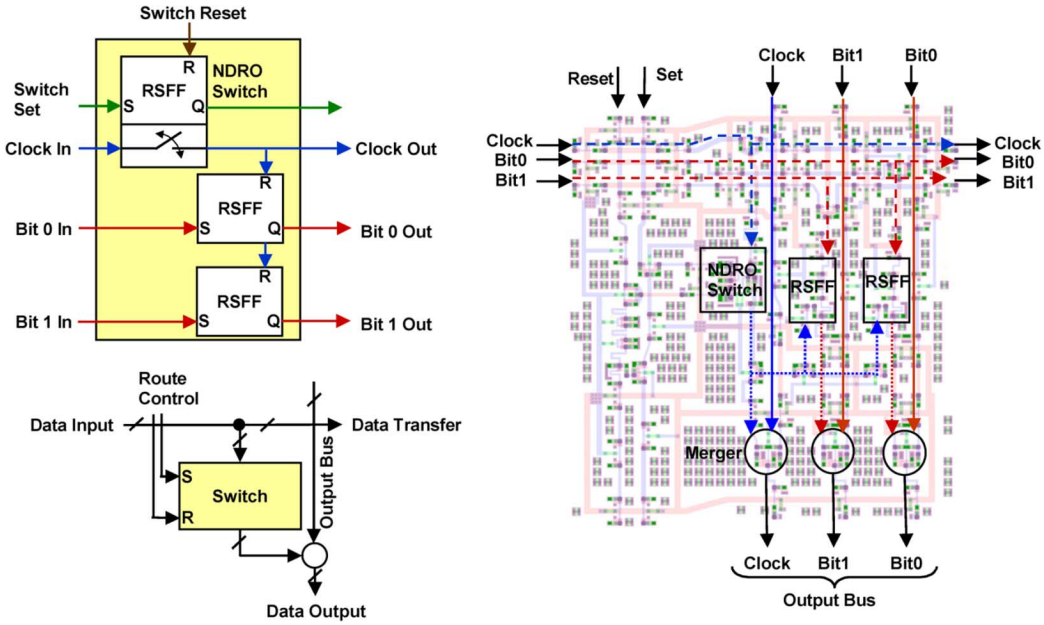

Fig. 3. Switch cell for 2-bit data stream. Block diagram (left) and the layout (right).

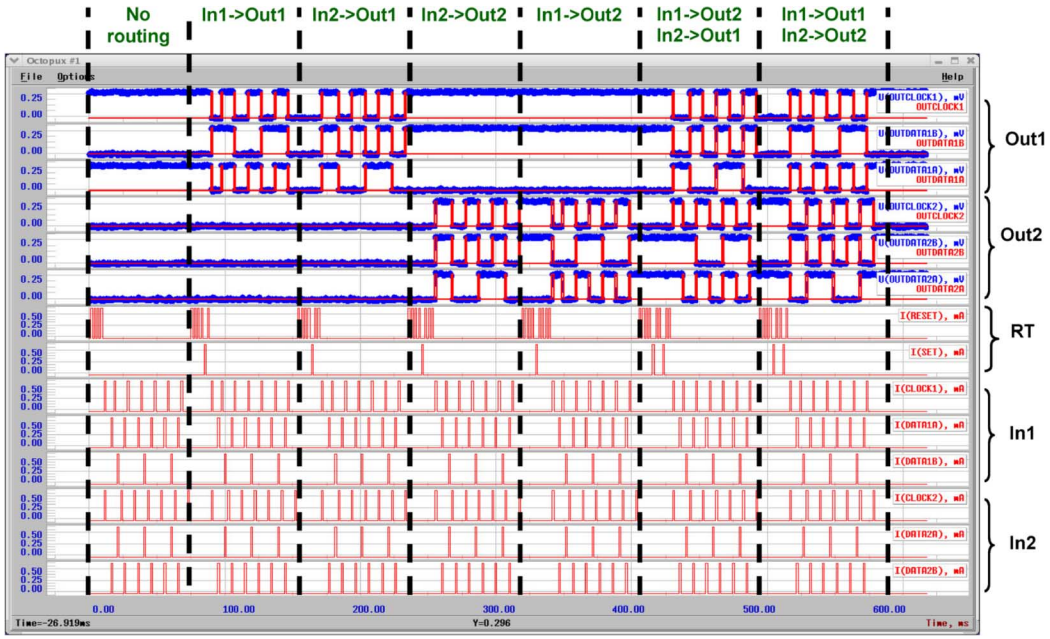

Fig. 4. Test results with a set of switch settings showing correct routing of input 1 and input 2 to output 1 and output 2 of the 2-bit 2 × 2 switch matrix chip. Each i/o port consists of three traces,—a clock (top trace) and two bit traces. The routing table is shown on the top of the pictre.

bits [1]. The size of a single switch node is $470\ \mu\mathrm{m} \times 540\ \mu\mathrm{m}$, mostly occupied by the relatively complex data bus wiring.

Although very simple, robust, and scalable, the suggested architecture is not suitable for the network switch implementation. It operates asynchronously and does not provide time-division mode, being prone to high skew. The most advanced network switch demonstration to date was performed by ISTEC NRL, Japan [2].

We have designed a single-bit switch matrix node for 1.0 $\mathrm{kA/cm^2}$ and 4.5 $\mathrm{kA/cm^2}$ standard HYPRES's fabrication process [3]. The switch was constructed from basic library cells and did not require extensive simulations.

B. *Functionality Test*

We have conducted low-speed functionality test of the switch with automated test setup Octopux [4]. Fig. 4 shows the correct routing of all possible combinations between two input and two output ports. In the picture, there are two groups of input and two of output traces. Each group consists of three traces,—a clock line and two bits. Two traces (clock and data) marked with RT is a serial routing table load.

The 2-bit 2 × 2 switch matrix functionality test has shown dc bias margins of 1.9–2.9 mV or ±20% at low speed. Remarkably, a single common power supply line has powered the whole switch matrix.

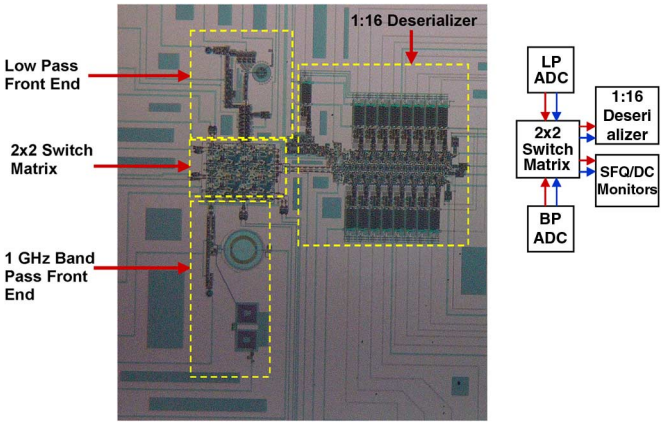

Fig. 5. The block diagram (right) and the photograph (left) of a chip containing two ADC (low-pass delta and L-band band-pass delta sigma) modulators, a 1-bit 2×2 switch matrix, and a 1:16 deserializer to lower data rate for room-temperature data interface.

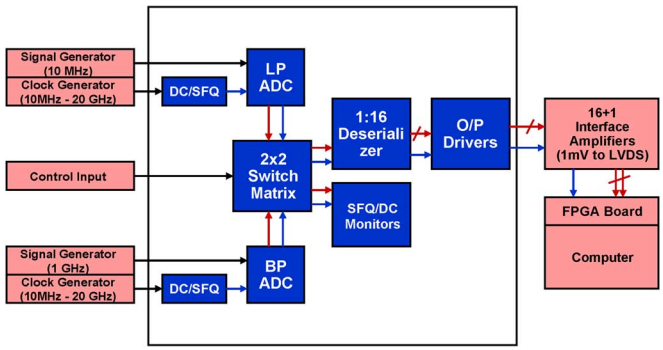

Fig. 6. Test configuration for dual-band ADC.

C. High-Speed Test

A stand-alone switch matrix cannot be easily verified at high clock speed. The best method is to use the switch matrix in its intended configuration by integrating it with ADC modulators to provide high-speed inputs and digital circuitry (digital filter, deserializer, etc.) at its output to facilitate testing with lower speed data acquisition and analysis equipment at room temperature [5].

We integrated two ADC modulators and a single deserializer (serial-to-parallel converter) with the switch matrix, all proven blocks from the HYPRES design library, in a 5-mm chip (Fig. 5). Fig. 6 shows the test configuration.

Both ADCs had previously been proven to work with the deserializer block on individual chips and the data acquisition system comprising a set of 17 high-speed digital amplifiers for boosting the signal to standard low-voltage differential signal (LVDS) logic levels and a commercial board with a Xilinx Virtex 4 FPGA chip connected to a computer [6].

Our goal was to connect inputs for RF signal and external clock to both the lowpass and the bandpass ADC [7], and by using a single control input to program the switch matrix, route the appropriate digitized RF data from the corresponding ADC to the data acquisition system. We successfully demonstrated operation up to a clock frequency of 16.384 GHz (see Fig. 7). This experiment has demonstrated correct operation of the switch at 10 GHz and proven validity of the concept. Yet, this is not a fully dual-band ADC; for the common data acquisition system does not allow operating both frontends simultaneously.

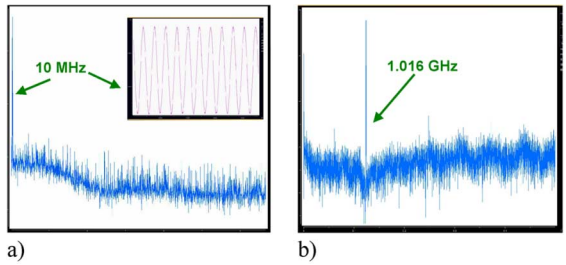

Fig. 7. Digital spectra of acquired input RF signals with 8.192 GHz clock frequency for (a) 10 MHz applied to the lowpass delta ADC, and (b) 1.016 GHz applied to the bandpass delta-sigma ADC respectively.

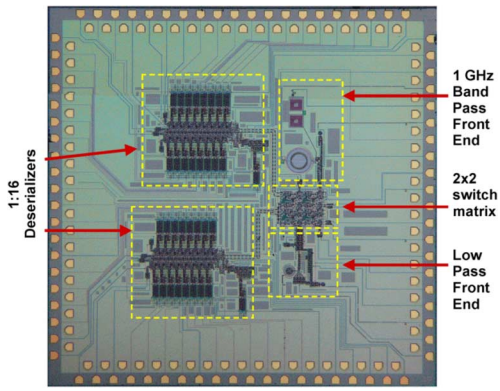

Fig. 8. The photograph of a 1-cm chip containing two ADC (lowpass delta and L-band bandpass delta sigma) modulators, a 2×2 switch matrix, and two 1:16 deserializers.

III. Multi-Band ADC

A 1-cm chip with two modulators and two 1:16 deserializers connected through the switch matrix is shown in Fig. 8. The chip shown in Fig. 8 is an extension of the one shown in Fig. 5; two deserializers are now attached to two output ports of the switch matrix, thus allowing simultaneous operation of both modulators.

For demonstrating simultaneous operation of modulators we used two interfaces described in Fig. 6. Instead of FPGA module, Agilent 16517 logic analyzer was used for postprocessing. The low-pass delta modulator was digitizing a 10-MHz signal with 8.0 GHz clock. At the same time, band-pass delta-sigma modulator was digitizing 852-MHz signal with 5.76 GHz clock. The result of this test is shown in Fig. 9.

Fig. 9(a) reveals an interesting detail. Besides the digitized 0.852 GHz signal, one can see two "parasitic" peaks at 2.556 GHz and 2.240 GHz. While the first one is obviously a third harmonic of the digitized signal, the second peak appeared to be related to the lowpass modulator clock. This is caused by poor RF isolation of the bandpass modulator input from the external (8 GHz) clock line to the lowpass modulator. The peak at 2.24 GHz is an aliased 8.0-GHz interferer sampled with bandpass modulator clock at a 5.76-GHz rate.

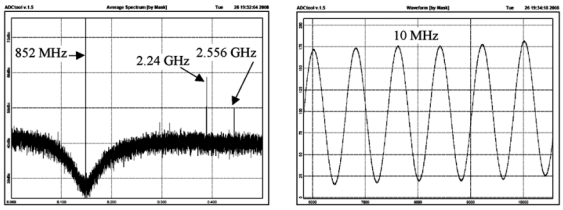

Fig. 9. Digital spectra of acquired input RF signals. (a) A 0.852 GHz signal has been applied to the bandpass delta-sigma ADC clocked at 5.76 GHz and (b) 10 MHz signal has been applied to the lowpass delta ADC clocked with 8.0 GHz clock.

IV. Conclusion

The switch matrix has been designed with a modular switch cell that allows scaling to arbitrary numbers of inputs and outputs to accommodate future multi-band, multi-channel digital receiver requirements. The design is asynchronous and permits routing of a data bus consisting of a set of bits along with their clock. The 2-bit 2×2 switch matrix was demonstrated with a single dc bias current line having $\pm 20\%$ operating margins. The switch matrix is capable of routing multi-bit data at rate of 40 GHz, although experimental set-up limitations have so far allowed validation up to 10 GHz. Two chips to demonstrate the concept of a multi-band digital-RF receiver, as well as to serve as a high-speed test platform for the switch matrix, have been designed. Each of these chips contained two different analog-to-digital converter modulators,—a lowpass delta modulator and a bandpass delta-sigma modulator. We demonstrated dual-band ADC operation with a digital switch matrix.

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