Flux Trapping Experiments in Single Flux Quantum Shift Registers

Raphael P. Robertazzi, Irfan Siddiqi, and O. Mukhanov
HYPRES, Inc., Elmsford, NY 10523

Abstract -- As the integration level of superconducting digital circuits increases, flux trapping in these devices becomes a serious problem. High resolution A/D converters and other high speed signal processing systems have been demonstrated with junction counts well into the 10^3 range. Such large circuits require special testing techniques to prevent flux trapping within the gates, which can reduce bias margins and cause malfunctions of these devices. We discuss the results of experiments using single flux quantum shift registers in which we have varied the ground plane hole pattern and magnetic shield degaussing procedure to minimize flux trapping in these circuits. The operating bias margins of the shift registers have been measured as a function of different testing procedures and ground plane hole designs. In situ degaussing of the magnetic shields aids in the reduction of flux trapping and gave the best results. Measurements of the permeability of mu metal at 4.2 K are discussed.

I. Introduction

In recent years remarkable progress has been made in the design, fabrication, and actual application of large scale digital superconducting circuits, including high resolution ADC's [1] digital SQUIDs [2], and superconducting memories [3]. Superconducting digital circuits invariably rely on dc SQUIDs to form the basic building blocks of storage, amplification, and logic elements. SQUIDs are inherently magnetically sensitive devices, so special precautions must be taken to ensure that magnetic flux trapped within large scale circuits will not cause them to malfunction. An external magnetic field present during the cooling of the superconducting chip through its transition temperature will trap flux within the circuit. Even a field as low as 1 mG will trap approximately 600 Φ_0 ($1\ \Phi_0 = 2.07 \times 10^{-15}$ Wb) in a 3.5 mm × 3.5 mm chip. For this reason protective ground plane holes and moats (elongated holes) have been employed by digital superconducting circuit designers to act as safe pinning sites for trapped flux. Although these structures have been used for years, very few quantitative studies have been done to judge their effectiveness.

Bermon [4] conducted a study of the protective properties of ground plane moats in reducing flux trapping in three junction SQUIDs. These devices were used in basic logic elements of the IBM Josephson computer program which was active in the mid 1970's. The Josephson junctions in the SQUIDs were coupled with inductors which employed central ground plane holes, and consequently were strongly coupled to local magnetic fields. In these experiments Bermon found that moats were able to protect the SQUIDs from trapping flux in ambient fields of up to several mG, although there was no report of how well these flux traps worked on improving the performance of digital circuits with many gates. Jeffery [5] used a scanning SQUID microscope to image the flux state of single MVTL digital gates. This study concluded that moats were more effective than patterns of small holes in protecting the circuits from flux penetration, but the circuits were not biased and were not tested, so no quantitative assessment of the effect of different ground plane hole patterns on the margins and operation of the circuits was made. In this study we report the results of bias margin measurements of 48 bit shift registers which were cooled through their transition temperature in magnetic fields of varying intensities. The shift registers were designed with five different configurations of ground plane hole patterns: (I) small holes interspersed within the cell, (II) two moats per cell, (III) one moat per cell, (IV) very large moats 30 microns away from the circuitry and surrounding the shift registers, and (V) no ground plane holes. In addition, the efficacy of different shielding and degaussing techniques on the reduction of flux trapping within the circuits was also explored.

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II. Shielding Technique

We performed all measurements in a model BCP-2 cryoprobe manufactured by American Cryoprobe, Inc. [6]. The probe was equipped with 2 concentric cylindrical mu metal cans and matching lids. The inner can had dimensions 14 cm × 2.87 cm o.d. × 0.076 cm wall thickness. The outer can had dimensions 15.2 cm × 3.2 cm o.d. × 0.076 cm wall thickness. Both cans were fabricated from AD-MU-78 mu metal alloy, a proprietary material provided by Advance Magnetics Inc. [7]. The shielded probe was tested in a shielded He storage dewar, so a total of three shields were employed during testing unless otherwise noted. The inner shield was wound with a Cu coil (19 turns/cm) which allowed it to be degaussed in situ while the outer can was mounted around it. In this way the degauss of the inner shield took place in the low field environment provided by the outer shield. We define this as the in situ degaus procedure, and discuss it more in section III.

The shielding factor g of a cylindrical shield c permeability μ may be calculated for a uniform fiel assuming that the direction of the applied magnetic field perpendicular to the axis of the cylinder, and that the ratio cylinder length to diameter is large (infinite cylind approximation). The shielding factor is defined as the rat of the magnitude of the magnetic field far from the cylind

to the magnitude of the field at the center of the cylinder. For a single infinite cylinder of inner radius a and outer radius b, the shielding factor g is given by the following formula [8].

$$g = \frac{1}{4}\frac{(\mu - 1)^2}{\mu}\left(1 - \left(\frac{a}{b}\right)^2\right) \qquad (1)$$

We measured the shielding factor of the inner can of our cryogenic test probe as a function of magnetic field applied parallel to the axis of the cylinder. A solenoid was used to apply the magnetic field, and a dc SQUID was used to read out the magnitude of the field inside of the cylinder. The shielding factor was measured as a function of applied field for magnetic field strengths near the center of the solenoid (without the shield mounted) from zero to 100 Oe. The effective permeability of the inner shield as a function of field was then deduced by inverting (1). Fig. 1 shows the results of these measurements. The initial permeability of the shield was 6300.

Using this result we calculate that the triple shielding arrangement used in the flux trapping experiments should yield a shielding factor of more than 325,000. Assuming a 1 G ambient from the earth's field, the field in the cryoprobe would be approximately 3 μG. In fact, measurements using arrays of washer SQUIDs indicate that the ambient was on the order of 100 μG using an optimal in situ degauss. The discrepancy between calculated and measured ambients may be due to an incomplete degaussing of the inner shield or some magnetic contamination of our sample holder.

Although the imposed solenoidal field was perpendicular to the direction for which (1) was derived, we feel that this analysis is justified because the shield was almost completely closed on all sides. (There were some holes in the lid for the cryoprobe wiring, but the diameter of these holes was much smaller than the shield diameter.) Magnetic shield designers have empirically found that (1) gives an accurate approximation to the shielding factor for a closed cylinder with a large length to diameter ratio, for axial distances inside the shield at least one diameter away from the end caps [9].

III. EXPERIMENTAL PROCEDURE

We designed 5 versions of a 48 bit Rapid Single Flux Quantum (RSFQ) shift register which were identical with the exception of the ground plane hole patterns in each design. The circuits were fabricated using our standard Nb foundry process. The shift register cell used a refined 6 Josephson junction design which has simulated bias margins of ± 40 % and current density margins of ± 30 %, similar to the circuit described in [10]. The shift registers were equipped with standard dc/SFQ converters on the inputs and SFQ/dc converters on the outputs. There was only one common bias for each circuit. Bias margins for a circuit are quoted as a percentage over which the optimal bias current could be

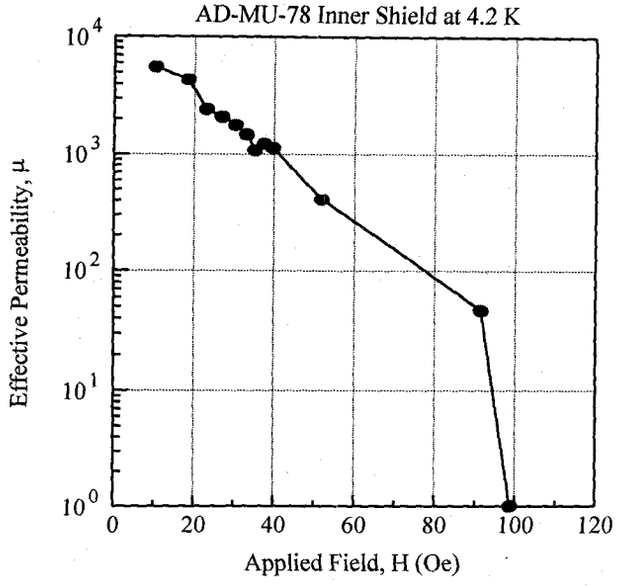

Fig. 1. Effective permeability vs. magnetic field strength deduced from dc shielding factor measurements for AD-MU-78 inner shield at 4.2 K. The data shows that the initial permeability (at zero applied field) is 6300.

increased or decreased with the circuit still operating correctly. Each chip used for comparison experiments contained four shift registers, two with no ground plane hole pattern (this device acted as a control) and two which contained a ground plane hole pattern as described in the introduction. A chip used to judge the effectiveness of the in situ degauss technique contained 3 shift registers without ground plane holes. In addition to the shift registers a square, single turn wire loop enclosed the central 3.5 mm × 3.5 mm area of the chip. The loop had a calculated inductance of 12 nH when the ground plane was not superconducting, and was used to introduce a predetermined amount of flux into the active circuit area of the chip while cooling.

In all of the bias margin experiments we performed rigorous, unambiguous testing of the shift registers. The test procedure was to load the shift register with a single flux quantum (test pattern 100...0) and then clock the device 48 times and observe the output. Any incorrect output pattern (for example, shifting by more or less than 48) was defined as incorrect operation of the device.

IV. DEGAUSS EXPERIMENTS

The first set of experiments was performed to determine the effectiveness of the shields as well as the in situ degauss procedure. In addition, the effect of leaving the inner shield with a nonzero magnetization on bias margins was also explored. In the first experiment, the shift register chip (containing 3 functioning devices and no ground plane holes) was loaded in the cryoprobe and tested without mounting the inner 2 magnetic shields. The bias margins were measured for each of the three shift registers, and these measurements

were repeated 4 times. This experiment yielded an average bias margin of ± 19 %.

In the second experiment, we mounted the two inner shields after using a commercial degaussing coil to degauss them, and repeated the bias margin measurements. We define this procedure as ex situ degaussing. Using this technique we obtained an average bias margin of ± 28 %. In the third experiment, we repeated the above except that now the inner shield was additionally degaussed in situ. We applied an exponentially damped sinusoidal current through the coil surrounding the inner shield. The maximum amplitude of the current was 7 A, with a 5 Hz drive frequency and a decay time constant of approximately 60 seconds. The maximum applied magnetic field strength, estimated to be greater than 200 Oe, should have been sufficient to saturate the shield at room temperature. The result of this third experiment was an average bias margin of ± 28.5 %.

We found these results rather surprising, in light of the fact that the in situ procedure has been demonstrated to provide a lower magnetic environment than the ex situ procedure, based on measurements of the threshold shifts of 100 SQUID array chips. Apparently at the level of complexity of the 48 bit shift registers both techniques are adequate although there was a measurable difference in bias margins when the two inner shields were removed. It should be pointed out, however, that the cooling rate of the cryoprobe is of critical importance in the amount of flux trapping induced in the circuits. This is because the greater the cooling rate, the larger the transient thermally induced electrical currents near the chip, and in general the more flux is trapped in the circuits. These currents flow when a thermal gradient exists between dissimilar metals in contact in the cryoprobe. With the shields removed we speculate that the average cooling rate of the cryoprobe tip was faster, hence an unambiguous comparison between experiments with and without shields is difficult to make.

We investigated the effect of leaving the inner shield with a small magnetic moment, by following the in situ degauss procedure with the momentary application of a dc current to the coil around the inner shield. We summarize the results of this set of experiments in Fig. 2. Small remnant magnetizations had little effect on bias margins until a critical value was reached, after which margins deteriorated rapidly and finally no operation was observed. The typical offset current of our in situ degaussing unit was less than 0.1 mA, approximately 400 times smaller than the current required to reduce the bias margins by a measurable amount.

IV. GROUND PLANE HOLE EXPERIMENTS

The second set of experiments was performed to determine if a measurable difference in protection could be discerned between ground plane hole patterns of various types. In these experiments the cryoprobe was equipped with both magnetic shields and degaussed in situ. Current was applied to the wire loop on chip surrounding the circuitry,

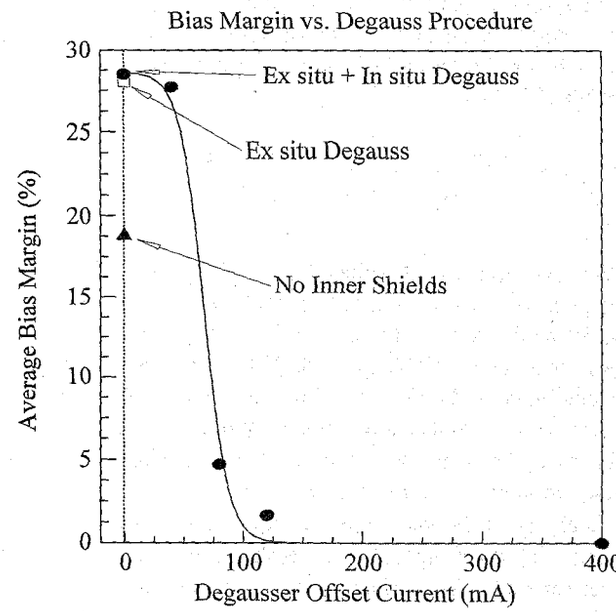

Fig. 2 Average bias margin for the control (no hole) shift register design as a function of shielding technique and degausser offset current.

introducing a known quantity of flux into the chip. The chip was cooled by lowering the cryoprobe slowly into the He bath, freezing the flux into the chip. The bias margins of the shift registers with holes were measured, and compared to the devices without holes on the same chip. For each chip we repeated these measurements three times. For each experiment, the cryoprobe was lifted out of the He bath and then recooled

Fig. 3 shows the data obtained from one shift register of type (III). This device had one moat per cell located near the clock line. Each symbol on the graph represents one deflux/bias margin measurement. Plots for each shift register measured were made and the data was sorted into four categories, as follows. ***1. Normal Operation:*** In this regime the shift registers operated normally with either full or slightly reduced margin. ***2. Reduced Margin:*** The shift registers operated correctly, but with significantly reduced margin. ***3. Incorrect Operation:*** The shift register output was incorrect, in either the output data pattern or the shift of the input. ***4. No Operation:*** The shift registers produced no output. In general, we observed that all shift registers had qualitatively similar operation modes as the amount of flux introduced during cool down increased. For small amounts of flux, no reduction in margins was observed. As the amount of flux increased, margins deteriorated rapidly at a critical flux density which depended on the ground plane hole pattern. For flux densities larger than this critical value no operation was observed.

A summary of the behavior of the four types of shift register layouts is shown in Fig 4. In this graph, each pair of bars represents data taken from at least one chip of each of the four kinds. The bar marked with (*) in each

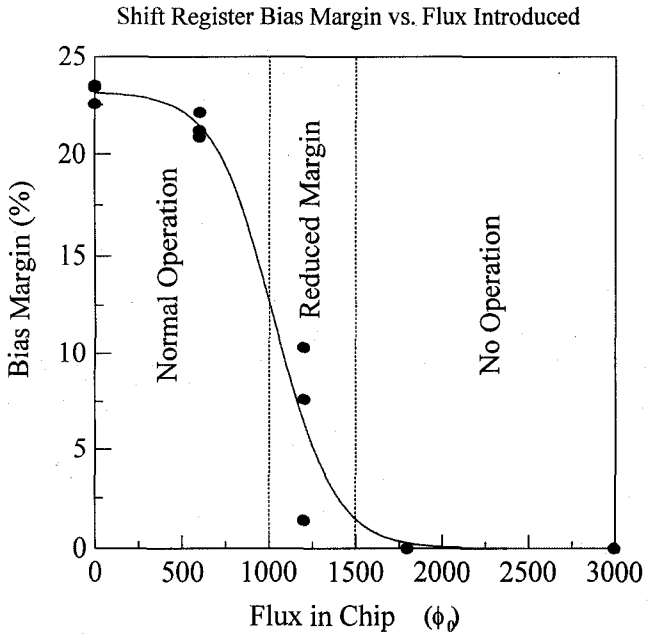

Fig. 3. Shift register bias margin vs. flux trapped in the chip for a shift register of design type III. The modes of operation which were observed for this circuit are indicated in the graph.

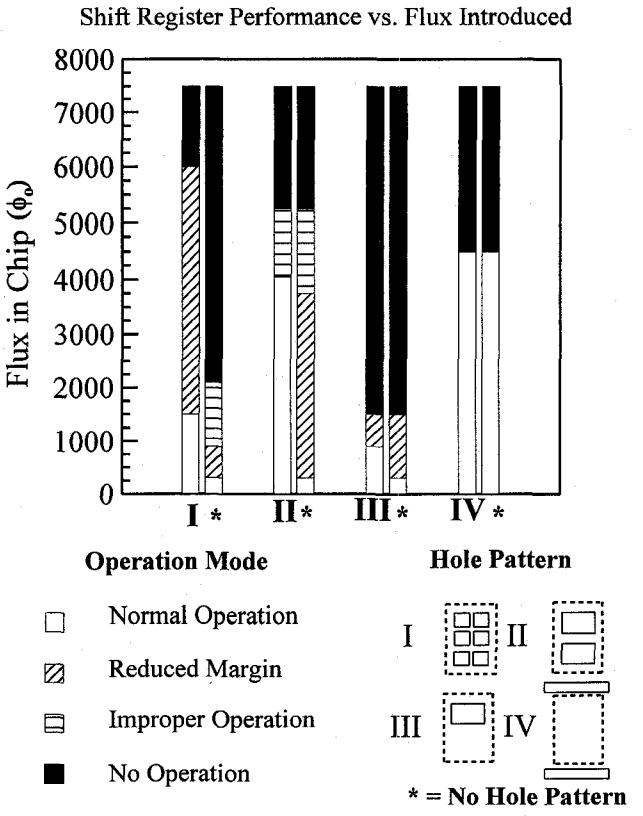

Fig. 4. Summary of shift register flux trapping experiments. In the legend, the shift register cell is indicated by the dotted line. The ground plane hole patterns are indicated by the solid rectangles. The data demonstrates that large moats were the most effective in preventing flux trapping, even protect the control shift registers. A field of 1 mG corresponds to 600 Φ_0 in the chip.

case represents the control shift registers (no holes). The legend schematically indicates the ground plane hole pattern. The large dotted rectangle in each picture represents an outline of the shift register cell. As can be seen from the data, the shift registers equipped with either small holes or moats were much better protected than the control shift registers. It is clear from the data that large moats (II) protected better than a pattern of small holes (I). In pattern (III) one moat was deleted from an area near the storage element of the shift register cell. It is evident that this moat is important in keeping flux away from this critical device area, as this design offered the least protection of all of the devices with holes or moats. Surprisingly, the best results were obtained with design (IV), which was simply a single large moat approximately 3000 μm long and 50 μm wide surrounding the shift register on three sides. We confirmed this data by measuring a second chip. The moats provided protection for both the shift register it surrounded as well as the control device.

V. CONCLUSIONS

From our experiments in this study as well as our extensive experience at HYPRES in testing complex digital superconducting circuits, we conclude that in situ degaussing aids significantly in reducing the ambient magnetic field in our double shielded probe. In general, the larger and more numerous the ground plane hole pattern, the better the protection from flux trapping. Large moats proved to be the most effective even though they were placed a considerable distance away from the circuitry.

REFERENCES

[1] S. V. Rylov and R. P. Robertazzi, "Superconducting high resolution A/D converter based on phase modulation and multichannel timing arbitration" *IEEE Trans. on Appl. Supercond.* **5**, pp. 2260-2263, June 1995.

[2] M. Radparvar and S. Rylov, "An integrated digital SQUID Magnetometer with high sensitivity input," *IEEE Trans. on Applied Supercond.*, **5**, 2142-2145, June 1995.

[3] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, "A 380 ps, 9.5 mW Josephson 4-Kbit RAM operated at high bit yield", *IEEE Trans. on Appl. Supercond.* **5**, pp. 2447-2452, June 1995.

[4] S. Bermon and T. Gheewala, "Moat guarded Josephson SQUIDs" *IEEE Trans. on Magn.*, **19**, page 1160-1164, May 1983.

[5] M. Jeffery, T. Van Duzer, and J. R. Kirtley, "Magnetic imaging of moat guarded superconducting electronic circuits", *Appl. Phys. Lett.*, **67**, page 1769-1771, 1995.

[6] American Cryoprobe, 5323 347th PL. SE, Fall City, WA 98024.

[7] Advance Magnetics, 625 Monroe St., Rochester IN 46975.

[8] A. P. Willis, "On the magnetic shielding effect of trilamellar spherical and cylindrical shells", *Phys. Rev.*, **4**, page 193-213, 1899.

[9] W. G. Gustafson, "Magnetic shielding of transformers at Audio frequencies", *Bell Sys. Tech. J.* , **17**, page 416-437.

[10] O. Mukhanov, S. Rylov, D. Gaidarenko, N. Dubash, and V. Borzenets "*Josephson output interfaces for RSFQ circuits*", submitted to Appl. Supercond. Conference, Pittsburgh, August 1996.