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Rapid single flux quantum technology for SQUID applications

O.A. Mukhanov*, S. Sarwana, D. Gupta, A.F. Kirichenko, S.V. Rylov¹

HYPRES, Inc., 175 Clearbrook Rd., Elmsford, NY 10523, USA

Abstract

The rapid single flux quantum (RSFQ) mixed-signal technology offers a way to enhance performance and reduce complexity and cost of SQUID systems. Ultra-sensitive analog SQUID front ends can be combined with low-power and ultra-fast RSFQ digital circuits on a single chip to form mixed-signal circuits combining the sensitivity and noise level of an “analog SQUID” and the increased slew-rate, dynamic range, linearity, and simple multi-channel readout electronics of digital RSFQ circuits. We have developed several RSFQ-based circuits to perform sensing, digitization, and timing of various weak signals including outputs of detector arrays. The key enabling factor for the implementation of all these SQUID-RSFQ circuits is the availability of a high-yield, low-noise fabrication process. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

Since its invention in 1985 [1], rapid (or resistive until 1987 [2]) single flux quantum (RSFQ) logic family has been dominant superconductive digital technology. No other digital technology can offer sub-terabit-per-second throughput while maintaining sub- μ W or potentially sub-nW power dissipation per logic gate. Such unique advantages should impact a wide variety of applications ranging from high-performance computing engines [3] to high-fidelity digital receivers [4]. However, practical insertion of such comparably large-integration-scale applications would require

an advanced manufacturable fabrication process with sub-micron lithography, which is not available to date. For small-integration-scale applications, there were several attempts to develop digital SQUID circuits. However, these digital SQUIDs were either too complex [5] for today's fabrication process or did not use the speed advantage of RSFQ technology (e.g. Refs. [6,7]).

We have identified medium-integration-scale applications (below 1000 Josephson junctions (JJs) per chip), which are suitable for a high-yield production using existing fabrication process [8]. These applications are digital readout circuits. For example, they can be used in place of analog SQUIDs to read out superconducting tunnel junctions (STJ) X-ray detector arrays and directly digitize their output pulses or time of their arrival. Other applications include readout of SIS mixers where no analog SQUIDs could be used due to high-bandwidth requirements. In this paper, we

* Corresponding author.

E-mail address: mukhanov@hypres.com (O.A. Mukhanov).

¹ Present address: IBM Research Center, Yorktown Heights, NY, USA.

present these two medium-complexity digitizer examples and describe their designs and results of experimental evaluations.

2. STJ detector readout digitizer

A typical STJ detector produces an output signal of about 1 μA peak and 5 μs duration in response to a 6 keV X-ray irradiation [9]. An objective for a readout digitizer is to obtain resolution of 1 eV. For some X-ray detector applications, the time of arrival of STJ pulses is also important. We have been developing an STJ readout digitizer capable of digitizing either signal or time of its arrival (Fig. 1). The digitizer consists of a sensitive front-end quantizer based on a dc SQUID followed by an RSFQ binary counter with parallel readout, serial memory buffer, parallel-to-serial converter, and output driver. A separate input for reference clock is used for the time-to-digital conversion (TDC). Depending of the desired function, either the sensitive quantizer or the reference clock input is connected to the binary counter using a dc current-controlled switch. Fig. 2 shows the layout of this signal/time digitizer fabricated using standard HYPRES fabrication process with 1 kA/cm^2 [8]. We designed the full-scale range of the input quantizer to be 1 μA , followed by a 15 bit binary counter. The chip comprises about 700 JJs and dissipates 0.25 mW. Power dissipation can be further reduced by scaling down bias resistors.

In signal digitization mode, the input sensitive quantizer is connected to the counter. An STJ produces a current pulse, which is magnetically coupled into this quantizer (dc SQUID) to produce voltage. This voltage is proportional to an SFQ pulse train frequency (pulse rate) generated at the output of this quantizer. The RSFQ binary counter counts number of these SFQ pulses over a certain counting time period.

In order to verify the designed voltage-to-frequency ratio of the input quantizer, we tested it in an analog mode as a stand-alone device and also in analog-to-digital conversion mode by applying a constant input current and reading out corresponding value of the digital binary counter. Fig. 3

shows reconstructed $V-\Phi$ curves using digitization over 200 ns counting period. We varied the constant applied current to trace these curves. The measured data fully corresponds to the analog measurement data confirming the correct operation of the digitizer for dc signals.

We also tested the digitizer for current pulses applied within the counting period. Here the output count represents the total charge of the pulse. Fig. 4 shows the digitizer output for three different pulse amplitudes each for five different pulse widths. The results show the excellent agreement with the theory. The linear curve fits through the count outputs for the same amplitude and different widths is also shown. This test confirms the ability to digitize the charge of a pulse.

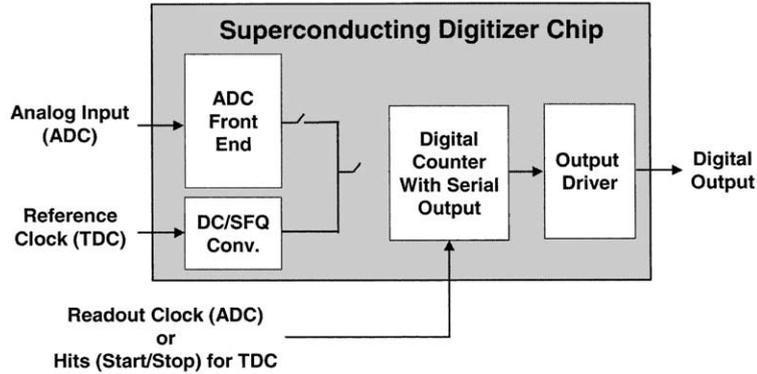
In time digitization mode, the reference clock input is connected to the counter. An STJ output signal is applied to Hit input. As one can see, now our digitizer becomes identical to TDC circuits which described in detail elsewhere [10]. For this particular chip, we performed successful time digitizer operation up to 10 GHz reference clock providing a 100 ps time resolution over 1.6 μs .

3. SIS mixer readout digitizer

For high-bandwidth readout applications such as SIS mixer readout, we have developed a novel digitizer architecture based on signal-to-delay transducing. The input signal is applied to analog front end, which converts this signal to the delay of the outgoing pulse triggered by the clock signal (Fig. 5). The delay is then digitized using three independent race arbiters with individually adjustable delays (timing thresholds). This architecture takes direct advantage of the ability of RSFQ logic devices to amplify (and fan out) SFQ pulses at very high frequencies (up to 100 GHz), and eliminates the need to use three individual signal-to-delay converters with associated signal splitting network.

Fig. 6 shows a block diagram of the signal-to-delay converter. The clock signal, which initiates the process of generating a pulse with signal-dependent delay is split at the input in four ways, so it produces four clock signals A_1 to A_4 with

(a)



(b)

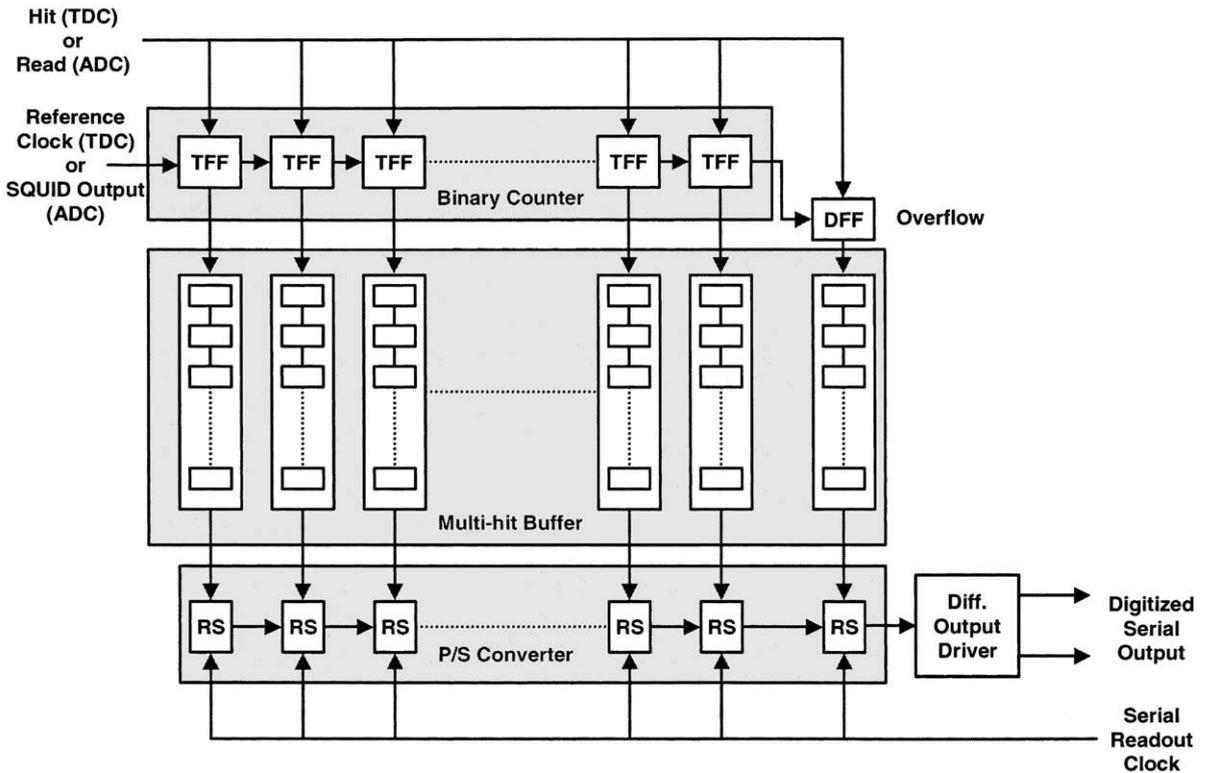


Fig. 1. (a) Block diagram of an STJ readout circuit that can perform either signal or time digitizer functions. (b) Block diagram of the RSFQ digital counter with memory buffer, a shift register, allows the time digitizer to store several time stamps between multiple input pulses. The parallel-to-serial converter reduces the number of outputs.

individually adjustable delays. The clock pulses A_1 and A_4 are recombined using an inductive merger. The circuit is designed in such a way that the output junction J_1 generates only one SFQ pulse.

This pulse is released somewhere in-between those individual clock pulses from A_1 to A_4 branches depending on the value of the input signal applied magnetically to the inductor L_1 . Fig. 7 shows this

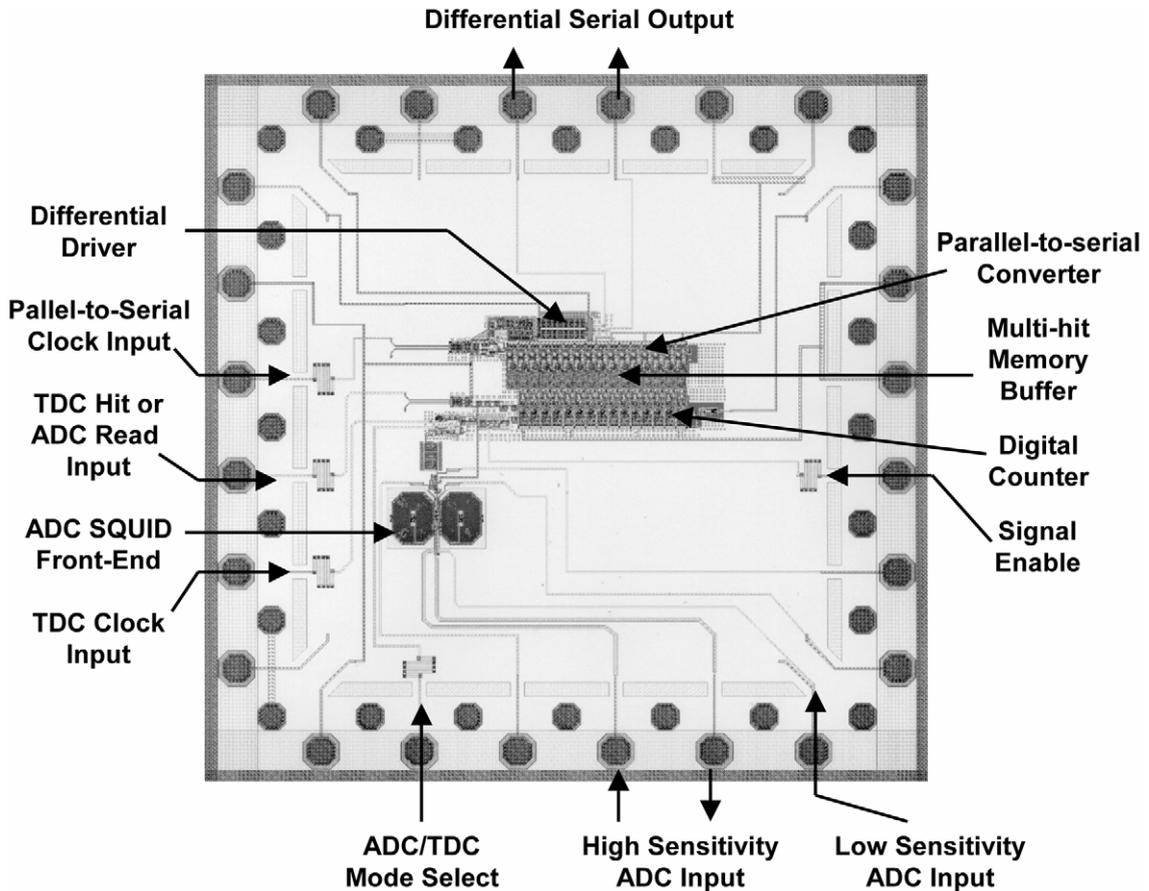
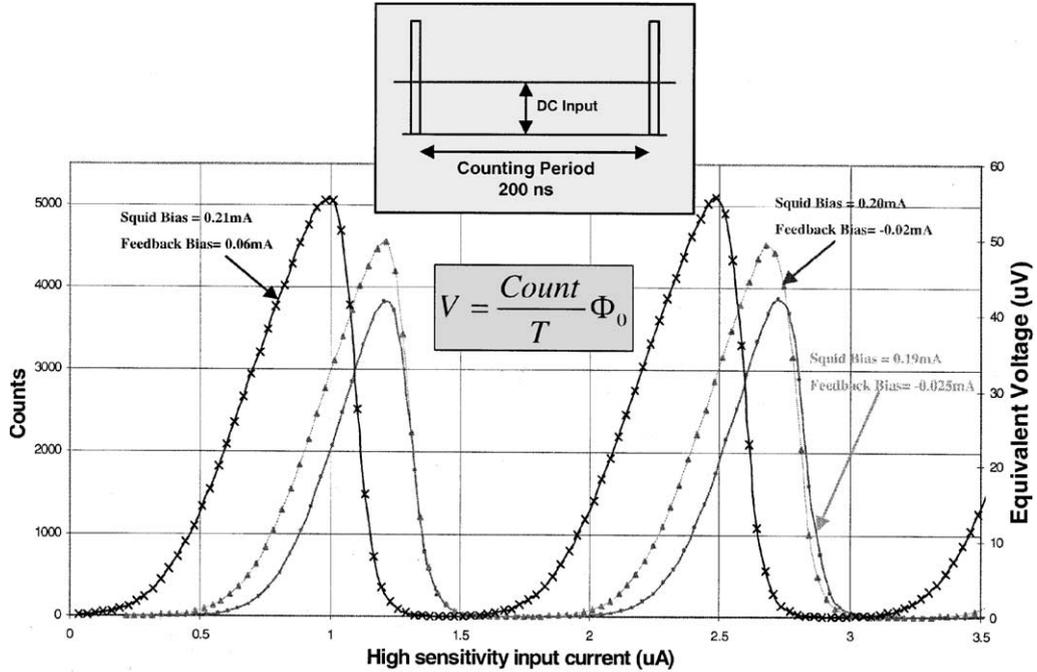


Fig. 2. Chip layout of the STJ readout digitizer ($5 \times 5 \text{ mm}^2$).

relationship between the input signal and the output pulse delay in a graphical form. The moment of the output pulse release is determined by crossing the plotted curve with a horizontal line representing a given value of the input signal. For instance, signal S_1 crosses the curve a half-way between the clock pulses A_1 and A_4 . Smaller input signal would cause the output pulse to be released earlier (closer to A_1), while larger signal will shift it closer to A_4 . In order to obtain a high-sensitivity comparator, the transducer is followed by a race arbiter device. In our design, we use for this purpose a so-called set-read-clear cell (SRC cell), which is a variation of a RSFQ logic B flip-flop [11]. It operates as follows: the cell periodically receives read signal and clear clock signals. If the

variable-delay signal arrives before the read signal, an output of “1” is generated, while if it arrives after the read signal, it would not be read out, but rather will be erased or cleared. In Fig. 7, the position of “read” signal is marked as point C , while the position of the clear signal is marked as B and B^* (the latter is clear signal of the next clock period). As one can see, by changing the position of the “read” timing threshold one can implement a signal comparator with a threshold position variable from point S_0 to S_2 , i.e. in a quite large dynamic range.

A photograph of a complete digitizer integrated circuit providing full implementation of the block diagram (Fig. 5) is shown in Fig. 8. The digitizer occupies a small portion of a HYPRES standard



- Counting period (T) = 200ns / Error bars not shown for clarity
- 14-bit digital word measured as counts

Fig. 3. Reconstructed $V-\Phi$ curves for three different SQUID bias values. The dc input to the primary coil of the transformer coupled to the front-end SQUID (high-sensitivity input) was varied and the number of SFQ pulses was counted in a 200 ns counting period. The counts are proportional to the SFQ pulse frequency that is proportional to the voltage across the dc SQUID.

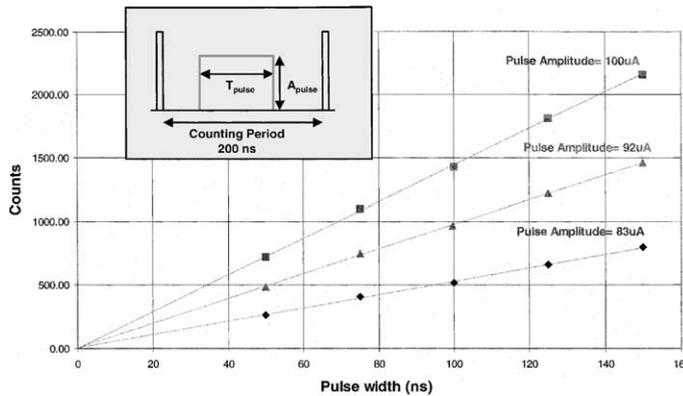


Fig. 4. The time integral of several current pulses of varying widths and amplitudes were digitized. The linear fits for each data set corresponding to three different pulse amplitudes (A_{pulse}) are shown.

$5 \times 5 \text{ mm}^2$ chip. It is implemented in HYPRES standard Nb technology with 1 kA/cm^2 critical current density [8].

Fig. 9a shows operation of the digitizer at high clock rate (10 GHz) with low-speed clock signal. The observed that amount of threshold noise

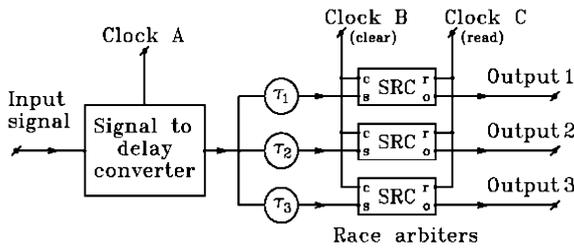


Fig. 5. Block diagram of a 2-bit signal digitizer for an SIS mixer readout based on signal-to-delay conversion and timing arbitration.

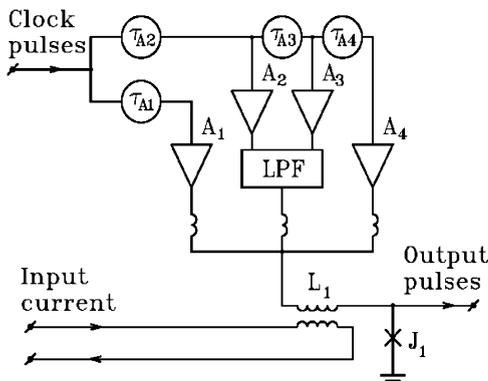


Fig. 6. Implementation of the digitizer front end based on a four-arm signal-to-delay transducer.

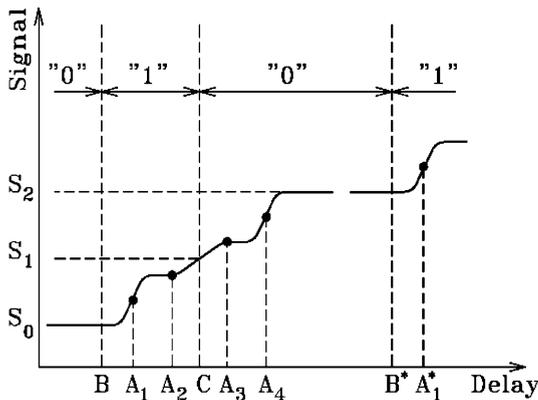


Fig. 7. Signal-to-delay conversion curves of the digitizer front end.

(which is about 1 μA in Fig. 9) does not change considerably from low-frequency clock up to about 10–11 GHz. At higher clock rates the noise

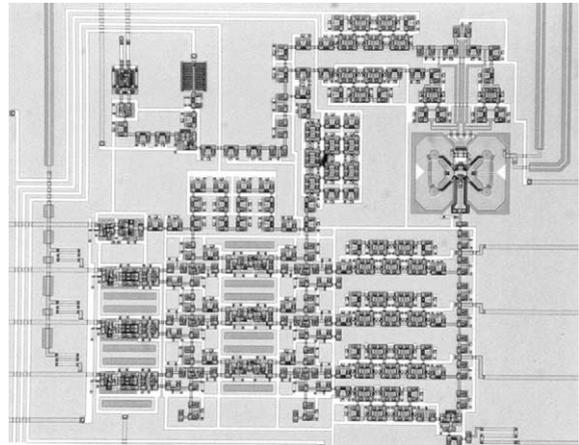


Fig. 8. Photograph of a 2-bit 10 GS/s RSFQ digitizer for SIS mixer readout. The chip size is $5 \times 5 \text{ mm}^2$. The area shown is $1.7 \times 1.3 \text{ mm}^2$.

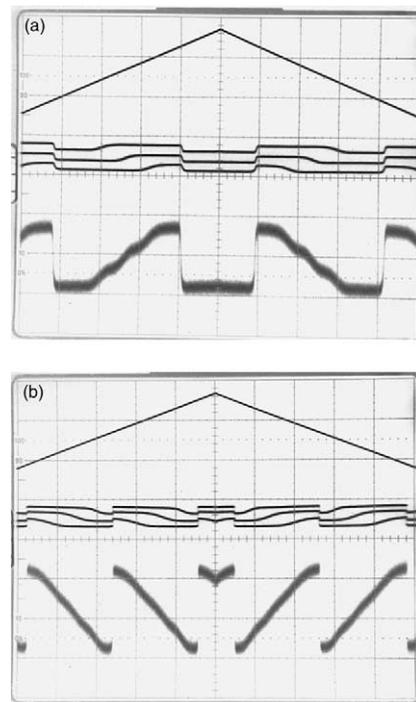


Fig. 9. Operation of the digitizer at high clock speed (a) 10 GHz, (b) 17 GHz and with low-speed input signal. Traces from top to bottom are input signal, three comparator outputs (0.2 mV each), output signal reconstruction from the on-chip digital-to-analog converter (0.2 mV). The digitizer sensitivity can be estimated from the circuit periodic response to the input signal: the period in this ADC is 8.6 μA . The noise at 10 GHz is about 1 μA , while at 17 GHz is about 3 μA .

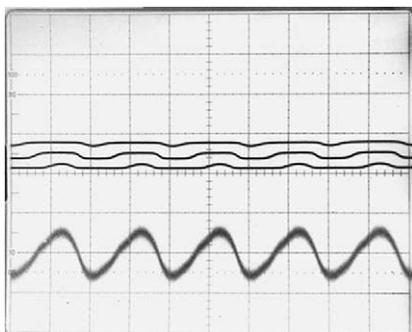


Fig. 10. Beat frequency test of a 2-bit digitizer at 10.000000 GHz clock and 10.000005 GHz signal. Upper traces—outputs of the three comparators (0.2 mV each), bottom trace—output of the on-chip DAC (0.2 mV). Period of output beat signal is 5 kHz. The signal amplitude is 2 μ A peak-to-peak.

performance gets progressively worse, for instance at 17 GHz clock (the highest clock frequency we had operated our digitizer) it approaches about 3 μ A (Fig. 9b).

It worth noting that the digitizer has the ability to achieve much better sensitivity under optimal conditions. It is seen that in Fig. 9, we have also sharp thresholds coinciding in all three comparators. The reason for their better noise is higher signal-to-delay conversion ratio (which is about two orders of magnitude higher near these thresholds). We measured that the threshold width can be reduced by this technique to 100 nA.

Fig. 10 shows the results of a beat frequency test of the digitizer at 10 GHz (both analog signal and clock). This test proves the ability of our digitizer to digitize high input bandwidth signals.

4. Conclusions

We have shown two possible applications for mid-complexity RSFQ readout digitizers. They can bring much greater functionality compared to traditional SQUID-based readouts placed in the nearest vicinity of sensors including e.g. STJs and SIS mixers. All these digitizers are built using a

combination of a sensitive front-end quantizer based on dc SQUID followed by high-speed digital RSFQ circuitry.

Compared to traditional analog SQUIDs, these digitizers require availability of a fabrication process capable of producing RSFQ chips with several hundreds of junctions integrated on a single chip. This integration level is well within capabilities of existing Nb fabrication foundries.

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