Superconductor Components for Direct Digital Synthesizer

Oleg Mukhanov, Amol Inamdar, Timur Filippov, Anubhav Sahu, Saad Sarwana, and Vasili Semenov

***Abstract*—We are developing a Direct Digital Synthesizer (DDS) based on a novel digital-to-analog converter (DAC) technology capable of directly generating wideband signals at RF with large signal-to-noise ratio (SNR) and spur-free dynamic range (SFDR). The key parts of this oversampling interpolating DAC are a digital interpolation filter (DIF), a digital sigma-delta modulator, a phase rotator, and an output amplifier array. We have developed first and second order DIF circuits to perform digital interpolation—accurate up-conversion of baseband data to RF (125 MS/s to 2 GS/s) followed by digital filtering using a Hogenauer Cascaded Integrator Comb filter. The digital sigma-delta modulator performs sigma-delta encoding of the interpolated data and comprises circuits similar to the DIF circuits. The phase rotator provides the phase information for the output amplifier array to create an analog waveform from a digital time-varying signal. The phase rotator provides the reference phases as four quadrature outputs. Depending on the digital input the rotator is capable of shifting phase by either one or two clock periods in any direction. The output driver is a differential digital amplifier based on SQUID arrays. It also can be assembled using voltage multipliers or superconducting quantum interference filters (SQIFs). Design and experimental results of these DDS components are presented and discussed.**

***Index Terms*—DAC, digital interpolation filter, output differential amplifier, phase rotator, RSFQ, transmitter.**

I. Introduction

HIGH-EFFICIENCY generation of spectrally pure, wide-band, multi-carrier waveforms is a key objective in modern communication and radar applications. This goal can be achieved by direct digital synthesis (DDS) of high-frequency RF waveforms with high bandwidth and linearity. Such a DDS would exclude non-linear, narrow-band, high-cost analog microwave components, implementing an essentially digital transmitter. It would allow one to combine digitally multiple waveforms and then directly synthesize the composite RF signal. Maintaining the digital nature of the generated RF signal all the way to the power amplifier (PA) would be enabled by the use of new highly efficient high-speed semiconductor digital amplifiers. It also would enable the implementation of digital predistortion at the RF level compensating for non-linearities of the amplifier chain. Such a Digital-RF architecture is made possible with the high speed and high linearity of superconductor RSFQ technology [1].

It is unlikely that semiconductor technologies can deliver the required performance. Commercial CMOS DDSs produce significantly lower bandwidth and require an analog up-conversion to high RF carriers. The most advanced DDS circuits today are based on the use of III-V compound semiconductor materials. While being targeted for GHz speed, these circuits are prone to excessive power dissipation, high cost, and an inability to combine high spurious-free dynamic range (SFDR) and low phase noise with generation of arbitrary waveforms.

To date, the development of superconductor-based digital-to-analog converters and waveform generators was focused mostly on low-frequency, high-accuracy metrology applications [2]–[4]. In contrast, we are developing transmit circuits for high-speed communication and radar applications. In this paper we report on the development of superconductor DDS components for a Digital-RF transmitter.

II. Architecture

Oversampling and digital filtering are the dominant techniques for superconductor analog-to-digital converters (ADCs) [5]. Similarly, these techniques can be successfully used for digital-to-analog converters (DACs). Low-speed baseband digital data are passed through a digital interpolation filter which generates the extra data points and effectively increases the sampling rate. This high oversampling rate moves image frequencies higher, simplifying output filters, and spreads the quantization noise over a wider band than the original signal bandwidth. This leads to an increase in the signal-to-noise ratio (SNR) within the signal bandwidth due to the processing gain.

A basic block diagram of our DDS is shown in Fig. 1. It consists of semiconductor and superconductor parts. The heart of the system is a high-speed low-temperature superconductor (LTS) module enabling ultra-linear direct generation of wide-band RF waveforms. It takes a baseband modulated multi-bit digital signal produced by a commercial CMOS baseband waveform synthesizer and digitally oversamples and interpolates. The N-bit words of baseband data are received at a rate f_{CLK}, representing a signal bandwidth $f_S = f_{CLK}/2$. The digital interpolation filter (DIF) inserts the extra data points and is clocked with oversampling frequency $f_{OS} > f_{CLK}$. This results in moving signal images farther out of the band of interest ($f_{IMAGE} = f_{OS} - f_S > f_{CLK} - f_S$).

Digital sigma-delta modulator takes the 16-bit output of the DIF and encodes it into a sigma-delta digital stream. Four outputs are generated for the following equalizer. The digital equalizer performs a predistortion in order to compensate for lim-

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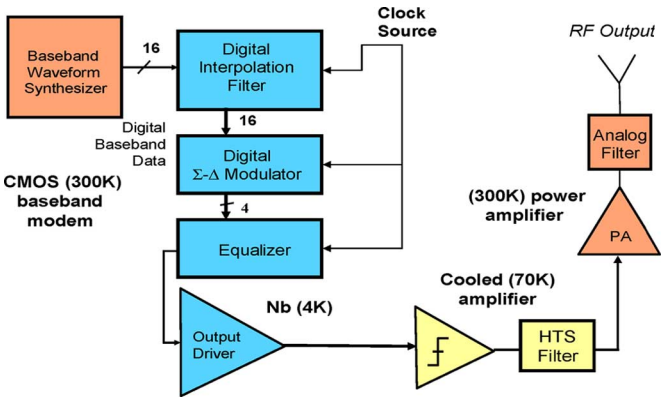


Fig. 1. DDS block diagram.

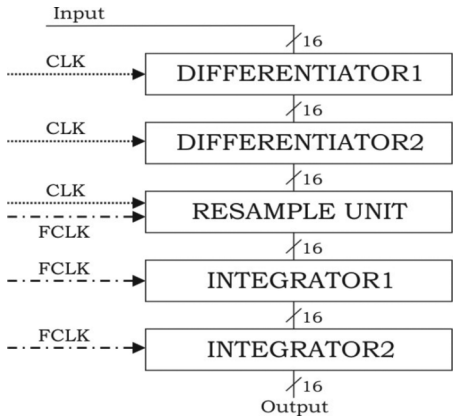


Fig. 2. Block diagram of digital interpolation filter (2nd order). CLK is 125 MHz, FCLK is 2 GHz.

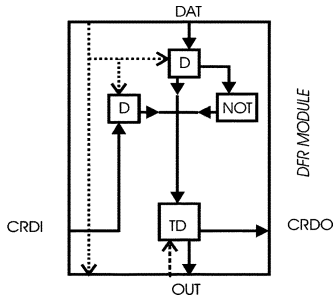


Fig. 3. Block diagram of a 1st order Digital Differentiator.

ited bandwidth of output lines and amplifiers. An equalization technique similar to one used in high-speed semiconductor digital links [6] is based on generation of a control signal of different phases applied to the output driver. The output driver (e.g., based on SQUID arrays) provides the first-step amplification. The output data is subsequently amplified using a cooled digital semiconductor amplifier and finally by a room-temperature semiconductor PA. The amplified signal is filtered using high quality analog filters.

III. DDS Components

In this paper, we focus on the superconductor part of the DDS consisting of the DIF and modulator, the equalizer, and the on-chip output driver.

A. Digital Interpolation Filter (DIF)

Digital interpolation provides for accurate up-conversion of baseband data (e.g., 125 MS/s) to RF (2 GS/s). It is then filtered using a Hogenauer Cascaded Integrator Comb (CIC) filter. There are four important reasons for choosing this filter design.

- — First, it has a recursive design with a small number of parts.
- — Second, in RSFQ technology, it is much easier to build filters using accumulators (flip-flops with internal gate memory) and inverters.
- — Third, the Hogenauer filter implementation is optimized for high-speed use.
- — Fourth, Hogenauer interpolation and decimation filters share many components. Therefore, the already developed decimation filter design [7] reduces risk and time for interpolation filter development.

The Hogenauer filter cell pair is an integrator/comb combination, implemented in RSFQ technology by an accumulator and differentiator (adder/inverter combination). These simple gates allow very high-speed operation when pipelined correctly. We have been building Hogenauer-type decimation digital filters for our oversampling ADCs.

There are two major differences between an *interpolation* filter and a *decimation* filter in the Hogenauer design:

- — In the interpolation filter, the comb part comes first, and the integrator sections follow. In the decimation filter, the comb and integrator order is reversed.
- — The interpolation filter up-samples data; data are down-sampled in the decimation filter.

A block diagram of the 2nd order DIF is shown in Fig. 2. The DIF is a massive but regular RSFQ structure. The first-order DIF consists of a differentiator, a resample unit and an integrator. The 2nd order DIF consists of two layers of differentiators and integrators. The differentiation is performed by summing up the current word and the inverted word from the previous clock period and storing the sum in a T-flip-flop with destructive read out (TD) in accordance with (1) as shown in Fig. 3.

$$z_k - z_{k-1} = z_k + \overline{z_{k-1}} + 1 \tag{1}$$

The resample unit is based on an RS flip-flop with nondestructive read out. The integrator is an accumulator circuit identical to one used in our digital decimation filters.

The differentiator cell was successfully implemented and integrated with the digital resample unit to form a bit slice. The main design issue of the DIF was to align timing between different clocks. We have designed and fabricated several test chips to optimize this timing (Fig. 4). Fig. 5 shows successful operation of the digital differentiator and the combination of the differentiator and resample unit. The 1st order differentiator circuit (top) performs an operation with the repeating input pattern {0,10,0,5} to calculate the periodic output pattern {10,11,7,4}. The integrated 1st order differentiator and resample unit (bottom) shows a single '1' applied to the 2nd bit input (DATA2) that triggers the corresponding output. The 1st slow clock (CLK) is followed by 8 fast clock pulses (FCLK) to insure the propagation of slow one along the circuit and demonstrate the resample function. The 2nd slow clock pulse triggers changes in the 3rd and 4th outputs (OUT3 and OUT4) that are read out by multiple fast clock pulses.

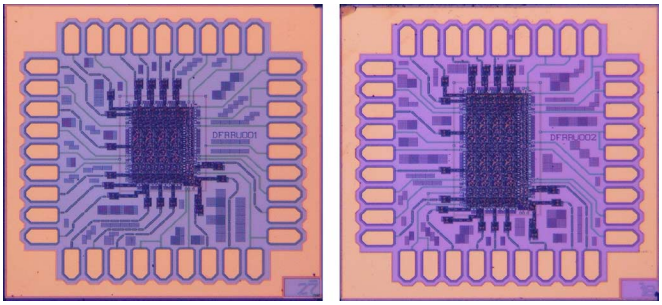


Fig. 4. Test chips with a 4 bit slice of a digital differentiator with resample unit. (left) 1st order circuit. (right) 2nd order circuit.

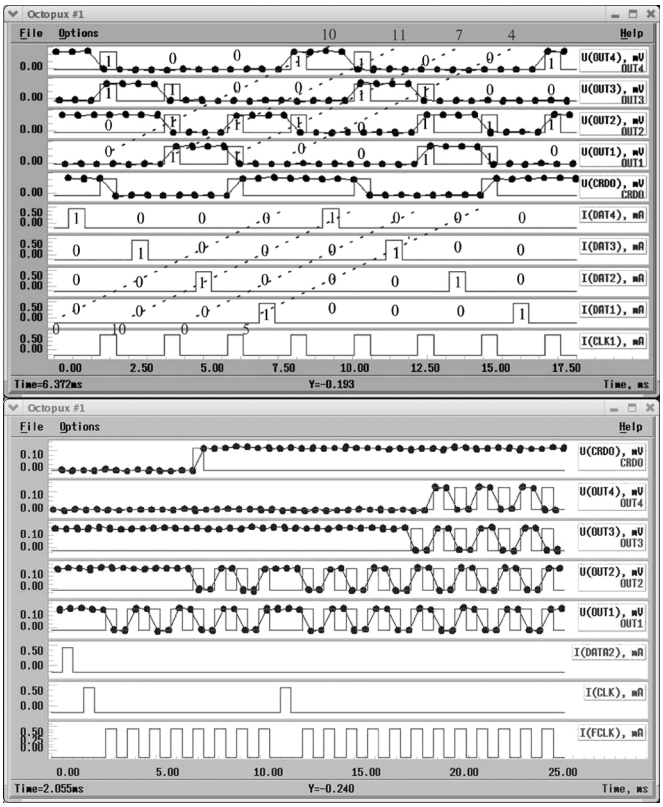


Fig. 5. Low-frequency test results of (top) 1st order differentiator and (bottom) combined differentiator and resample unit.

B. Digital Sigma-Delta Modulator

Fig. 6 shows the block diagram of the sigma-delta modulator designed for subsequent integration with the following digital equalizer. This 1st order design consists of the same differentiator and integrator elements developed for the DIF.

C. Equalizer—Phase Rotator

Often in digital communications, there is a need for equalization when high-speed digital data are to be transmitted through a lossy and/or limited bandwidth channel, which causes attenuation of the spectral components of the transmitted signal. These spectral distortions complicate detection of digital information from the received signal and may cause a finite bit error rate (BER). One such problem known as inter-symbol interference (ISI) is caused by difference in propagation delay for different spectral components through the channel. On the eye diagram ISI is manifested as horizontal eye closure, similar to jitter. One

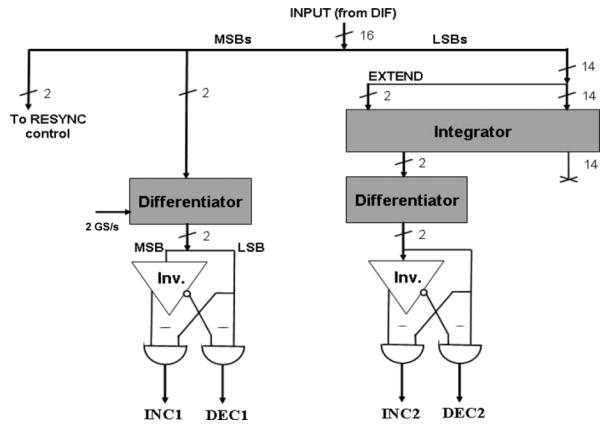


Fig. 6. Block diagram of digital sigma-delta modulator. The modulator comprises elements mostly used in the design of digital interpolation filter.

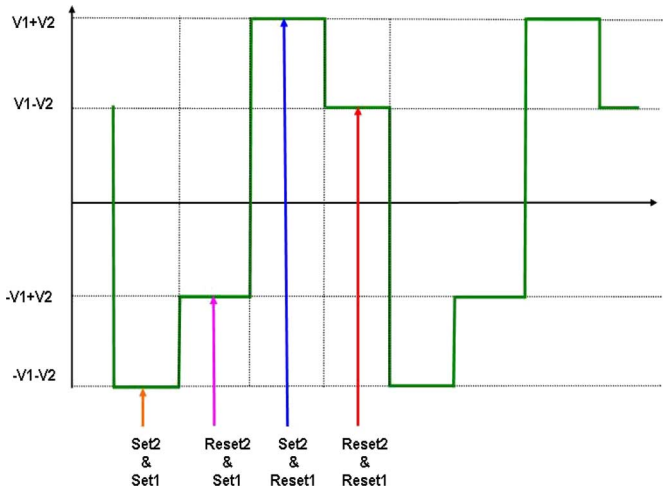


Fig. 7. A four level pre-distorted waveform to suppress inter symbol interference.

of the common techniques to reduce the ISI is to pre-distort the transmitted signal. Such pre-distortion, known as transmitter equalization, can be achieved by using a low-order FIR filter. The simplest FIR-based transmitter equalizer uses a two-tap FIR filter where the tap weights have opposite polarity: $\mathrm{y(i)} = (1-a)\mathrm{x(i)} - a\mathrm{x(i-1)}$, and '$a$' is a filter parameter. The net effect of such an equalizer is to attenuate the low-frequency components of the transmitted signal by $(1-2a)$ with respect to the highest-frequency pattern (010101). By choosing an optimum value of parameter 'a', it is possible to achieve nearly complete ISI suppression in a first-order channel. In practical terms this means creating a four-level waveform, such that for any high frequency change (0 to 1 or 1 to 0) an additional gain (peak) is added to the output waveform. Fig. 7 shows the desired pre-distorted waveform.

In order to generate such a pre-distorted waveform, we implement a novel waveform generation scheme that comprises a phase rotator, which drives an output amplifier (e.g., based on a SQUID stack). Fig. 8 shows the block diagram of this scheme.

The phase rotator is an integral part of the DDS and provides the phase and magnitude information for the DAC to create an analog waveform from a time-varying signal in digital form. The phase rotator employs a high resolution digital-to-phase

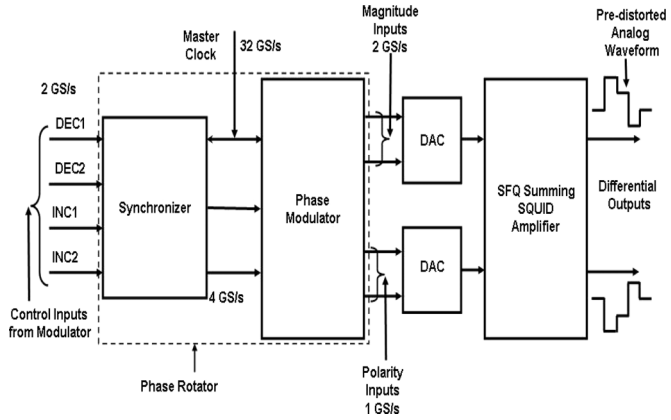


Fig. 8. Block diagram of the waveform generation scheme.

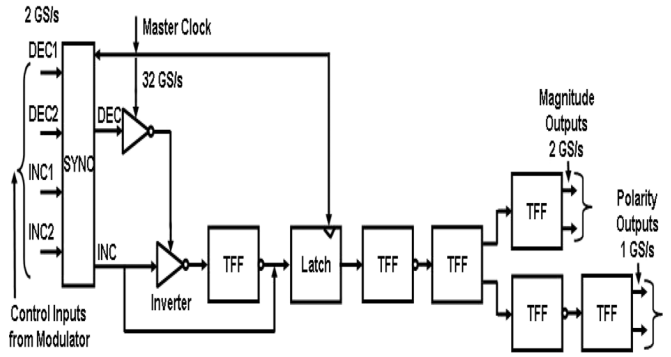
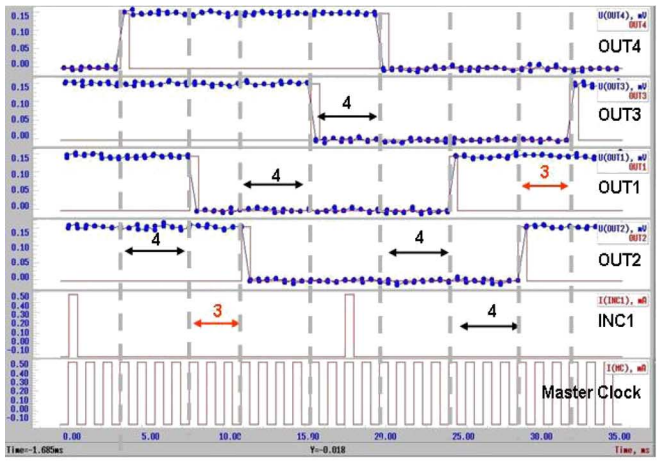


Fig. 9. Conceptual design of the phase modulator.

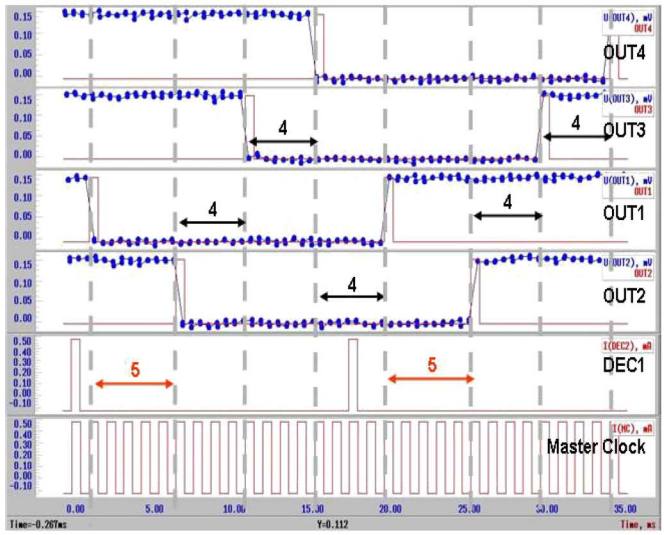
converter (or phase modulator), in order to finely locate every single edge of the output signal at the right instant in the time domain. The time resolution of the digital-to-phase converter directly determines the spectral purity of the produced output signal. In the semiconductor technology a phase rotator is routinely used in high-speed signaling circuits to generate precisely aligned clocks. In our implementation the transmitter equalization technique is also embedded in the phase rotator.

The outputs of the rotator are used to drive the DAC for waveform generation. In the absence of the control inputs from the sigma-delta modulator, the rotator provides four reference phases from its four outputs. Two of the outputs carry the magnitude information and are at a nominal frequency equal to the maximum permissible frequency of the control input. The remaining two outputs control the polarity and are at half the maximum permissible frequency of the control input. Depending on the control input, the rotator shifts the phase of the output pulse stream on every output channel, by either one or two clock periods in any direction. The increment inputs cause a negative phase shift shrinking the time period, whereas the decrement inputs cause a positive phase shift, increasing the time period.

To ensure extremely high accuracy, the phase rotator includes a synchronizer that synchronizes the low frequency control inputs to a very high frequency clock (see Fig. 9). The synchronizer consists of a chain of toggle flip-flops (TFF) to subdivide the master clock into its binary sub-harmonics. The control inputs are stored in a latch, clocked by the binary sub-harmonic of the master clock whose frequency is equal to the maximum permissible control input frequency. The two increment control inputs (INC1 and INC2) at a maximum rate of 2 GS/s are multiplexed on a single line to give a maximum rate of 4 GS/s. Similarly the



(a)



(b)

Fig. 10. Low-frequency test results for the Phase Rotator: (a) INC1 input applied. (b) DEC1 input applied.

decrement control inputs (DEC1 and DEC2) are multiplexed on a single line. The synchronizer also includes a cancellation circuit that cancels out increment and decrement pulses present in the same clock period. The control inputs are further successively re-latched and read by the higher subharmonic clock until they are finally read by the master clock itself and passed on to the phase modulator. Depending on these control inputs, the modulator either advances or retards the timing of the output pulse stream by one or two clock periods. An input signal of INC1 bypasses the first TFF to advance the timing of the output pulse stream by one clock period on all output channels. In case of both INC1 and INC2, the timing of the output pulse stream advances by two clock periods on all output channels. Similarly DEC1 causes the inverter to absorb one pulse and retards the timing of the pulse stream by one clock period, whereas both DEC1 and DEC2 retard the timing of the pulse stream by two clock periods. Thus the outputs shift phase by either one or two clock periods depending on which of the input signals are present.

In our design of the phase rotator, for ease of testing we eliminated the last toggle flip-flop on the polarity outputs, so as to have four outputs with the same nominal output frequency. The design was tested at low frequency using the Octopux automated test

Fig. 11. Frequency spectrum of the phase rotator output at 16.384 GHz master clock. The center spectrum represents absence of control inputs, whereas the right and left spectra are in the presence of increment and decrement inputs respectively.

setup (Fig. 10). Since the outputs are decimated by a factor of 16, an output appears on one of the four outputs every 4 master clocks in a cyclic fashion. In response to an increment input, the phase shift between two outputs shrinks to 3 clock periods. Thus, the phase shift between two output pulses on a single output channel shrinks from 16 clock periods to 15 clock periods. Similarly, in the presence of a decrement input, the phase shift between two outputs expands to 5 clock periods. Thus, the phase shift between two output pulses on a single output channel expands from 16 clock periods to 17 clock periods.

The rotator was tested at high frequency and was found operational up to a clock frequency in excess of 16 GHz (Fig. 11). In the absence of the control inputs and a 16.384 GHz master clock, the fundamental tone in the frequency spectrum is seen at 1024 MHz for the clock decimated by a factor of 16 by the TFF chain in the phase modulator. In response to an increment on one input channel at 1024 MHz, the frequency shifts in a positive direction by 1024/16 or 64 MHz, so that the fundamental tone is now at 1088 MHz. Similarly, in response to a decrement on one input channel at 1024 MHz, the frequency shifts in a negative direction by 64 MHz, so that the fundamental tone is at 960 MHz.

D. Output Driver: Differential Digital Amplifier

The four outputs of the phase rotator are used to drive DACs based on RSDCA cells (non destructive RS flip-flop followed by an SFQ-to-DC converter) followed by a JTL amplifier. The outputs from both the RSDCAs are summed together and further amplified by the differential digital amplifier to provide the pre-distorted waveform. The digital amplifier consists of eight SQUID stacks, grouped in four combinations of two series stacks as shown in Fig. 12. Each SQUID stack is a linear array of 48 SQUIDs biased near its critical current. The current outputs of the DAC's are used to modulate the voltage of each of the SQUID stacks. Digital control signals (SET1, RESET1 and SET2, RESET2) from the rotator outputs are chosen to place a combination of two series stacks in the resistive state and other two in the superconductive state, to provide lossless paths for the applied voltages to the two differential outputs.

The amplifier is used to generate the pre-distorted waveform as shown in Fig. 7. The diagonal pairs of the inner SQUID stacks

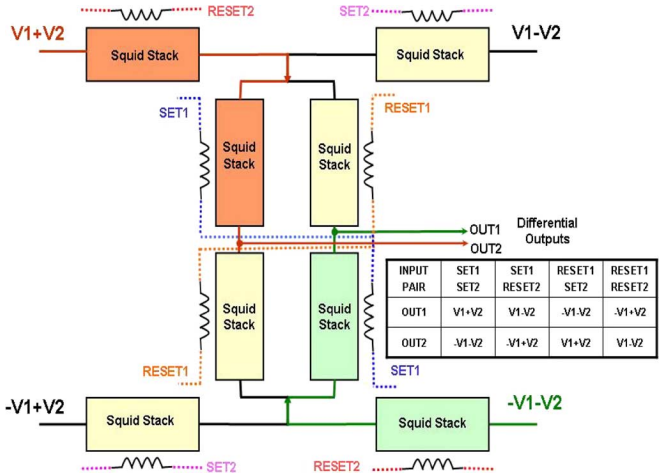


Fig. 12. Differential digital amplifier with dynamic equalization. Instead of a SQUID stack one can use a SQIF.

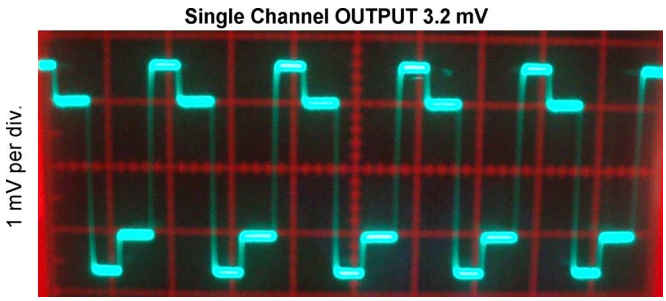


Fig. 13. Low frequency test results for the differential digital amplifier based on SQUID stacks showing a four-level pre-distorted waveform.

control the polarity of the output voltage and are driven by the polarity outputs of the rotator. The outer pair of SQUID stacks is driven by the magnitude outputs of the rotator. In order to achieve high speed operation, the stacks are arranged in push-pull configuration; with individual SQUID stacks driven by the control line splitting into multiple parallel branches with no more than eight SQUIDs per branch.

Fig. 13 shows the oscilloscope trace for one of the outputs of the amplifier tested at low frequency. The gain of the pre-distorted peak can be varied by adjusting the applied voltages across the voltage rails.

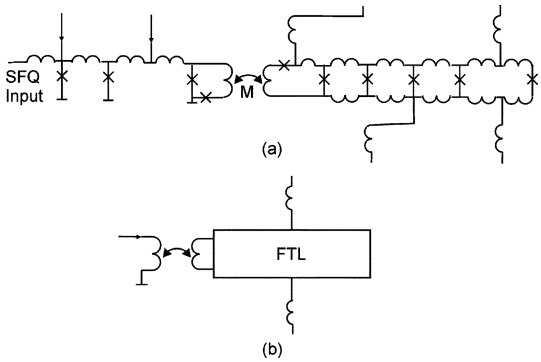


Fig. 14. Elemental VM circuit: (a) Equivalent circuit. (b) Notation.

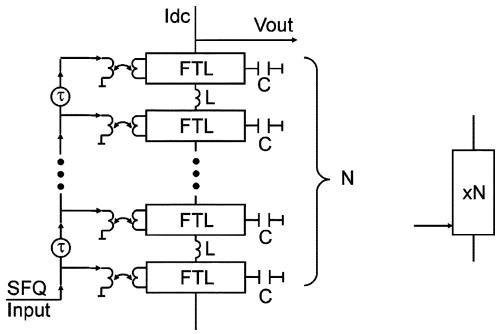


Fig. 15. Structure of VM based output driver module with voltage gain N.

E. Differential Amplifier Based on Voltage Multiplier

Instead of the SQUID arrays or possibly SQIFs [8], a voltage multiplier (VM) can be used to form the differential amplifier shown in Fig. 12. The voltage multiplier was developed for a low-speed but very accurate DAC for metrology applications [2]. It is based on processing SFQ pulses with very high accuracy due to the fundamentally accurate Josephson frequency-to-voltage relationship. The elemental VM circuit can be described as a Floating Transmission Line (FTL) that receives SFQ pulses from a conventional (grounded) Josephson Transmission Line (JTL) (Fig. 14). Circuit details of such a device were discussed in [9].

In order to increase speed and loading capability for use in the high-speed DDS, the VM circuit was re-optimized. This re-optimization dramatically increased the speed without any loss in the fundamental accuracy of the generated waveforms. This is because the output voltage is strongly proportional to the frequency of a reference signal f shown in Fig. 16. In particular, this means that the output voltage of the driver does not depend on the load current during correct operation. This is the principal advantage of the VM based drivers over conventional SQUID-array based drivers.

Our analysis showed that the speed of the VM circuits is limited mostly due to distorting effects of parasitic capacitances of each serially connected FTLs to ground (Fig. 15). However, this distortion could be represented as a propagation delay in a parasitic micro-strip line composed of the parasitic capacitances and inductances of the wires connecting FTLs. As a result, the bandwidth could be dramatically increased if SFQ pulses are applied to the FTLs with delays τ equal to corresponding propagation delays in serially connected FTLs.

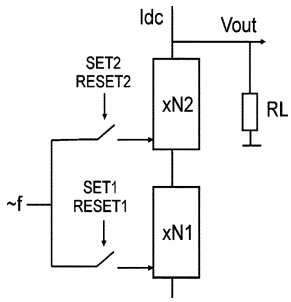


Fig. 16. Series connection of two VM modules controlled by NDRO switch.

The output driver could be composed of two voltage multipliers with different gains (N1 and N2) as shown in Fig. 16. Common RSFQ cells with non-destructive readout (NDRO cells) can be used to implement switches which are shown schematically in Fig. 16. The driver module has been fabricated and successfully measured at a low speed. In particular, it has been found that the output voltage of the driver remains constant within ± 0.2 mA variations of load current. The achieved margins for the load current allow up to ± 10 mV output voltage with a standard 50 Ohm load.

IV. Conclusion

We have developed the principal components for a Digital-RF direct digital synthesizer capable of direct generating of gigahertz RF waveforms. These components include a digital interpolation filter, a modulator, an equalizer, and an output driver. This output driver is formed as a differential amplifier, which can be assembled from either SQUID arrays, SQIFs, or voltage multipliers.

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