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High-resolution ADC operation up to 19.6 GHz clock frequency

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Abstract
We have designed, fabricated and tested the second-generation (2G) design of a high-resolution, dynamically programmable analog-to-digital converter (ADC) for radar and communications applications. The ADC chip uses the phase modulation–demodulation architecture and on-chip digital filtering. The 2G ADC design has been substantially enhanced. Both ADC front-end modulator and demodulator, as well as decimation digital filter, have been redesigned for operation at 20 GHz. Test results of this 6000 Josephson junction 2G ADC chip at clock frequencies up to 19.6 GHz are described. These test results were compared to the results of ADC functional simulation using MATLAB.

1. Introduction

Progress in wireless communications, radar and electronic warfare systems relies on the ability to utilize more and more sophisticated digital signal processing. However, the effectiveness of such digital signal processing depends on the quality of the digital input data, which represent the digitized analog input signal delivered from the antenna. High-resolution, high-fidelity analog-to-digital converter (ADC) technology is critical to the quality of this digitization.

In the past, we reported the design and evaluation of a superconductor ADC based on the phase modulation–demodulation architecture [1]. These results showed that even our first-generation (1G) ADC design was able to compete favourably with the best semiconductor ADCs and demonstrated superior linearity [2, 3]. To improve the ADC performance further, a new second-generation (2G) design was developed [3]. In this paper, we present details of measurements and evaluations of the first 2G ADC chip.

2. Summary of design innovations

The most straightforward way to increase performance of an ADC is to increase clock frequency of the operation. Therefore, the prime objective of our new ADC design was to increase the clock frequency. The goal for this 2G ADC chip was to achieve 20 GHz without any change in our current fabrication process with 1 kA cm^{-2} critical current density[3]. This would be 50% higher than the established 12.8 GHz operation of the 1G ADC design reported earlier [2, 3].

In order to achieve such a speed increase, all high-speed parts of the ADC chip were redesigned including both an ADC front-end (modulator–demodulator) and a decimation digital filter. Figure 1 shows the new 15-bit 2G ADC chip with a two-channel synchronizer. The ADC front-end (the inset to figure 1) was redesigned with new library cells, including rebalancing of the reference phase generator, quantizer, multi-channel synchronizer and interconnecting delay lines based on Josephson transmission lines (JTLs). A new input transformer design was employed instead of an old four-hole design. Perhaps, the most substantial innovations were employed for the new fully modular digital filter: a fast carry-look-ahead algorithm, a new high-speed, micro-pipelined accumulator cell design based on half adders and a new timing scheme with clock skipping for the filter readout [4]. The ADC was also equipped with a programmable clock controller [3] with externally selectable 1:128, 1:64, 1:32 and 1:16 clock decimation ratios. This clock controller allows us to dynamically program the ADC output sampling rate and bandwidth.

[3] The standard HYPRES Nb process flow and design rules are available at www.hypres.com.

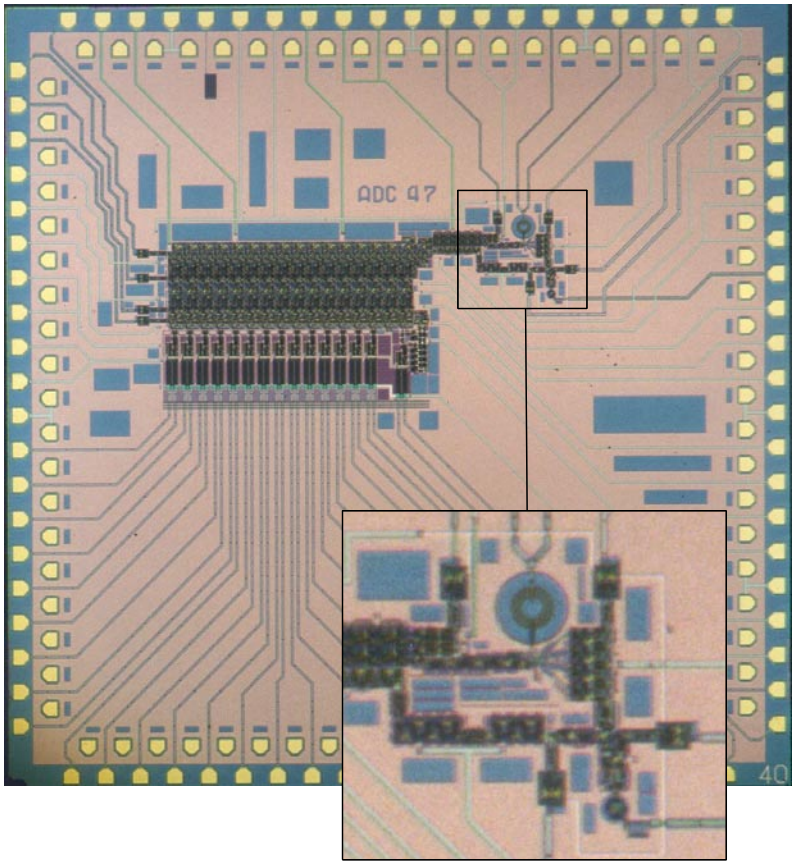

Figure 1. A 15-bit 2G ADC chip with a two-channel synchronizer. The inset shows the ADC front-end (modulator). The 6000-junction 1 cm^2 chip was fabricated using HYPRES' standard 1 kA cm^{-2} process with a 3 μm minimum junction size.

3. Test results

We tested the first sample of the 2G ADC using our ADC test set-up described in detail in [3]. The new ADC chip was able to operate up to 19.6 GHz clock frequency, which is very close to the target 20 GHz. The ADC output data was acquired to a computer running our custom 'ADCtools' ADC analysis software. We performed an FFT analysis with 'Blackman' windowing on 8192-point and 16 384-point acquisitions. For evaluation of the ADC chip at Nyquist sampling rate (at $\times 2$ input tone), we performed additional off-chip low-pass filtering in software, if necessary, since ADC chip has the maximum decimation ratio not exceeding 1:128.

Figure 2 shows typical measured FFT spectra for 10 MHz input sine wave sampled at an 18.6 GHz clock frequency. Up to this clock frequency, the ADC chip demonstrated excellent stability—about 90% of all 16K-point FFT acquisitions were good, i.e. they did not contain any glitches (digital errors). This is substantially better than it was with the 1G ADC chip even at 11.2 GHz. The stability was somewhat lower at the highest operational clock frequency of 19.6 GHz. Figure 3 shows the results of the 19.6 GHz operation with a 40 kHz unfiltered input tone. While the reconstructed 40 kHz signal (the inset to figure 3) was visually fine, FFT analysis showed some excessive noise content. Therefore, we concluded that this ADC chip has its peak performance at 18.6 GHz.

Figure 4 shows the dynamic range of the 2G ADC chip operating at an 18.6 GHz clock frequency and a comparison with its operation at 11.2 GHz. As expected, the increased clock frequency produced a better performance both in terms of signal-to-noise ratio and distortion (SINAD) and spur-free dynamic range (SFDR). However, the peak SINAD and SFDR performances of the 2G ADC chip still did not exceed the previously demonstrated performance of the 1G ADC design reported in [3]. In order to compare both ADC designs, we conducted tests of both ADCs at the same conditions. Figure 5 shows comparative performance of these two ADC chips operating at 11.2 GHz and 10 MHz input tone. Both chips demonstrated the expected linear growth of dynamic range with amplitude over several orders of magnitude. The 2G ADC chip was designed to be more sensitive, and indeed, it exhibited a greater SINAD and SFDR than the 1G ADC chip for a given voltage input in the ranges they overlap. But the lower slew rate limited the maximum dynamic range available. This suggested that some excess noise affected the performance of the 2G ADC chip.

4. Simulation and comparison with measurements

In order to understand and correct this problem, we carried out MATLAB functional simulations of the ADCs in addition to the experimental measurements. Figure 6 shows a MATLAB functional model of the ADC architecture that we used in our

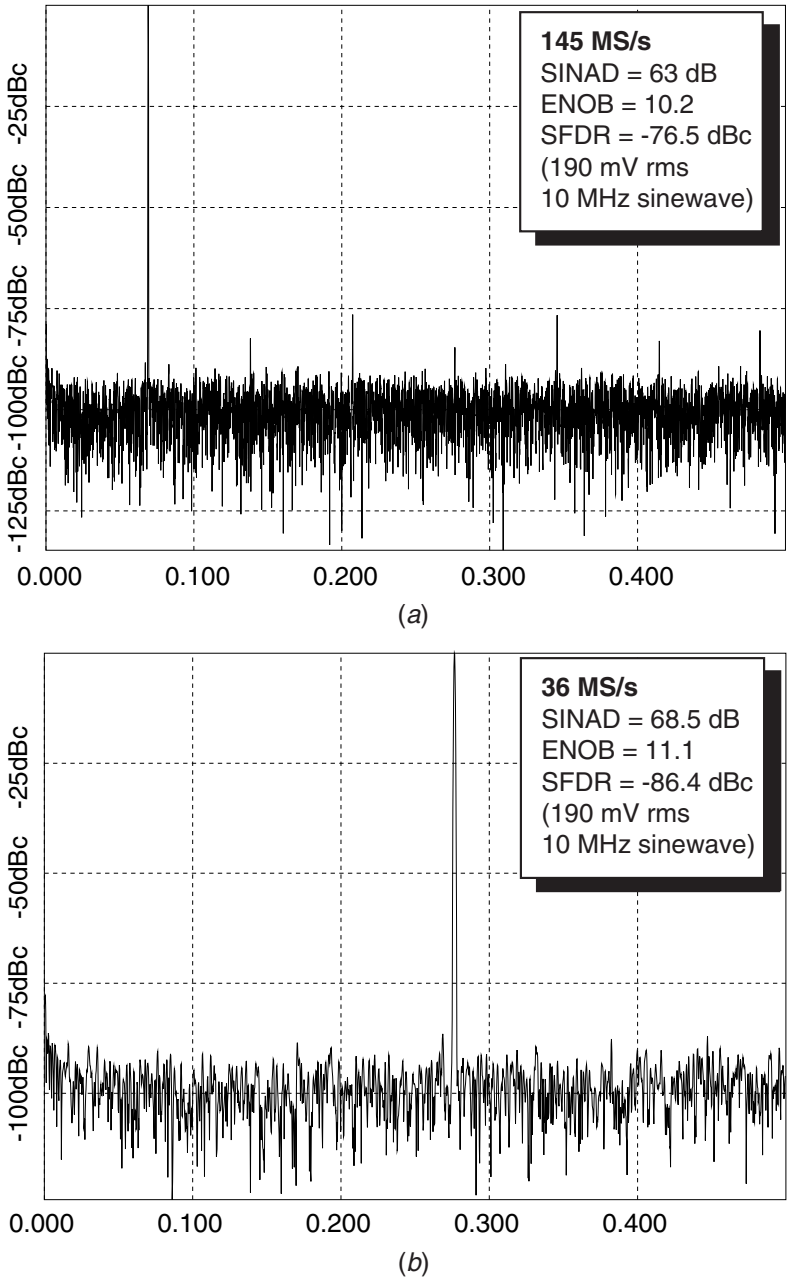

Figure 2. Measurement of the 2G ADC chip at 18.6 GHz clock using 16K-point FFT for a 10 MHz input sine wave. (*a*) 145 MS/s data for a 1:128 on-chip decimation and (*b*) 36 MS/s data with an additional 1:4 off-chip averaging.

MATLAB program. Details of this ADC architecture can be found elsewhere [1, 3].

One way to model all sources of excess noise is to add a single random (white) noise source to the input signal. This was done in the MATLAB program simply by adding one sine wave component (of fixed amplitude, but with random phase) for each output frequency of the digital Fourier transform. In this way, we could compare the theoretical model directly with the measurements, although the results are slightly different each time due to the random number generator. As one can see from the figures 7 and 8, the agreement is excellent for both ADCs for the SINAD and SFDR.

There is only one adjustable parameter for each chip, which is the rms amplitude of the noise. The fit to a straight line (with a slope of one) on this log–log plot corresponds to a noise floor which is independent of amplitude from very small to the slew rate limit, assuring that the ADC is ideally linear and does not generate harmonics that impact the frequency spectrum.

We also used the slew rate limit, above which the performance of the ADC falls sharply, as a calibration point. It assures the exact conversion between input signal amplitude presented in fluxons Φ_0 in simulations and the experimentally measured signal amplitude in millivolts. For our ADC architecture, the slew rate limit corresponds to an amplitude of the signal derivative of one-half flux quantum per clock period, or a signal amplitude $A_{\max} = (\Phi_0/2) f_{\mathrm{clk}}/2\pi f$, where f is the signal frequency. For a typical clock frequency of 11.2 GHz

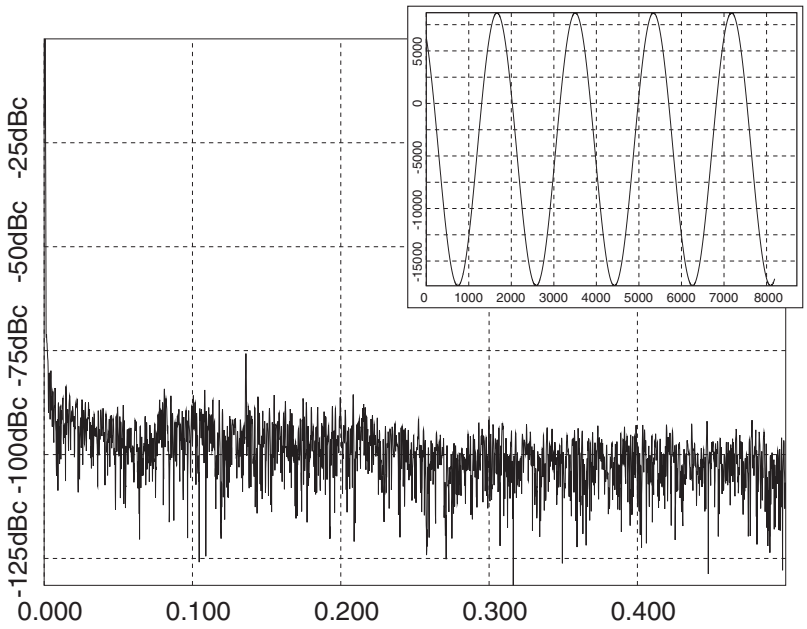

Figure 3. Measured 8K-point FFT and reconstructed output (inset) for an unfiltered 40 kHz input sine wave. The 2G ADC chip ran at 19.6 GHz clock and was set for a 1:128 decimation ratio (153 MS/s output sample rate).

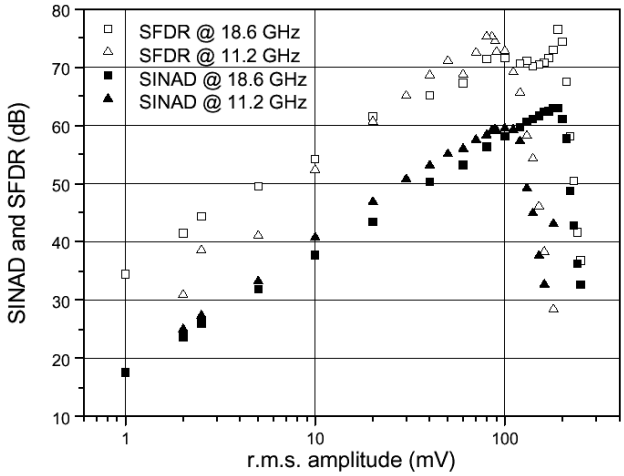

Figure 4. Measured SINAD and SFDR for a 2G ADC chip running at 11.2 GHz and 18.6 GHz clock for a 10 MHz input sine wave. The selected 1:128 decimation ratio in the digital filter provides 87.5 MS/s and 145 MS/s output sample rate, respectively.

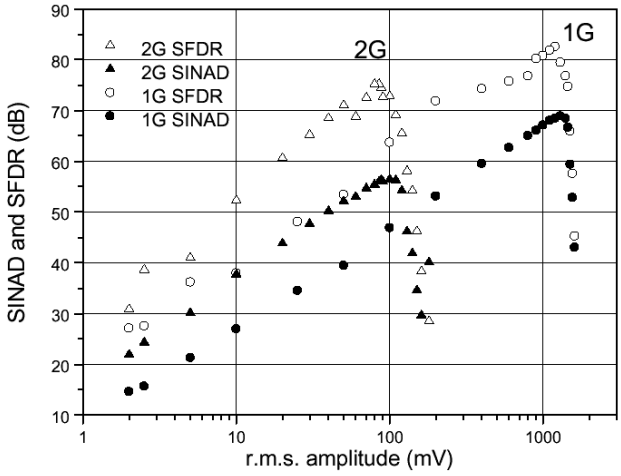

Figure 5. Measured SINAD and SFDR for a 1G and a 2G ADC chip running at 175 MS/s (11.2 GHz clock with a 1:64 output decimation) and a 10 MHz input sine wave.

and a signal frequency of 10 MHz, this corresponds to $A_{\max} = 89\,\Phi_0$, or an rms value $A_{\rm rms} = 62.9\Phi_0$ or 36 dB[Φ_0]. If the SINAD at the slew rate limit is measured to be 70 dB (as it is for the 1G ADC design), then the rms noise amplitude is $N = 36 - 70 = -34$ dB[Φ_0] $= 0.02\,\Phi_0$. This can be converted into a noise density value by dividing the noise amplitude by the square root of the effective bandwidth. For a sampling rate of 11.2 GHz, decimated by a factor of 64, the output sampling rate is 175 MHz and so the effective Nyquist bandwidth is $B = 87.5$ MHz. The noise density is then $n = N/\sqrt{(B)} = 2.1\,\mu\Phi_0/\sqrt{(\text{Hz})}$.

In contrast, the 2G ADC chip seems to be much noisier, at least in terms of equivalent flux in the signal quantizer input. The SINAD at the slew rate limit (for a decimation factor of 64) corresponds to about 58 dB, so that the rms noise amplitude is $N = 36 - 58 = -22$ dB[Φ_0] $= 0.11\Phi_0$. Dividing the noise power by the effective bandwidth $B = 87.5$ MHz, the noise density is now $n = 8\,\mu\Phi_0/\sqrt{(\text{Hz})}$.

The noise floor for both chips is significantly larger than the expected limit set by the quantization noise. A simple estimate for the quantization noise floor is given by $N_{\rm q} = \Phi_0/m\sqrt{(24 f_{\rm clk})}$, where m is the number of synchronizers in the demodulator section of the ADC front-end. In the present case, with $m = 2$ and $f_{\rm clk} = 11.2$ GHz, this gives $N_{\rm q} = 1.0\,\mu\Phi_0/\sqrt{(\text{Hz})}$. This is consistent with the results of the MATLAB simulations. So there is a significant amount of excess noise in both cases. It is worth noting that independent (uncorrelated) noise powers add linearly, so that the amplitudes add in quadrature. Then, the excess noise is

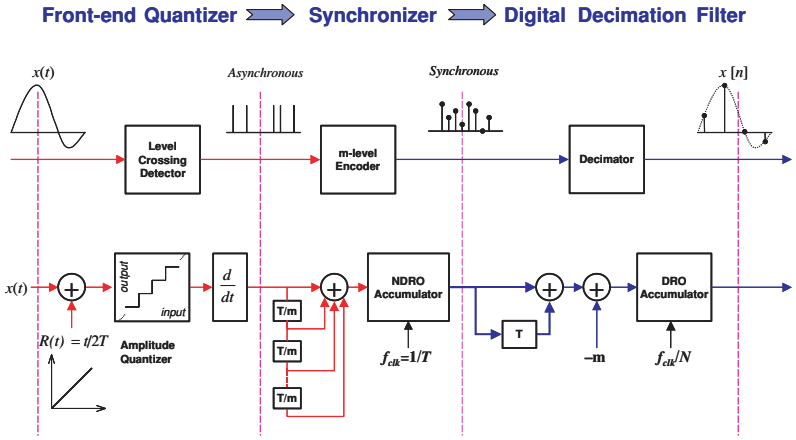

Figure 6. Functional model of our ADC based on phase modulation–demodulation architecture.

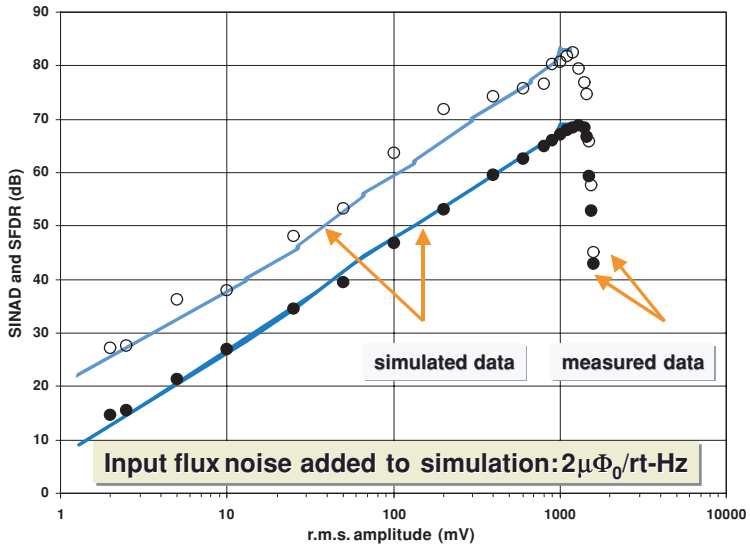

Figure 7. Comparison of measured and simulated data for the 1G ADC chip running at 11.2 GHz clock, 175 MS/s output sampling rate (1:64 decimation), and 10 MHz input sine wave. In order to achieve a close fit, a 2 $\mu\Phi_0/\sqrt{\text{Hz}}$ input flux noise was added.

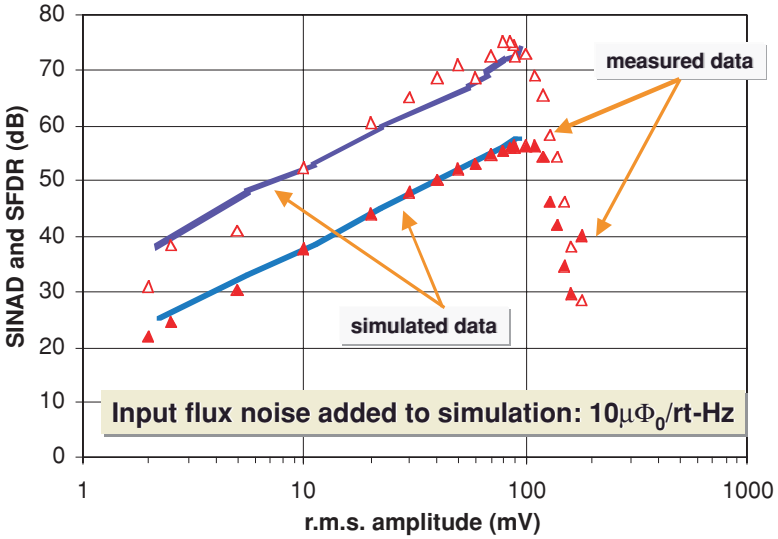

Figure 8. Comparison of measured and simulated data for the 2G ADC chip running at 11.2 GHz clock, 175 MS/s output sampling rate (1:64 decimation), and 10 MHz input sine wave. In order to achieve a close fit, a 10 $\mu\Phi_0/\sqrt{\text{Hz}}$ input flux noise was added.

$N_{ex} = 1.8\,\mu\Phi_0/\sqrt{}(\mathrm{Hz})$ for the 1G and $7.9\,\mu\Phi_0/\sqrt{}(\mathrm{Hz})$ for the 2G chip. Again, this is generally consistent with the MATLAB simulations.

5. Conclusions

The first sample of a 6000-junction 2G ADC chip showed correct operation up to 19.6 GHz: to our knowledge, this is the world's fastest operation of the most complex superconductive digital chip to date. We have completed the measurement and evaluation of the first 2G ADC chip and found its excellent stability at high-speed operation.

We also found that the 2G ADC chip exhibited some excessive noise limiting its performance. For better understanding, we performed MATLAB simulation of this ADC and compared it with the experimental data. The excellent fit was achieved assuming the presence of an excess noise about five times higher than that of the 1G ADC design. We believe that this noise is associated with the non-optimal input circuitry and/or fabrication. Further testing of other ADC samples and comparison with the MATLAB model should enable the correction of this problem.

Acknowledgments

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