Superconductor Digital Receiver Components

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***Abstract*—We have developed and experimentally demonstrated several new RSFQ circuits, designed as components for digital receivers that are being developed by HYPRES. The first circuit is a digital phase generator, which produces a periodic digital signal with a controllable phase shift. This signal is obtained by decimation of an external high frequency signal by a factor of 1024, and provides a controllable phase shift with digital precision of $\pi/512$. The second circuit, a precise digital static frequency divider, is capable of dividing of an input signal frequency by any integer value between 1 and 1024. The third circuit is a digital quadrature mixer performing digital downconversion of bit-stream data. This report presents results of experimental evaluation of these circuits at speeds in excess of 30 GHz.**

***Index Terms*—Digital signal processors, HF receivers, static frequency dividers, superconducting integrated circuits.**

I. Introduction

A direct digital receiver of wideband radio frequency signals is an attractive application for superconductor digital electronics. In this paper, we report the development of circuit components for realization of two types of digital receivers developed at HYPRES.

Fig. 1 shows the block-diagram of a single channel of a Channelizing Digital Receiver. This receiver consists of a common wideband ADC modulator and multiple digital channelizing units for simultaneous extraction of independent sub-bands from the wide receive band with programmable band location and bandwidth [1]. Conversion of the RF signal directly into the digital domain with an ultrafast ADC permits application of this *digital-RF* signal to multiple channelizing units without compromising signal quality. Each channelizing unit consists of a digital quadrature mixer, a Programmable Local Oscillator (PLO), and two second-order decimation filters. In this paper, we present the digital frequency divider as a part of the PLO and the digital quadrature mixer.

Fig. 2 shows the block diagram of a more generic digital receiver based on cross-correlation of the input signal, directly digitized at RF, with a digital waveform template, which defines the properties of the receiver. For example, a simple periodic template at the local oscillator frequency performs functions such as channelization and demodulation of phase-shift key (PSK) modulated waveforms. Implementing more complex functions, such as dehopping and despreading of spread spectrum signals, requires changes in the waveform template only;

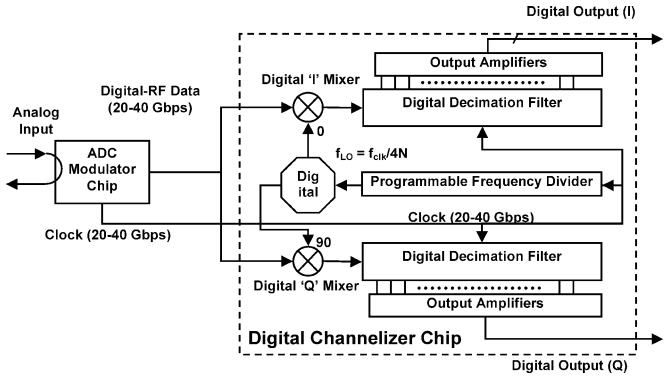

Fig. 1. Block diagram of a channelizing digital receiver.

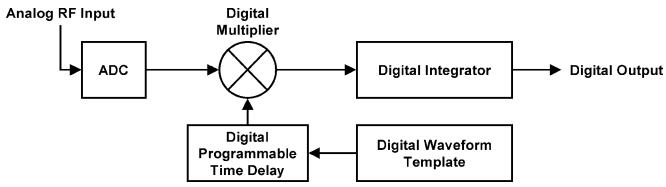

Fig. 2. Block diagram of a generic correlation-based digital receiver.

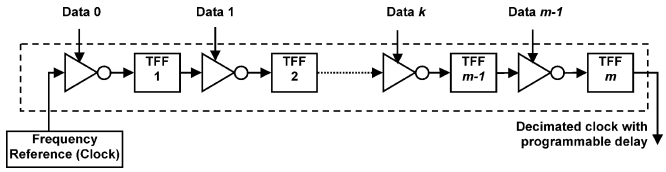

Fig. 3. Block diagram of programmable phase generator.

no hardware change is necessary. The programmable time delay circuit ensures synchronization of the template with digital-RF data. Here, we present a phase synchronization circuit for periodic templates employing programmable discrete time delay.

II. Digital Programmable Phase Generator

As its foundation, the programmable phase generator (PPG) uses the classic binary ripple counter to generate a periodic signal. This simple circuit, comprising a chain of RSFQ toggle flip-flops (TFFs) [2] decimates the input SFQ pulse sequence by a factor of 2^m, where m is a number of TFFs. By extracting an SFQ pulse from the k-th stage of the counter, one can delay the output signal by $T \cdot 2^k$, where T is an input pulse sequence period. Thus, it achieves a phase shift of the output sequence by $2\pi \cdot 2^{k-m}$.

To realize this algorithm, we placed an inverter (NOT gate) [3] before each T flip-flop (Fig. 3). The clock input and the data output of each inverter is connected to the output of the preceding T-flip-flop and the input of the next T-flip-flop respectively. In the absence of data signals, an inverter forward all

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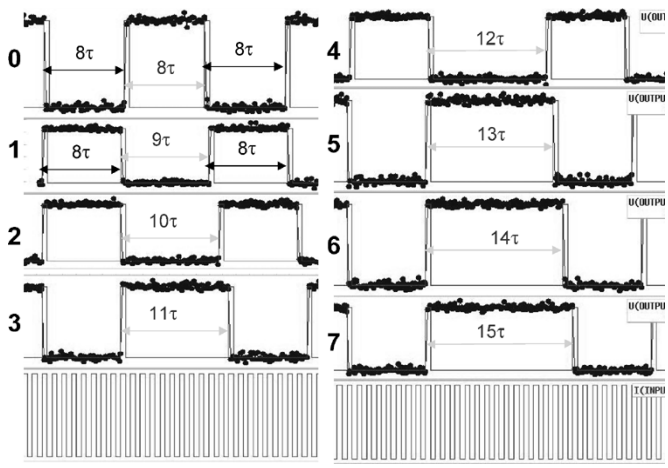

Fig. 4. Functionality test of the PPG.

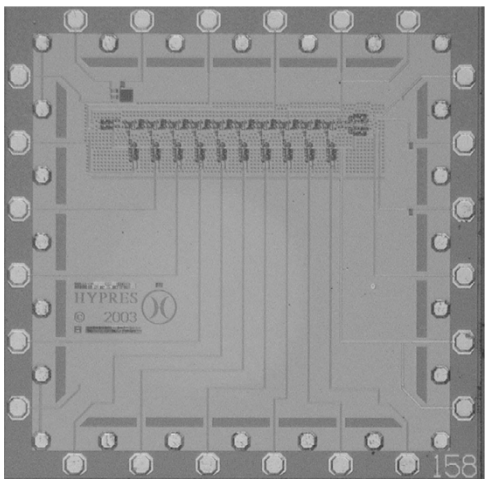

Fig. 5. Photograph of a 5-mm chip fabricated using HYPRES' 1 $\mathrm{kA/cm^2}$ process with a 10-bit programmable phase generator.

clock pulses to its output. When an SFQ pulse is sent to the data input of the inverter, it skips the following clock pulse. Thus, by sending an m-bit binary number N to the control port of the device, we achieve a phase shift the output signal by $2\pi \cdot N \cdot 2^{-m}$.

In order to perform a low-speed functionality test we designed and fabricated a short (3-bit) version of the phase generator. For the high-speed test a full 10-bit phase generator was designed using both 1.0 $\mathrm{kA/cm^2}$ and 4.5 $\mathrm{kA/cm^2}$ HYPRES fabrication processes [5]. We have tested only the 1-$\mathrm{kA/cm^2}$ version of the device.

The low-speed (functionality) test was performed on a 3-bit version of the phase generator. The experiment was performed with the automated test setup Octopux [4]. Fig. 4 was concatenated from responses of the PPG on applying 3-bit numbers (from 0 to 7). The clock frequency in the experiment (bottom trace) was ~500 Hz, which corresponds to a clock period τ of 2.0 ms. The DC bias current margins for this very-low-speed test were 17%.

The high-speed testing was performed on a 10-bit version of the phase generator (Fig. 5). By applying SFQ pulses to corresponding bits, we observed the proper phase shift on the oscilloscope. The minimum phase shift of the 10-bit phase generator is $2\pi/2^{10} \approx 0.006$ rad. We could clearly observe the phase shift

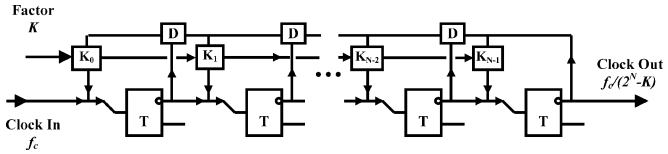

Fig. 6. Block diagram of the programmable frequency divider.

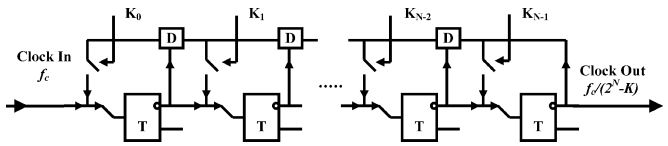

Fig. 7. Block diagram of a simplified version of the PFD.

on the oscilloscope up to a maximum input frequency of 12.288 GHz, which produced a 12-MHz output signal. Although we could not observe the smallest phase shifts at higher frequencies, the device was actually operational up to 40 GHz.

III. Digital Programmable Frequency Divider

Another interesting circuit based on the binary ripple counter is a programmable digital frequency divider (PFD). A programmable local oscillator (PLO) is a very useful part of many DSP systems. The traditional way of producing a pulse signal of needed frequency is to divide a high-frequency reference signal by a certain factor. Previously suggested RSFQ clock dividers were able to decimate only by a factor of 2^n. We have suggested a frequency divider (Fig. 6) capable of dividing input signal frequency by any natural number from 1 to 2^N, where N is a number of bits (length of the circuit).

The frequency divider consists of very well known basic RSFQ cells: T flip-flops, D flip-flops, and Non-Destructive Read-Out cells (NDRO) [2]. The NDRO cells are sequentially connected to form a shift register. That allows loading the divider from a single terminal. For test purposes, we have designed a simplified parallel version of the frequency divider (Fig. 7). Here, we replaced NDRO cells with DC-driven SFQ switches.

The functionality of the PFD is rather complex. When all N switches are OFF ($K = 0$), it works as a regular ripple counter, dividing input frequency by a factor of 2^N. Let us consider the case where we close only the last switch ($K = 2^{N-1}$). Now, the output pulse loops back to the last T flip-flop, setting it to the initial state. Thus, the last T flip-flop becomes effectively shunted and does not participate in the decimation process. So the dividing factor becomes 2^{N-1}. Next, let us consider a slightly more complicated case, when we close only the first switch ($K = 1$). Now, the decimated output SFQ pulse moves through the pipeline structure to shunt the first T flip-flop. For every 2^N-th input SFQ pulse, the first T flip-flop idles its cycle remaining in the initial state. Thus, instead of 2^N, we obtain a decimation factor $2^N - 1$. This can be extrapolated for any given number K from 0 to $2^N - 1$, or decimation factor from 1 to 2^N. The most complicated case is when all switches are shorted ($K = 2^N - 1$). In this case, every T flip-flop is "shunted" with a loopback. Neither of them divides the input signal, thus propagating it to the output without decimation.

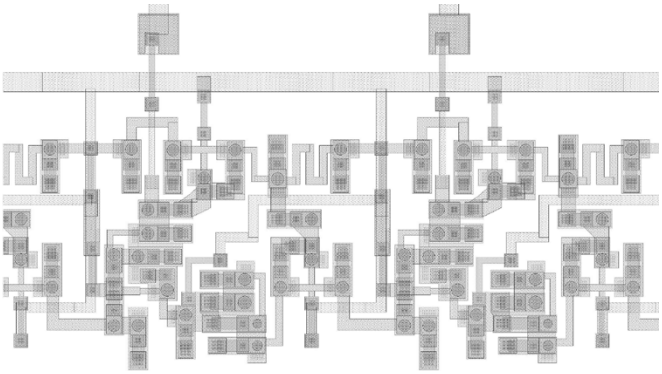

Fig. 8. Layout fragment of 2 bits of the programmable frequency divider.

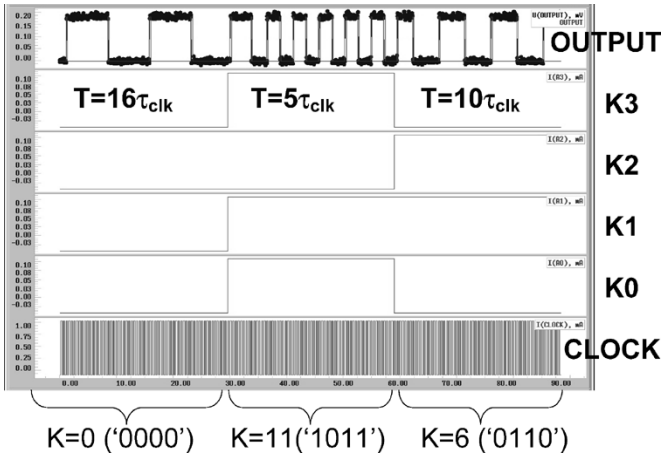

Fig. 9. Functionality test of the 4-bit programmable frequency divider.

A 2-bit fragment of the PFD layout is -shown in Fig. 8. The size of a single stage of the PFD is $150\ \mu\mathrm{m} \times 150\ \mu\mathrm{m}$ for HYPRESs old 3-μm design rules [5]. This fragment is of the parallel version of the PFD (Fig. 7). We have designed and fabricated two programmable frequency dividers: a 4-bit (short) version for low-speed (functionality) testing and a 10-bit for high-speed testing.

The results of a low-speed (functionality) test of the 4-bit PFD are shown in Fig. 9. Here, we apply a low-frequency clock (2 kHz) to the bottom trace, set different 4-bit factors by current levels on DC-driven switches (the next four traces), and monitor the output voltage from the toggling SFQ-to-DC converter (upper trace). As one can see in the picture, the 4-bit PFD decimates the input clock pulses by a factor of 16 for $K = 0$, by 5 for $K = 11$, and by 10 for $K = 6$. It takes 16 (2^N) clock pulses for transitioning from one frequency to another. This number of clock pulses is needed to clean up the shift register (Fig. 7). We have checked DC bias current margins for all 16 numbers. The minimal margin was 8% for $K = 15$ and the maximum margin was 22% for $K = 0$.

A high-speed test was performed on a 10-bit PFD. We used a 50-GHz Agilent 83 650B generator for input signal and monitored the output on a Tektronix TDS694C oscilloscope. The results of this test for 30.72 GHz input frequency is shown in Fig. 10. The programmable frequency divider was operational within 18% DC bias current margins at decimation factor 1024

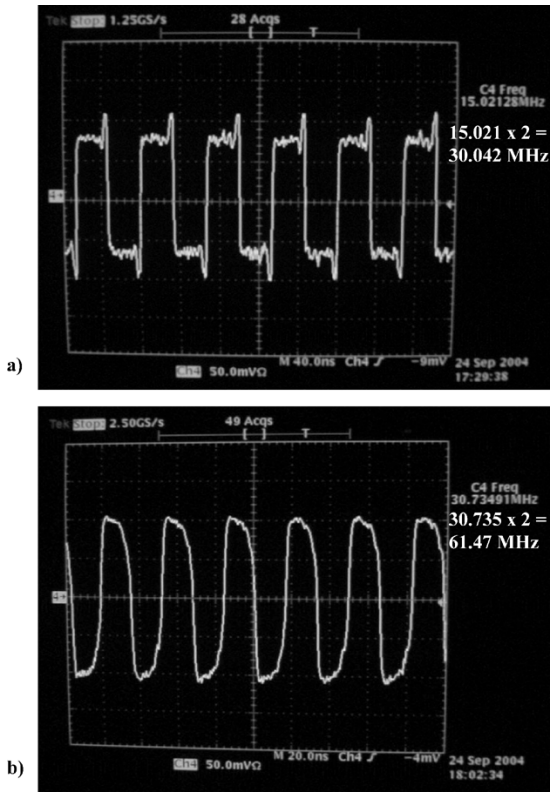

Fig. 10. HF test of the programmable frequency divider at 30.72 GHz. With decimation (a) by 1024 $(K = 0)$ and (b) by 500 $(K = 524)$.

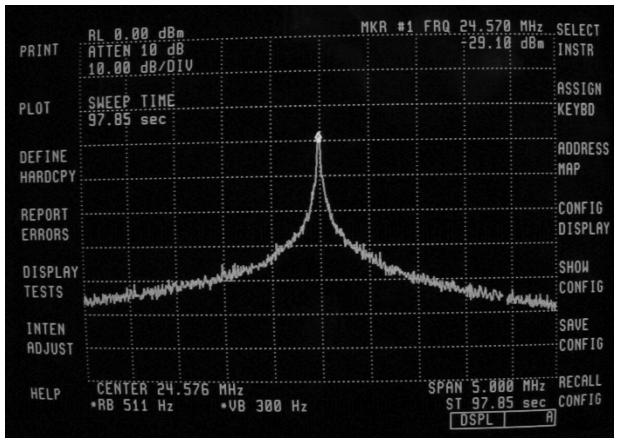

Fig. 11. HF test of the 10-bit PFD with spectrum analyzer.

$(K = 0)$ and within 3% at decimation factor 500 $(K = 524)$. Because of a toggle-type SFQ-to-DC converter, there is an additional factor of 2 in frequency reduction at the output. Also, the low level of the signal and the phase noise from the amplifier caused slight (less than 0.01%) deviation of the measured from the expected frequency. As one can see in Fig. 10(a), the result of decimation of 30.72 GHz by a factor of 1024 $(K = 0)$ is 30.042 MHz, which, within the experimental error, matches the expected 30.0 MHz. At a decimation factor of 500 $(K = 524)$, the expected output frequency is 61.44 MHz, and we have actually observed 61.47 MHz (Fig. 10(b)).

We also performed a high-speed test with HP70000 spectrum analyzer (Fig. 11). The input frequency and decimation

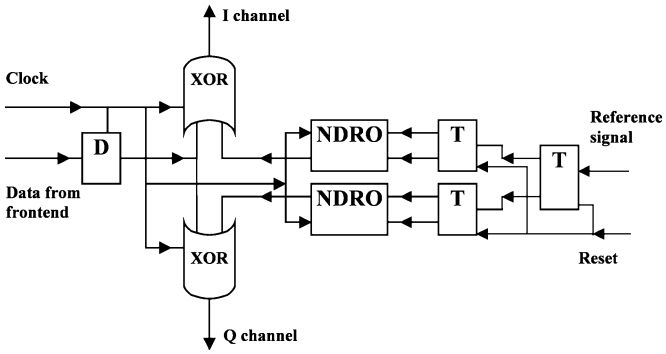

Fig. 12. Block-diagram of the digital I/Q square-wave mixer.

factor were set to 24.576 GHz and 500 ($K = 524$). The expected output was 24.576 MHz (taking into account the additional factor of 2). We observed a single peak at the expected frequency indicating the absence of systematic errors in the device.

We have tested the digital programmable frequency divider at up to 40 GHz clock frequency. The circuit starts malfunctioning at $K = 511$ at frequencies above 31 GHz. We have also designed a PFD for the 4.5 $\mathrm{kA/cm^2}$ HYPRES' fabrication process [5] and expect its maximum speed to be around 60 GHz.

IV. Digital I/Q Mixer

An important component of the digital receiver being developed by HYPRES is a digital I/Q mixer for converting narrowband (~5 MHz) signals down from a few GHz. To achieve this goal with maximum efficiency we chose a circuit that is similar in principle to the Gilbert quadrature mixer [6]. The basic idea of this mixer is to use square waves as a local oscillator signal instead of sine waves. The mathematical representation of square wave is $G(t) = sign[\sin(\omega_{LO} \cdot t)]$, where ω_{LO} is a local oscillator frequency. The digital version of such a mixer is comparably easy to implement in RSFQ in case of single-bit coding, e.g. output of a delta-sigma modulator.

The most straightforward implementation of squarewave digital mixer in RSFQ is shown in Fig. 12. The right side of the device on the block diagram serves as a single-bit square wave generator. The binary tree of resettable T flip-flops creates two (I and Q) local oscillator signals with 90° relative phase shift. The T flip-flops control RS-type NDRO cells, which, in turn, create digital square waves turning on and off a stream of SFQ pulses. Modulated signal gets mixed with 90° shifted square waves on XOR cells [2], producing I and Q products. Here, we used a combination of an RS-type NDRO cell and a T flip-flop, instead of a T-type NDRO cell, in order to avoid a possible collision between the NDRO read-out pulse and reference pulse. Such a collision may cause a wrong phase shift between I and Q local oscillator signals. If such a problem occurs, the only way to correct it is by applying a RESET signal, and we do not want to do it too often. Despite its simple design, this version of the mixer has issues with timing, limiting its performance to unacceptable levels.

To avoid this problem, we have designed a novel mixer performing single-bit-stream XOR multiplication (Fig. 13). In this case, we use the simple fact that $A \otimes 0 = A$ and $A \otimes 1 = \overline{A}$. After

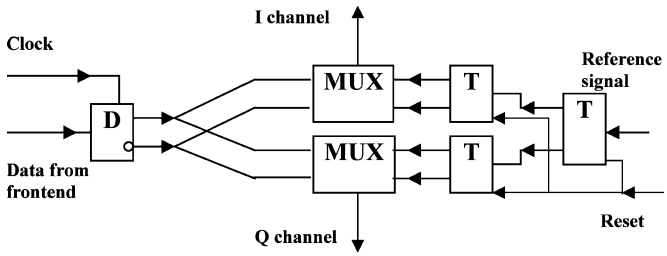

Fig. 13. Block-diagram of a novel digital I/Q square-wave mixer.

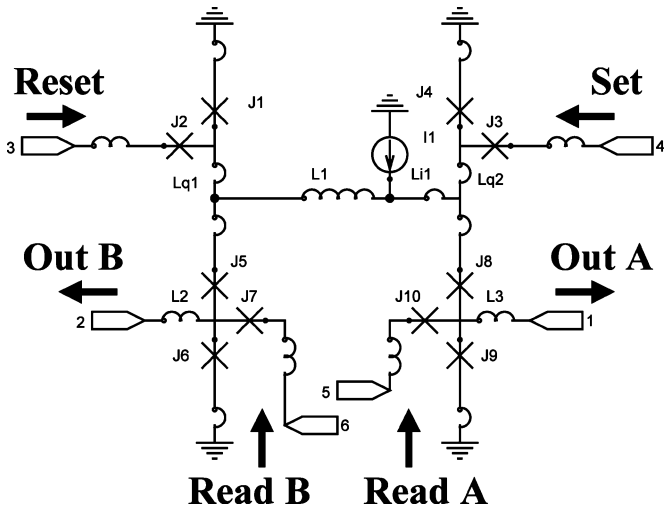

Fig. 14. Schematics of the dual-port NDRO cell.

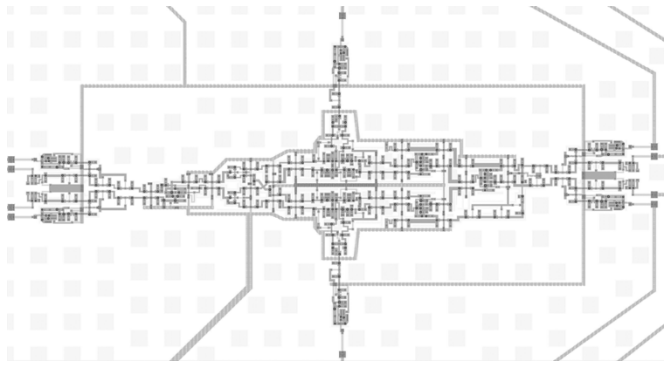

Fig. 15. Layout of digital I/Q mixer.

the modulated signal passes through a D flip-flop with complementary outputs (DFFC) [7], it becomes asynchronous. Multiplexing direct and inverted data outputs to the proper channel, we effectively perform digital I/Q signal downconversion. The multiplexing is done by two multiplexer cells controlled by the same T flip-flop binary tree as in Fig. 12, providing a 90° phase shift between I and Q channels.

The multiplexer is based on the same template cell as the demultiplexer from [7]. This cell (Fig. 14) basically comprises a dual-port NDRO cell. From this cell, a designer can build either a demultiplexer [7] by merging inputs A and B, or a multiplexer by merging outputs A and B.

We have designed and fabricated the digital I/Q mixer using the standard HYPRES 1 $\mathrm{kA/cm^2}$ fabrication process (Fig. 15). The same design was also converted to the standard HYPRES 4.5 $\mathrm{kA/cm^2}$ fabrication process.

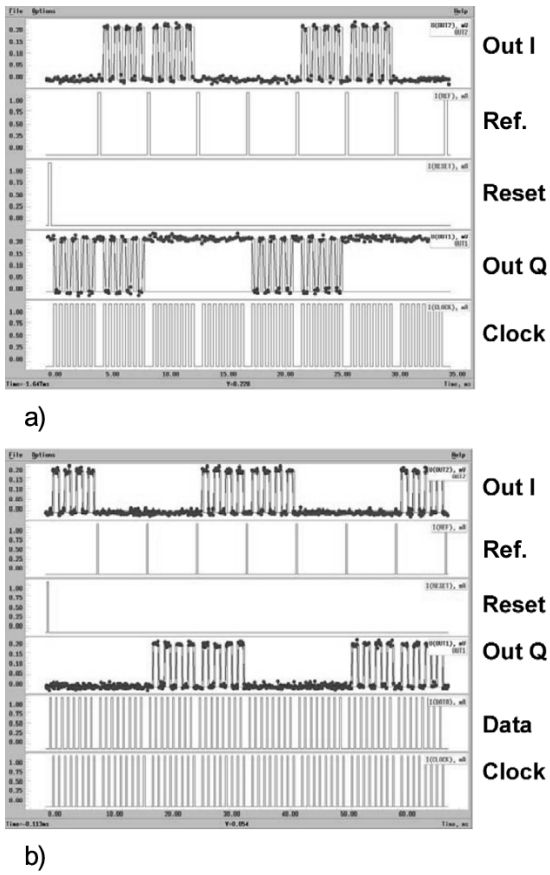

Fig. 16. Low-speed functionality test of the mixer, with maximum negative slew rate signal (a) and maximum positive slew rate signal (b).

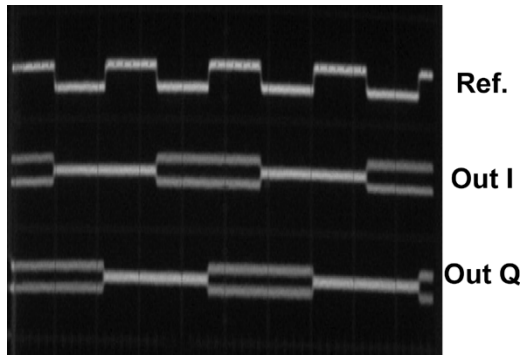

Fig. 17. High-speed test of the mixer at maximum negative slew rate signal case. Clock—42 GHz, no Data, Reference—20 kHz.

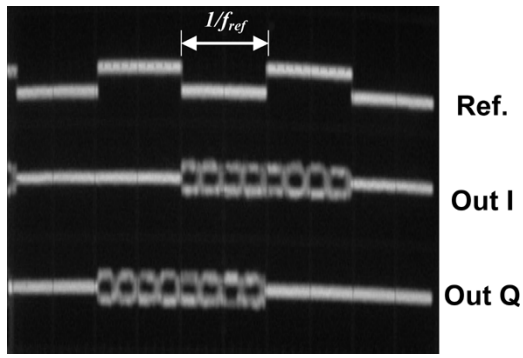

Fig. 18. High-speed test of the mixer. Clock—40.0 GHz, Data—10.000 01 GHz, Reference—10 kHz.

In order to demonstrate functionality of the digital I/Q mixer, we have first carried out a low-speed functionality test (Fig. 16). The most critical test conditions occur at the two extreme cases: maximum negative signal, when the modulator output is zero (Fig. 16(a)), and the maximum positive signal, when the modulator output is all "ones" (Fig. 16(b)). In the first case, all input SFQ pulses go to the inverted output of the D flip-flop only (see Fig. 13); in the second case, only to the direct output. In both cases, the I and Q outputs of the mixer produced the correctly (90°) phase shifted I and Q outputs. The mixer was operational within 16% DC bias margins.

For high-speed testing of the mixer, we applied high-speed data and low-speed reference signal. On the oscilloscope (Fig. 17), we observed an eye-diagram for I and Q outputs synchronized to the reference signal. First, we applied only the clock signal, emulating a trail of zeros from the modulator. The output voltage of I and Q monitors (bottom traces) formed eye diagrams shifted by 90° in accordance with the Reference signal monitor (upper trace). The output signals were monitored with toggling SFQ-to-DC converters with DC voltage swing ∼0.3 mV. Because of this, the absence of output signal leaves a double line on the oscilloscope (0 and 0.3 mV), and the high-speed output leaves a single line at an average voltage 0.15-mV. The clear "eyes" in Fig. 17 indicate a very low error rate for operation at a clock frequency up to 42 GHz within 6% DC bias current margins.

To verify high-speed operation, when the output from the modulator is not "all-zeroes", we applied to the data input of the mixer (Fig. 13) a signal at 1/4th of the clock frequency ($f_{data} = f_{clk}/4$). To study possible malfunctioning due to simultaneous arrival of Clock and Data SFQ pulses, which is forbidden in RSFQ, we did a beat-frequency test, i.e. a slow phase creep between data and clock ($f_{data} = 0.25f_{clk} + f_{ref}$). Now, the output from the modulator is a one-to-three mix of "ones" and "zeroes". This causes both channels to generate HF output, and therefore, there should be no "eyes" on the oscilloscope screen for proper operation. Increasing the clock signal frequency (and proportionally the data signal frequency), we stopped at the point when the first sign of malfunctioning (eye diagram) appeared (Fig. 18). This occurred for a 40-GHz clock and 10.000 01-GHz data.

The reason for this malfunction is in the performance of the input DFFC (Fig. 13). If two SFQ pulses arrive at the Data and the Clock input terminals of DFFC within ∼10 ps time interval (for the given fabrication process), the DFFC ignores the Data pulse and produces inverted output (as if there was a Clock pulse only) [7]. This means that at some particular phase shift between Clock and Data SFQ signals, the mixer ignores the actual Data and behaves as if the Data were zero (Fig. 17). A 40-GHz clock rate gives a 25 ps period between clock pulses, leaving only 5 ps "room" for proper functionality. Each "eye" in Fig. 18 represents one clock period. Four "eyes" in a single Reference period indicates correct data to a clock frequency ratio (1/4). When we

increased the clock frequency above 40 GHz, the small operation regions between the "eyes" disappeared, giving a picture similar to Fig. 17. This experiment shows that the maximum operational bit rate of the mixer is 40 GHz.

V. Conclusion

We designed, fabricated using the 1.0-$\mathrm{kA/cm^2}$ HYPRES process, and successfully tested three novel RSFQ devices for digital receivers developed at HYPRES. The Digital Programmable Phase Generator, the Digital Frequency Divider, and the Digital I/Q Mixer were successfully tested up to a 40 GHz clock rate, well over the intended system clock rate of 20 GHz. We expect to double their performance using the 4.5-$\mathrm{kA/cm^2}$ standard HYPRES process.

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