A Prescaler Circuit for a Superconductive Time-to-Digital Converter

Steven B. Kaplan, Alex F. Kirichenko, Oleg A. Mukhanov, and Saad Sarwana

***Abstract*—The high-speed capability of superconductive electronics is being harnessed to develop a time-to-digital converter (TDC) with picosecond time resolution. We have designed and successfully tested prescaler circuits for improving TDC resolution first to 5 ps, and then below. These circuits are designed to act as a vernier for a superconductive TDC that counts clock periods using a binary counter. One prescaler circuit has already demonstrated 5 ps resolution at a clock frequency of 20 GHz.**

***Index Terms*—Time-to-digital converter, analog prescaler, superconductive digital electronics, time-of-flight**

I. Introduction

Measuring the time of flight (TOF) of nuclear and high-energy particles is a standard method of particle characterization. TOF determination requires three critical elements: a flight path sufficiently long to exclude errors, fast detectors or other sources of precise start and stop signals, and electronics with sufficient dynamic range and precision to resolve the TOF time difference.

The recent development of microchannel-plate (MCP) detectors with less than 10 ps of jitter would enable experiments with extraordinary time resolution if an appropriate TDC were to be developed. We do not know of any TDC systems with a time resolution better than 10 ps. However, by using delay lines, constant fraction discriminators, and a time-to-amplitude converter, it is claimed that a commercial TDC has a time resolution of 10 ps [1].

Rapid Single Flux Quantum (RSFQ) electronics [2] can provide 5-ps time resolution using present Niobium (Nb) trilayer technology [3]. Eventually, Nb technology will surpass 1-ps resolution with modest improvements in lithography. This extraordinary time resolution can be accomplished using less than 1 mW of power dissipation per TDC channel. Moreover, Nb technology is naturally radiation hard [4]. This enables measurements in harsh accelerator laboratory environments.

HYPRES is working together with Fermi National Accelerator Laboratory (FNAL) to develop a TDC system for the so-called MuCool experiment. This Department of Energy effort is designed to test the feasibility of cooling muons for a muon collider. The cooling method requires the muons to be time-stamped with better than 10-ps time resolution. The HYPRES TDC system will have a dynamic range of better than 17 bits, and a time resolution of better than 5 ps.

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The key to obtaining such high time resolution is to race the electrical signal to be timed against a clock pulse train. A set of superconductive race arbiters determines the outcome of the race at each arbiter location. Simulation and experiment have demonstrated that this type of prescaler produces a digital output corresponding to how far the signal races before being overtaken by a clock signal. So far, we have operated prescaler circuits at clock rates of up to 20 GHz. Feasibility of better than 5-ps time resolution has been demonstrated.

II. TDC Architecture and Principle of Operation

The TDC system consists of a monolithic Nb trilayer circuit on a cryogenically cooled silicon substrate, and an electronics interface to a room-temperature computer. Fig. 1 shows a block diagram of a multi-hit version of the TDC. It consists of two parts: a fine TDC and a coarse TDC.

The coarse TDC is based on an N-bit destructive read-out (DRO) counter operating at a high clock rate. The instantaneous value of this counter can be captured and saved while the counter continues to run at high speed. The time resolution of this coarse TDC is just equal to the clock period of the counter clock. To date, we have demonstrated robust 33 GHz multi-hit operation of this coarse TDC [5].

The fine TDC is based on an analog prescaler. Josephson Transmission Lines (JTLs) are used to transfer Single Flux Quantum (SFQ) pulses with a delay adjusted by JTL bias currents. With properly adjusted delays, RSFQ logic gates are used to resolve each event pulse-front with extremely high accuracy. The TDC time resolution is equal to a clock period divided by the number of prescaler bins. This analog prescaler allows us to achieve a time resolution of 5 ps for a ten-bin prescaler operating at 20 GHz.

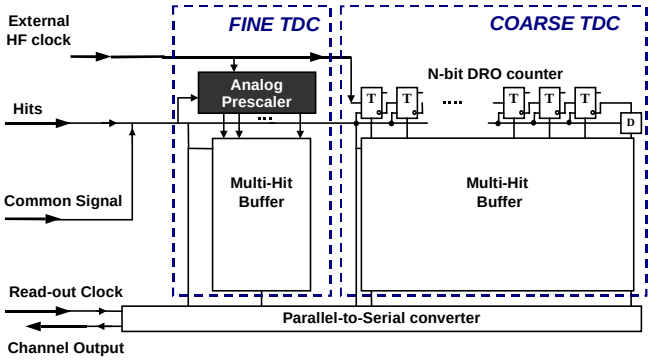

Fig. 1. In this multi-hit superconductive TDC, the signal ("Hits") and clock pulse train are applied to both a fine and a coarse TDC. The fine TDC consists of an analog prescaler and a multi-hit buffer. The coarse TDC consists of an N-bit DRO counter and a multi-hit buffer. The fine and coarse TDC outputs are sent to a parallel-to-serial converter for single-line data output.

Buffers can be used in both fine and coarse TDC units to produce multi-hit capability. A serial-to-parallel converter is used to produce a single bit-serial output stream.

III. Prescaler Architectures and Simulations

Several different prescaler architectures have been investigated. Each of these designs is based on the interaction of signal and clock pulses. The progression of our designs has been towards more compact prescalers to enable monolithic TDC fabrication on 5-mm substrates. Eventually, we will choose the design that optimizes circuit complexity without sacrificing the performance goal of 5 ps resolution.

There are two basic classes of prescaler architecture. The first class utilizes the racing of signal and clock pulses along parallel JTL paths. The two paths are designed so each has a different SFQ pulse propagation velocity, thereby realizing an SFQ time vernier. Because of the different velocities of these lines, one SFQ pulse always "catches up" to the other. The position along the delay line where this event occurs is directly related to the initial delay between two pulses.

The second class of prescalers is based on the simultaneity of signal and clock pulses on *anti-parallel* JTL paths. With the appropriate delays applied, the position where the signal and clock pulses coincide is again directly related to the initial delay between signal and clock pulses.

A. Prescaler Based on Synchronizer

The architecture for the synchronizer-based prescaler was originally developed for a phase modulation/demodulation analog-to-digital converter [6]. Its original purpose was to increase the resolution of the demodulation process. In the TDC prescaler, the synchronizer has a similar function. A time vernier enables higher resolution by racing the signal with the clock pulses. A set of synchronizers encodes the spatial information of these racing conditions. The resolution can be increased by a numerical factor equal to the number of synchronizer bins.

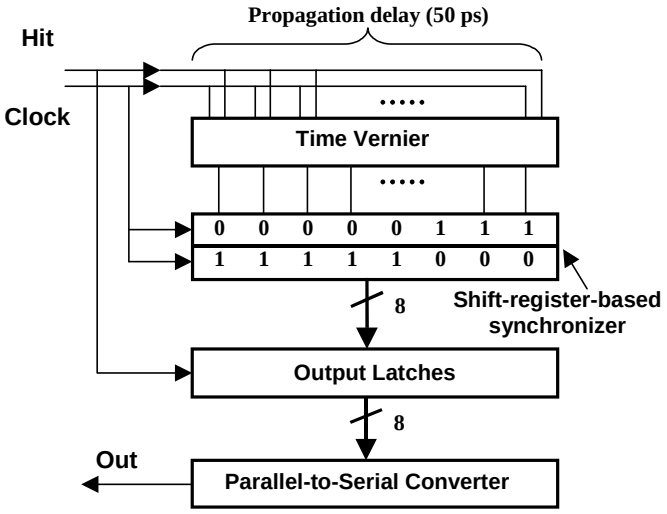

Fig. 2. This block diagram shows the architecture of the shift-register-based analog prescaler. A time vernier converts the initial delay between clock and hit pulses to a spatial position, and a synchronizer acts as a race arbiter to encode the precedence of clock and hit pulses.

Fig. 2 shows a block diagram of an eight-bin synchronizer-based prescaler. The time vernier is set so the 20 GHz clock pulses travel through all of the bins in 50 ps. The basic synchronizer has four shift registers stages per bin. The shift register stages in each bin are operated in pairs by a two-phase clock. The first and third shift register cells operate on one clock phase (CLK_1); the second and fourth cells are clocked by another phase (CLK_2).

If the data pulse arrives at a particular shift register before the clock, the data (hit) pulse is clocked out to the next shift-register stage at the arrival of the clock pulse. It can be seen that in Fig. 2, the clock pulse overtakes the hit pulse between the fifth and sixth bin.

The layout for the four-stage synchronizer circuit is shown in Fig. 3. For this test circuit, the clock pulse train CLK_1 is split; one branch is decimated by a T flip-flop. This CLOCK÷2 pulse train functions as a signal source. For each cell in this circuit, circuit parameters were extracted. A hierarchical electrical model of the prescaler circuit was integrated using the WRSpice circuit analysis package [7], assuming a Josephson current density of 1 kA/cm^2. Simulations were performed using different initial delays and JTL bias values, until the simulated operation of the time vernier and the synchronizer could be verified.

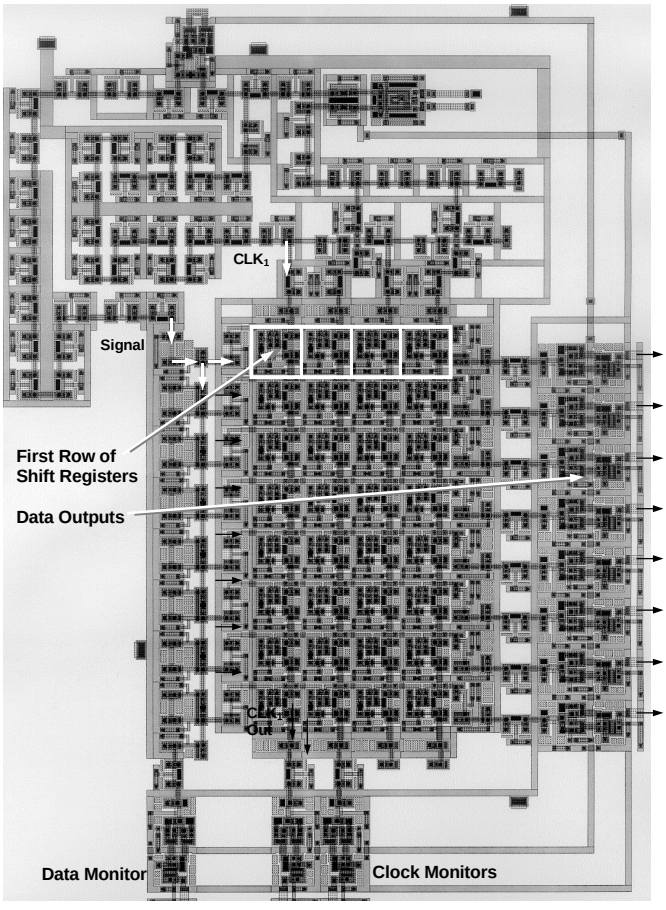

Fig. 3. This layout shows the four-stage synchronizer-based prescaler circuit. It contains eight rows of shift registers. At each row, the signal is split off and raced with pulses from the first clock phase, CLK_1. Data are output in parallel in this design. This circuit contains 526 Josephson junctions.

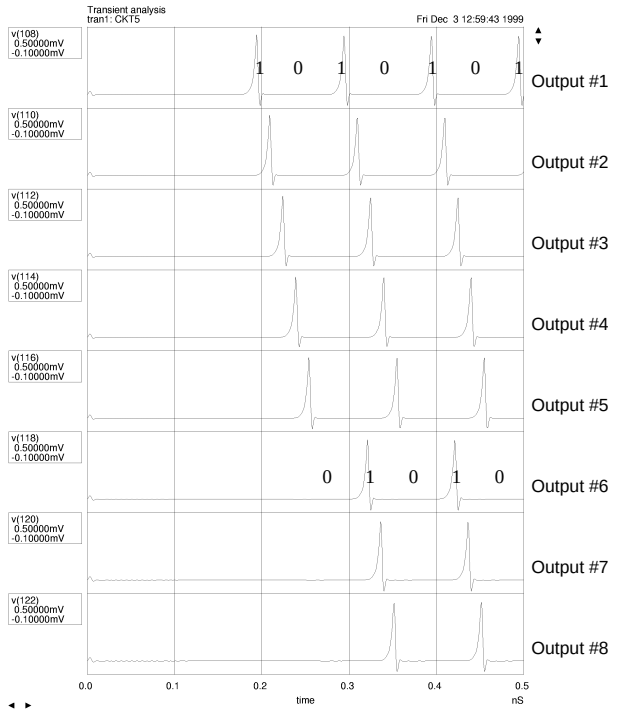

Fig. 4. This set of curves represents a simulation of the circuit shown in Fig. 3. In this particular simulation, the clock pulse overtakes the signal or hit pulse between the fifth and sixth bins, just as in Fig. 2. This corresponds to between 5/8 and 3/4 of the 50 ps clock cycle.

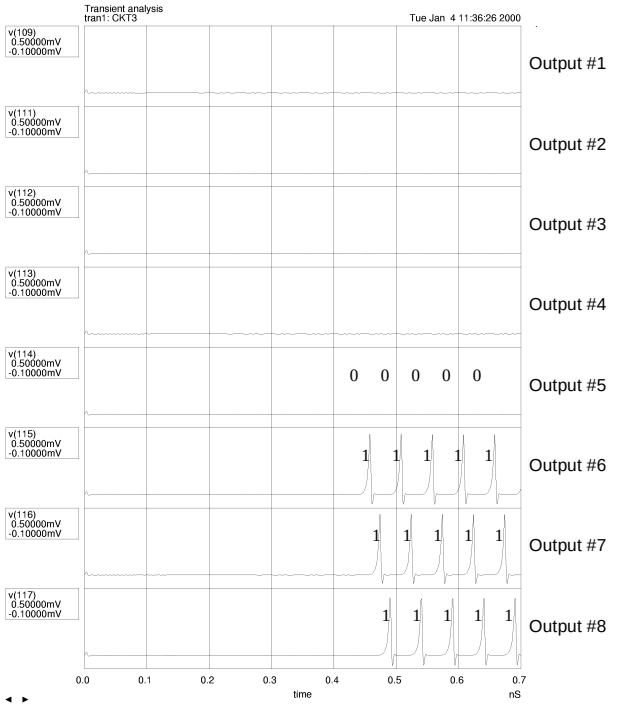

Fig. 5. This simulation shows the first eight of ten outputs of the SRC prescaler. The upper boundary between the "0" and "1" data indicate that the clock overtakes the data between the fifth and sixth rows. (The lower boundary, not shown here, is of no consequence.)

Fig. 4 shows a simulation of the 4-stage prescaler. Signal pulses are launched every 100 ps (two clock periods). Outputs #1-5 have pulse trains of 1 0 1 0 1 … and outputs #6-8 have pulse trains of 0 1 0 1 0. For rows #1-5, the signal precedes the clock; the signal is clocked into the shift register upon clock pulse (CLK_1) arrival. For rows #6-8, the clock arrives first, thereby clocking a "zero" into the register chain. The "zero" gets clocked into the second stage upon CLK_2 arrival.

Fig. 4 clearly shows that each word output is followed by a set of complementary redundant data. The redundant data can be removed by adding a column of destructive read-out flip-flops (called Set-Read-Clear or SRC cells [8]). Simulations show that the (1 1 1 1 1 0 0 0) data are removed; the (0 0 0 0 0 1 1 1) data remain. Adding the SRC cells increases the circuit complexity. Even by removing two (superfluous) stages of the four-stage synchronizers, the junction count for an eight-bin prescaler is still increased from 526 to 607.

B. Compact Prescaler Based on Set-Reset-Clear Flip-Flop

The SRC flip-flop can be used as a race arbiter between its set and clear inputs. One can dispense with the synchronizer (shift-register) cells, and build a more compact prescaler with only a time vernier and SRC cells. For a ten-bin prescaler, this results in a reduction of junction count from 707 to 471. This prescaler allows pulse arrival at twice the rate of synchronizer-based versions. In the simulation of Fig. 5, signal pulses are launched at 50-ps intervals. The 20-GHz clock overtakes the signal pulse at the boundary between "0s" in the top rows and "1s" in the bottom rows. The point at which the clock overtakes the signal in Fig. 5 is therefore between the fifth and sixth rows, or between 25 and 30 ps.

C. Compact Prescaler Based On Dynamic AND Gates

A prescaler based on dynamic AND gates [9] has also been designed, simulated, and fabricated. This design is substantially less complex and more compact than the others are. Fig. 6 shows a schematic of this new prescaler. The CLOCK and HIT pulses move *toward* each other from opposite ends of the two delay lines. These delay lines are connected with dynamic AND gates. The delay, τ, between two AND gates is adjustable to between 2 to 6 ps. The dynamic AND gate has an internal cycle time that should be set to 1.5τ. The gate produces an output pulse if and only if the HIT and CLOCK pulses arrive at the AND-gate input terminals within this time interval. Upon changing the clock frequency, the JTL delay elements must be tuned by adjusting the bias current.

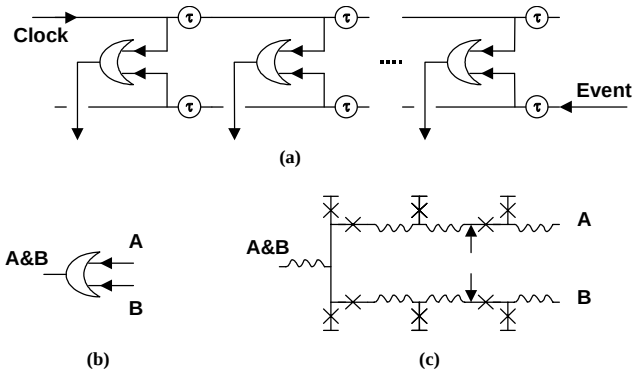

Fig. 6. (a) The dynamic AND prescaler uses anti-parallel pulse propagation. The time vernier is connected to dynamic AND gates. The symbol and schematic for this novel gate are shown respectively in (b) and (c).

III. Experimental Results

A. Functional Test Results

The four-stage synchronizer-based prescaler was functionally tested. Fig. 7 shows the low-speed test results of this circuit. All output bins were monitored with T flip-flop SFQ/DC converters; thus the switching of output voltage state between 0 and ~150 mV indicates the output "1". The preset value of the variable delay was 20 ps. Immediately after the "HITs", bins 1 – 3 produce output "0", while bins 5 – 8 produce output "1". (Bin 4 is in the "gray zone" and outputs either "0" or "1.") This indicates that the delay between CLOCK and HIT pulses is between 3/8 and 4/8 of 50 ps. By changing the DC bias current on the variable delay JTL line, we have observed the expected response from the prescaler outputs. The bias current of the time vernier affects the SFQ pulse propagation time, thus changing the prescaler resolution. In this experiment, we observed our prescaler fully operational at up to 30 ps propagation time, which corresponds to 4-ps resolution.

B. High-Speed Test Results

To test the synchronizer prescaler at high speed, the clock was decimated by a T flip-flop. The CLOCK÷2 signal was used as a HIT signal. Fig. 8 shows that by scanning the bias current on the HIT delay line with a saw-tooth signal and applying a 20-GHz clock, we were able to observe a family of so-called "eye diagrams". At any given value of delay, some of the bin toggle monitors generated "ones" (single lines), while the rest of them produced "zeros" (double lines). The equidistant positions of the thresholds reflect the high linearity of the delay line with respect to the race arbiter. The clearly open "eye" between the double lines indicates the absence of a significant error rate. The transition between "1" and "0" (the so-called gray zone) is about 2 ps. This makes a 5-ps time resolution goal more than feasible.

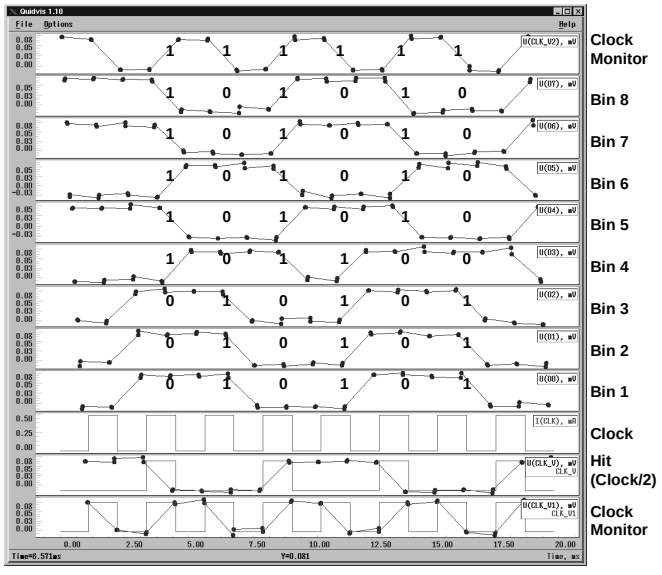

Fig. 7. These experimental results show the correct functionality of the synchronizer prescaler. Total time vernier delay is 50 ps. The value of the HIT/CLOCK delay is 20 ps. The initial output is 11100000, or 3/8 of 50 ps. Then, the complement data 00001111 are output.

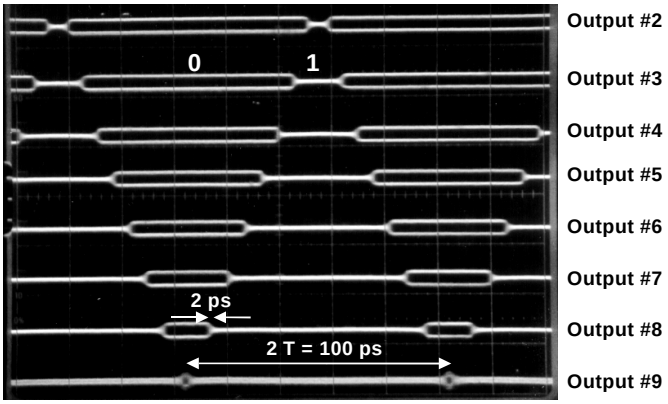

Fig. 8. This test of the synchronizer-based prescaler at 20 GHz was done by modulating the HIT/CLOCK delay with a saw-tooth waveform. Only the middle eight of the ten bins are displayed in this oscilloscope photograph.

IV. Conclusion

We have designed, fabricated and tested several types of prescaler circuits for use in a time-to-digital converter system. For a Josephson current density of 1 kA/cm^2, our simulations and experimental results verify that Niobium-based prescaler circuits can operate at 20-GHz clock rates. Our high-speed results have shown that one of our prescaler circuits can divide a 50-ps clock period by a factor of 10. This results in a 5-ps TDC resolution, limited primarily by the width of the SFQ pulses. By increasing the Josephson current density to 10 kA/cm^2, the resolution could be improved by roughly a factor of 3, limited mainly by clock and signal jitter.

The various types of prescaler circuits have different levels of circuit complexity. Tradeoffs between circuit performance and operational margins will help to determine the ultimate choice of which circuit to use in our TDC system.

References

[1] This TDC, Model #TDC-14/8, is marketed by Siegmund Scientific, 1848 Tice Valley Blvd., Walnut Creek, California 94595, (925) 296-0848.

[2] For a review, c.f. K. Likharev and V. Semenov, "RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol. 1, pp. 3-28, March 1992.

[3] The standard HYPRES process uses a current density of 1000 A/cm^2 and a minimum junction diameter of 3 μm. Nb process flow and design rules are available from HYPRES, 175 Clearbrook Road, Elmsford, NY 10523, or visit the HYPRES web site at http://www.hypres.com/.

[4] S. Pagano, et al., "Radiation hardness of Josephson junctions and superconductive digital Devices," *Extended Abstracts of ISEC'97*, Berlin, Germany, vol. 2, pp. 263-265, Jun. 1997.

[5] A. F. Kirichenko, S. Sarwana O. Mukhanov, I. V. Vernik, Y. M. Zhang, J. Kang, and J. Vogt, "RSFQ time digitizing system," this conference.

[6] S. V. Rylov, L. A. Bunz, D. V. Gaidarenko, M. A. Fisher, R. P. Robertazzi and O. A. Mukhanov, "High-resolution ADC system," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2649-2652, June 1997.

[7] WRspice, ©Whiteley Research Incorporated, 456 Flora Vista Ave., Sunnyvale, CA 94086.

[8] This gate is essentially half of the B flip-flop. S. V. Polonsky, V. K. Semenov and A. F. Kirichenko, "Single flux quantum B Flip-Flop and its possible applications," *IEEE Trans. Appl. Supercond.*, Vol. 4, pp. 667-670, Nov. 1991.

[9] “A superconductive high-resolution time-to-digital converter,” O. A. Mukhanov and A. F. Kirichenko, *ISEC’99*, Berkeley CA, pp.353-355, Jun. 1999.