Superconducting Switching Amplifiers for High Speed Digital Data Links

Amol Inamdar, Sergey Rylov, Saad Sarwana, and Deepnarayan Gupta

***Abstract*—In a superconductor digital-RF transmitter, the power amplifier chain can be implemented in hybrid temperature, hybrid technology environment, where the superconductor switching amplifier forms the first stage of the amplification chain. We have designed several flavors of SQUID based switching amplifiers, each targeted for different power output and speed. One of the amplifiers is a differential amplifier featuring dynamic equalization. To minimize the intersymbol interference, the amplifier employs a pre-emphasis technique, thereby compensating for the bandwidth limitations of the channel. The differential output voltage of this amplifier is 16 mV at low speed (200 Mbps), which rolls off to 2 mV at 16 Gbps data rate, for an "1100" pattern (no consecutive transitions on the input data sequence). For high speed operation of the SQUID amplifiers, simultaneous switching of SQUIDs is desired to reduce the output rise and fall times. Hence, in another amplifier design, called the Differential H-Tree Amplifier, the SQUIDs are arranged in an "H-tree" structure, to equalize the propagation delay of the control signal to each SQUID. The amplifier's differential output voltage is 8 mV at low speed (200 Mbps), and rolls off to 2 mV at 10 Gbps data rate. A third type of amplifier is a differential SFQ-to-DC amplifier; it consists of a pair of synchronously driven SFQ-to-DC converters that produce complementary positive and negative voltage waveforms respectively. The differential output voltage of this amplifier is 0.8 mV, and it can be operated at very high speeds. Moreover, the complexity of this amplifier enables it to be yielded in higher critical current density process. Both, the speed and the output voltage scale as the square root of the process critical current density.**

***Index Terms*—Differential amplifiers, rapid single flux quantum (RSFQ) logic, SQUIDS, superconductor integrated circuits.**

I. Introduction

HIGH SPEED digital interface to semiconductor electronics has been a severe limiting factor for superconductor integrated circuits. While the low switching energy per junction (in the range of 10^{-18} Joules) results in low power dissipation at very high speeds, it stands out as a major disadvantage from the data links perspective. Consequently, the digital output from superconductor electronics needs further amplification. Lack of very high speed amplifiers limits the operating speed of this, otherwise, very high speed technology.

Manuscript received August 26, 2008. First published June 30, 2009; current version published July 10, 2009. This work was supported in part by the Space and Naval Warfare Systems Command Contract N00039-04-C-2134.

A. Inamdar, S. Sarwana, and D. Gupta are with HYPRES, Inc., Elmsford, NY 10523 USA (e-mail: ainamdar@hypres.com).

S. Rylov is with IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TASC.2009.2018413

Some of the initial amplifier designs involved ac-driven SFQ-to-latch converters [1], [2] that suffered from ac-current induced crosstalk and ground ripple. On the other hand, the dc-driven HUFFLEs [3] were free of crosstalk problems, but were limited to operations below 4 GHz. Single-ended unipolar amplifier based on a stack of dc SQUIDs are described in [4], [5], and their adaptations for receiver outputs is described in [6].

In this paper, we describe several flavors of amplifiers based on stack of dc SQUIDs. First, we describe the improvements to the unipolar single-ended digital amplifier described in [6], and further introduce amplifiers with bipolar outputs; both, single-ended and differential versions are described. Most commercial high-speed amplifiers have differential outputs because of their common mode noise rejection properties. Two layout configurations for SQUID stacks are discussed: one containing SQUIDs arranged in linear fashion, resulting in sequential switching and hence relatively low speed, whereas the other containing SQUIDs arranged in H-tree fashion, resulting in simultaneous switching and therefore high speeds.

II. Improved Unipolar Single-Ended Amplifier

The original amplifier consists of RS flip-flop based SFQ-to-DC converter (RSDCA), followed by a JTL current amplifier, and bunch of series connected SQUIDs, driven by multiple control inductors [6]. On receiving the Set pulse, the RSDCA outputs a stream of fluxons constituting a low voltage output, which drives the SQUID stack into the resistive state, resulting in an output voltage $(\mathrm{V_L})$ at the load. The speed at which the RSDCA injects the fluxons, determines the rise time of the amplifier. The Reset pulse stops the stream of fluxons, and the fall time of the amplifier is determined by the L/R relaxation time constant of the control inductor. In the improved amplifier (Fig. 1), a fluxon doubler circuit doubles the voltage output of the RSDCA, thereby reducing the rise time in half.

The fluxon doubler is a splitter followed by a confluence buffer, splitting the stream of fluxons and recombining the two streams, to double the output voltage. The fall time is also reduced to half, by appropriately adjusting the value of the resistance. Consequently, the improved architecture doubles the speed of the digital amplifier. The output amplitude in a 50 ohm load is measured to be 3.5 mV at 0.2 Gbps, which drops down to 2 mV at 2.5 Gbps (Fig. 2).

III. Amplifier With Bipolar Outputs

A. Bipolar Single-Ended Digital Amplifier

This bipolar single-ended digital amplifier consists of two SQUID stacks, connected in series between two voltage rails

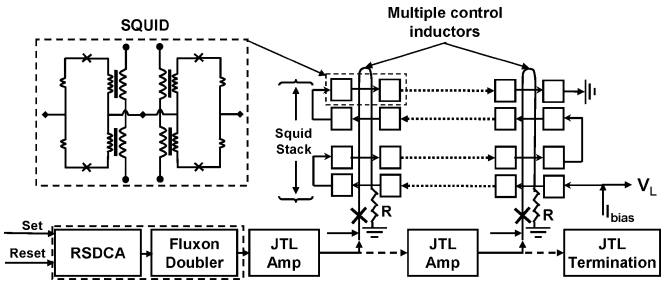

Fig. 1. Functional schematic of improved unipolar single-ended digital amplifier based on SQUIDs modulated by multiple control inductors coupling flux into the SQUID loops.

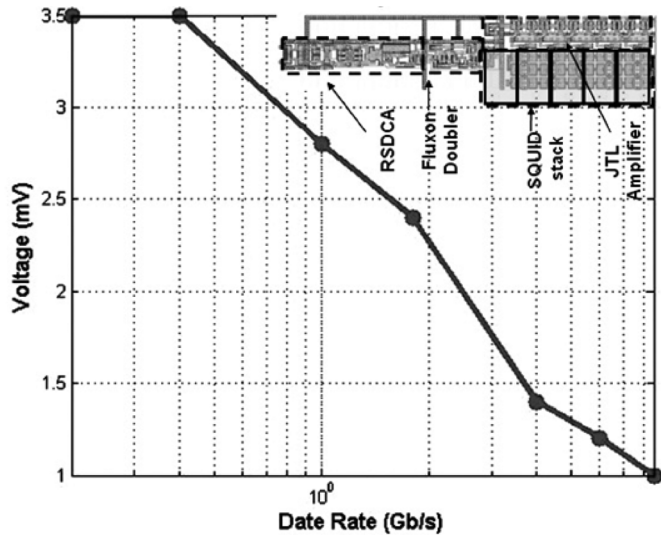

Fig. 2. High speed response for the improved unipolar single-ended digital amplifier. Inset shows the layout of the amplifier.

$(+\mathrm{V}_0, -\mathrm{V}_0)$. These stacks work as switches: "closed" when the SQUIDs are in the superconducting state, and "open" when they are driven to the resistive state by passing a current through a magnetically-coupled control inductor (Fig. 3). SET and RESET control signals drive the SQUID stacks in a push-pull fashion, such that, when one of the stack is driven into the resistive state, the other stack is driven out of the resistive state and into the superconductive state. The stack in which fluxons are injected in the same direction as $\mathrm{I}_{\mathrm{bias}}$, sets up a current in the control inductor, driving the stack in resistive state, whereas the stack in which fluxons are injected in opposite direction to $\mathrm{I}_{\mathrm{bias}}$, resets the current in control inductor, driving the other stack into superconductive state. The applied voltage across the superconductive stack is carried to the load $(\mathrm{V_L} = \pm\mathrm{V}_0)$; the voltage across the resistive stack is always $2\mathrm{V}_0$.

When a control current is applied, the critical current of a SQUID is suppressed by a factor of α. Upon exceeding this suppressed critical current $(\mathrm{I_{C\,min}} = \alpha \mathrm{I_C})$, the current through the resistive SQUID stack $(\mathrm{I_{RS}})$ follows a non-linear IV curve; its shape being a function of the SQUID parameters and the total number (N) of SQUIDs in the stack. To maintain the other SQUID stack in the superconductive state, the current through it must remain below the critical current $(\mathrm{I_C})$. The current through superconductive stack $(\mathrm{I_{SS}})$ is the sum of the current through the

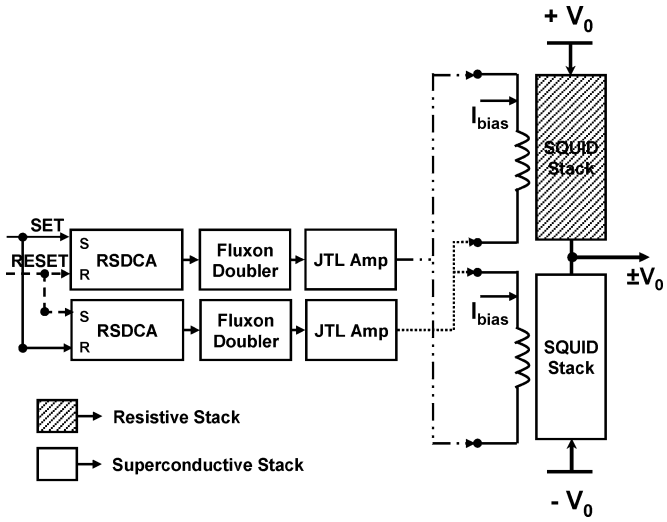

Fig. 3. Functional schematic of the bipolar single-ended digital amplifier. The structure consists of two SQUID stacks driven by control signals SET and RESET such that one stack remains in resistive state while the other stack remains in superconductive state. The superconductive stack provides a loss less path from the applied voltage to the output.

resistive stack $(\mathrm{I_{RS}})$ and the load current $(\mathrm{I_L})$ flowing through a load resistor $(\mathrm{R_L})$ connected to the output:

$$I_{SS} = I_L + I_{RS} < I_C \tag{1}$$

$$I_{RS} \geq I_{C\,\min} = \alpha I_C \tag{2}$$

Therefore, the maximum load current $(\mathrm{I_{L\,max}})$ and voltage $(\mathrm{V_{L\,max}})$ can be written as

$$I_{L\,\max} = I_{SS\,\max} - I_{RS\,\min} < I_C(1-\alpha) \tag{3}$$

$$V_{L\,\max} = R_L I_{L\,\max} < I_C R_L (1-\alpha) \tag{4}$$

Thus, the total number of SQUIDS (N) in a stack, required to obtain the maximum output voltage, is given by:

$$N = \frac{2V_{L\,\max}}{V_{SQ}(I_{ctrl}, I_{RS})}, \tag{5}$$

where, $\mathrm{V_{SQ}}$ is the voltage of a single SQUID, biased at current $\mathrm{I_{RS}}$, with a control current of $\mathrm{I_{ctrl}}$.

B. Bipolar Differential Digital Amplifier

Fig. 4 shows the architecture of the bipolar differential digital amplifier. The structure includes four squid stacks, grouped in two diagonal pairs of series stacks for the differential outputs. As mentioned earlier, the stacks are driven in and out of resistive state by modulating the current in the control inductor. To obtain a differential output between $-\mathrm{V}_0$ and $+\mathrm{V}_0$, these SQUID-stack switches are placed between two voltage rails ($+\mathrm{V}_0$ and $-\mathrm{V}_0$) as shown in Fig. 4. The two diagonal pairs are driven by complimentary control signals (SET, RESET), ensuring that one diagonal pair of SQUID stack is in the resistive state, whereas the other pair is in the superconductive state, to provide a lossless path for the applied voltages to the two differential outputs. For example, when $\mathrm{SET} = 1$ $(\mathrm{RESET} = 0)$, the diagonally shaded are in the resistive state, so that $\mathrm{V_{L1}} = +\mathrm{V}_0$ and $\mathrm{V_{L2}} = -\mathrm{V}_0$. Reversal of control signals switches the output polarity. To obtain higher voltages, the total number of SQUIDs

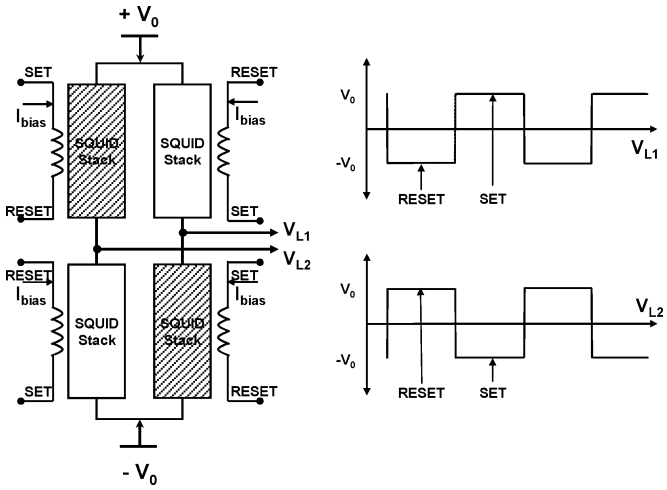

Fig. 4. Functional schematic (left) of bipolar differential digital amplifier. SET, RESET signals chosen to place a diagonal pair of stacks in resistive state while the other diagonal pair in superconductive state. Expected waveforms for the SET, RESET inputs shown on the right.

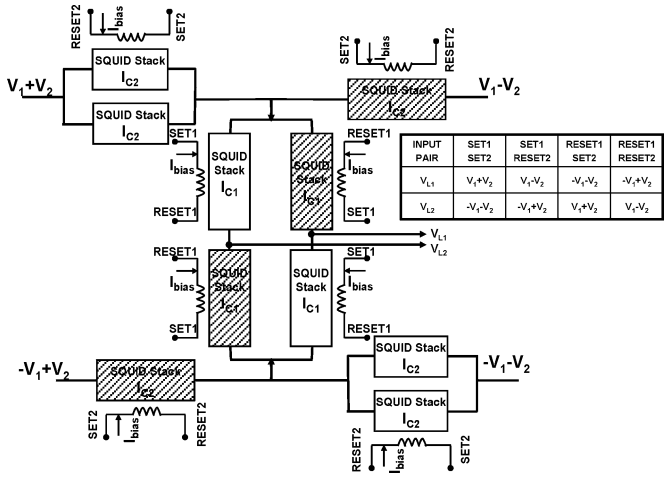

Fig. 6. Differential digital amplifier featuring dynamic equalization. RSDCA and other control circuitry are not shown. Table shows the voltages at respective outputs for different combinations of SET and RESET signals.

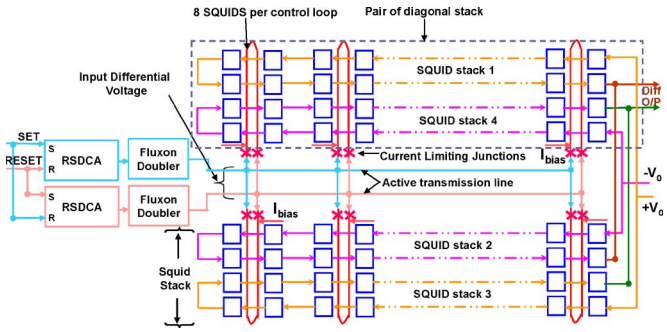

Fig. 5. Schematic of the bipolar differential digital amplifier designed to work in a push-pull configuration with equal rise and fall times.

is increased. while to improve the speed, fewer SQUIDs are coupled per control loop. Furthermore, the SQUID stacks are driven actively between superconductive and resistive states, ensuring equal rise and fall times.

As seen in the schematic (Fig. 5), the RSDCA cells are arranged in push-pull configuration. Depending on the control signal (SET, RESET), the diagonal pair in which fluxons are injected in the direction of bias current goes into the resistive state, whereas the other pair in which the fluxons are injected in the opposite direction to the bias current is driven into the superconductive state. This forced injection of fluxons in the opposite direction, helps reducing the current in the control inductor much faster than the L/R relaxation time, significantly reducing the fall time. The rise and fall times are further reduced by employing multiple control inductors, each coupled to fewer SQUIDs. The amplifier's maximum output voltage depends on the parameters of the SQUIDs, and the total number of SQUIDs used in a stack.

IV. Dynamically Equalized Digital Amplifier

In high speed digital communications, equalization is often employed to compensate for the band limitations of the transmission channel. These bandwidth limitations result in inter symbol interference that cause attenuation of the high frequency components. Moreover, different propagation times for different bit patterns result in pattern dependent skews. These distortions significantly reduce the signal to noise ratio (SNR), thereby complicating detection of the received signal. One method of channel equalization, called pre-emphasis, involves distorting the transmitted waveforms, to pre-compensate for the losses to be incurred in the channel, thus facilitating higher SNR at the receiver. The pre-emphasis driver creates a four-level waveform (strong high, weak high, strong low, and weak low), such that for any transition in the input signal (low to high or high to low), the waveform transitions to the strong voltage, whereas for repeated input data the waveform either transitions from strong to weak voltage or continues to remain in the weak voltage state [7]. Analyzed in frequency domain, pre-emphasis add high frequency components to counteract high frequency attenuation in the transmission channel. For example, a square wave with 50% duty cycle contains only odd harmonics of the fundamental frequency, whereas a square wave with non-50% duty cycle produces both even and odd harmonics of the fundamental frequency. In a pre-emphasis waveform, the extra levels boost at every transition edge, produces an additional pulse in amplitude that contains both odd and even harmonics of the fundamental frequency. These odd and even harmonics of the pre-emphasis pulse add to the frequency spectrum of the original square wave, thereby reducing ISI by counteracting the low-pass-filter response of the transmission channel [8].

The digital amplifier consists of eight SQUID stacks, grouped in four combinations of two series stacks (Fig. 6). A preliminary version of this amplifier has been described in [7]. The current in the control inductors, magnetically coupled to the stacks, is used to modulate the voltage of each of the SQUID stacks. The stacks are driven in push-pull configuration with multiple control inductors per stack. Digital control signals (SET1, RESET1 and SET2, RESET2) are chosen such that a combination of two series stacks is driven into the resistive state, whereas the other two stacks are driven into the superconductive state, providing lossless paths for the applied voltages to the two differential outputs. The amplifier is used to generate

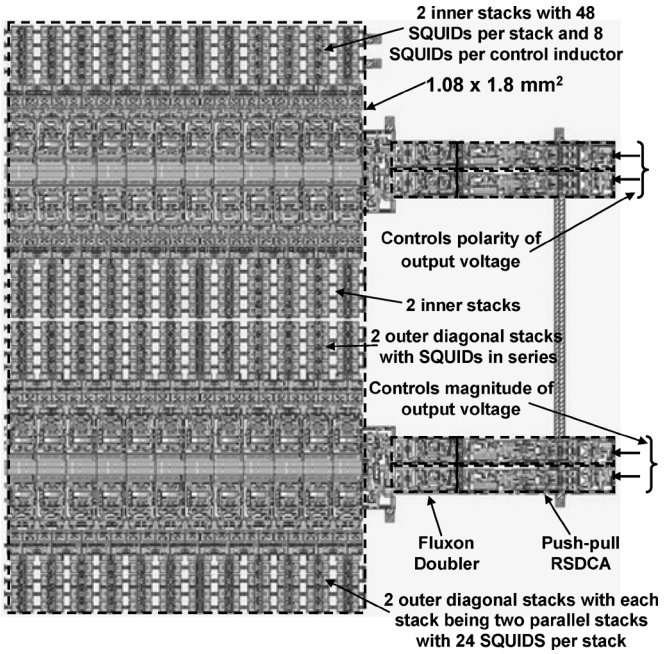

Fig. 7. Layout of differential digital amplifier featuring dynamic equalization.

a four level pre-emphasized waveform. The inner pair of the diagonal SQUID stacks controls the polarity of the output voltage, whereas the outer pair of SQUID stacks controls the magnitude.

The outer stacks operate in a different regime compared to the inner stack; the outer stack needs to be optimized for greater current carrying capability, while the inner stacks for greater voltage drop. It is easy to show that the maximum current the outer stacks can supply to the inner bridge is the difference of $\mathrm{I_{SS(max)}}$ and $\mathrm{I_{RS(min)}}$ of the outer stacks (that would be the case of very small $\mathrm{V_2}$), and progressively less as the difference of $\mathrm{V_1 + V_2}$ and $\mathrm{V_1 - V_2}$ grows (the current in the resistive stack non-linearly increases with increased voltage drop). For maximum voltage, the total current that needs to be supplied by the outer stack is the sum of the suppressed currents of the outer stack ($\mathrm{I_{RS(outer)}}$), the inner stack ($\mathrm{I_{RS(inner)}}$), and the load current ($\mathrm{I_L = V_L/R_L}$). Thus,

$$I_{SS} \geq I_{RS(outer)} + I_{RS(inner)} + I_L < I_{C(outer)} \qquad (6)$$

On the other hand, the outer stacks do not require as much voltage drop as the inner stacks. Hence, it is possible to arrange each stack as a parallel connection of two stacks, each with half the number of SQUIDs, thus keeping the total number of SQUIDs the same. However, the critical current of the SQUIDs in the outer stack need to be larger than that of the inner stacks. If so, one might find that the large current is needed primarily only in the stack connected to strong level (higher voltage port). Hence, by converting only that stack into two parallel stacks, while maintaining the other outer stack as a single series connected stack, the necessary current can be supplied to the load.

A. Layout and Test Results

Fig. 7 shows the layout of the differential digital amplifier featuring dynamic equalization. The SQUID stacks along with the control circuitry occupy 1.08 mm by 1.8 mm area. The inner stacks consist of 48 SQUIDs in series, each with an $\mathrm{I_C}$ of 400 μA. The outer stacks connected to higher voltage rails consists of two parallel stacks, each with 24 SQUIDs and an $\mathrm{I_C}$ of 550 μA, whereas the outer stacks connected to lower voltage rails consists of 48 SQUIDs in series, each with an $\mathrm{I_C}$ of 550 μA.

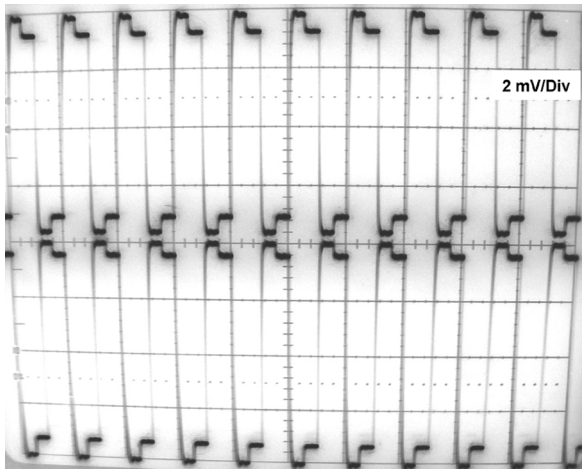

Fig. 8. Low speed test result for the amplifier with pre-emphasis. The amplifier exhibits 16 mV differential output.

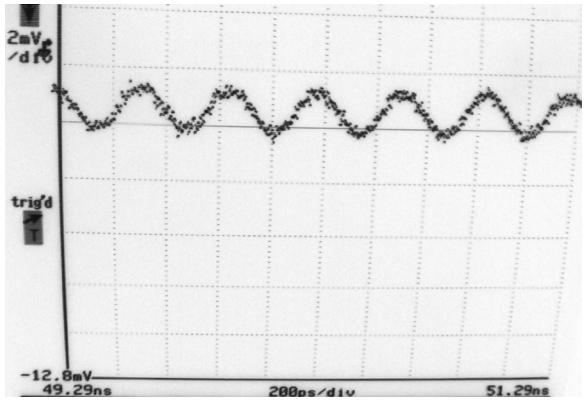

Fig. 9. High speed test result for the amplifier with pre-emphasis. Only one output is shown in the figure. Input data applied without consecutive transition ("1100" pattern).

A 5-mm chip containing the differential digital amplifier was fabricated using the standard HYPRES Nb process for Jc of 4.5 $\mathrm{kA/cm^2}$ [9], and tested in a standard 40-pin test probe in liquid helium. Fig. 8 shows the low speed test of the amplifier exhibiting a pre-emphasized waveform with 16 mV differential output. The gain of the pre-emphasis peaks can be adjusted by adjusting the applied rail voltages. Fig. 9 shows the high speed test result for the differential amplifier. Only a single output is shown. To clearly observe the pre-emphasis steps a "1100" data pattern (no consecutive transition) was applied at the input. Thus a 3 GHz NRZ output corresponds to 12 Gbps input data rate. The single-ended output is 1.4 mV translating to 2.8 mV differential output. Fig. 10 shows the voltage as a function of data rate for the differential amplifier featuring dynamic equalization. The 3-dB cutoff point corresponds to 11.46 mV a 4 Gbps. Although the amplifier is not designed for very high speeds, it could be operated up to 16 Gbps data rate with a 2 mV differential output, for a data pattern without consecutive transitions on the input.

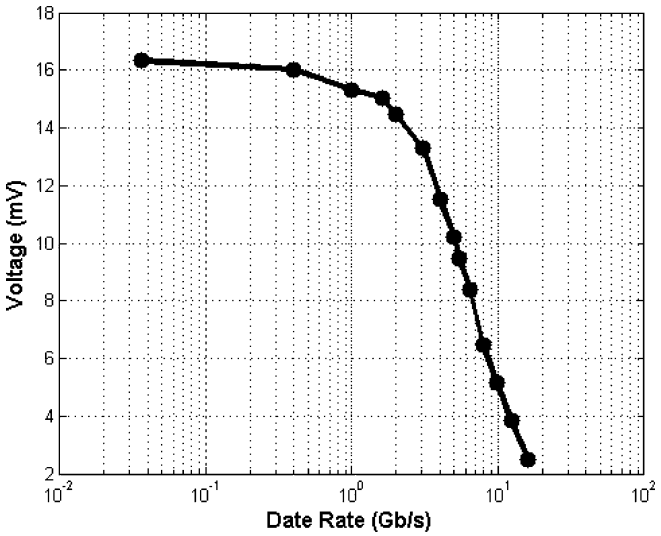

Fig. 10. High speed response of the differential amplifier featuring dynamic equalization.

To better characterize the amplifier, measurements for open eye and for random input pattern need to be performed.

V. High Speed H-Tree Amplifier

In the differential amplifier featuring dynamic equalization, the SQUID stack is a linear array of SQUIDs, modulated by multiple control inductors, each coupling to few SQUIDs. Since a linear active transmission line with splitters is used to feed the control inductors, a small propagation delay is incurred in the transmission of the control signal to the individual control inductors. The delay causes the SQUIDs to switch states sequentially, resulting in a rise time that might be too high for very high speed data links. To enable higher speed operation, the SQUIDs can be arranged in an "H-tree" structure, equalizing the propagation delay of the control signal to each SQUID. This is expected to increase the synchronization of switching in the SQUIDs by reducing or eliminating signal skew. There is now a longer latency, but since all the SQUIDs switch state simultaneously, the rising and falling edges of the voltage waveform will be much sharper. Additionally, in this design, each control inductor drives only two SQUIDs per loop, proportionally reducing the total fluxons required to modulate the SQUIDs.

Although the H-Tree driver can permit equalizing the propagation delay of the control signal, a major drawback of the structure is its size, which grows very large even for small number of SQUIDs. The fewer SQUIDs in turn results in relatively lower voltages. To obtain higher voltages while keeping the size within limits, we replaced the individual heads of each "H" by a triangular structure, with 10 SQUIDs per structure. The propagation delay of the control signal for each SQUID is designed to be constant by ensuring that the sum of horizontal and vertical delays for each SQUID is the same. More specifically, we intentionally added some delays on the vertical paths to the control loop, which are progressively reduced by a unit delay for each of the successive SQUID loop, thus compensating for the delay incurred on the horizontal path. The schematic of the H-Tree

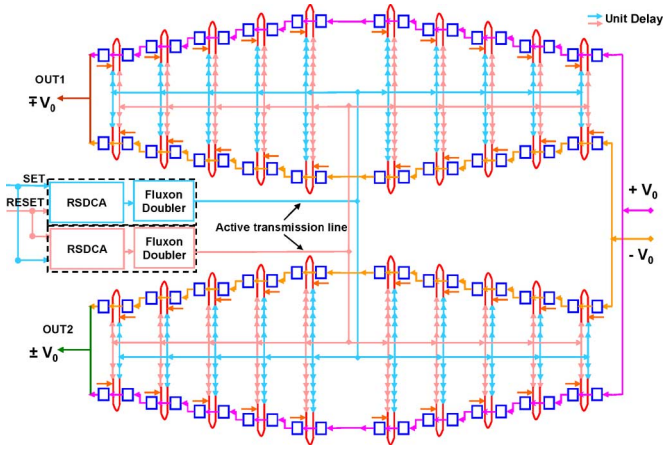

Fig. 11. Schematic of the H-Tree amplifier with triangular heads. Equalized propagation time of the control signal to each SQUID.

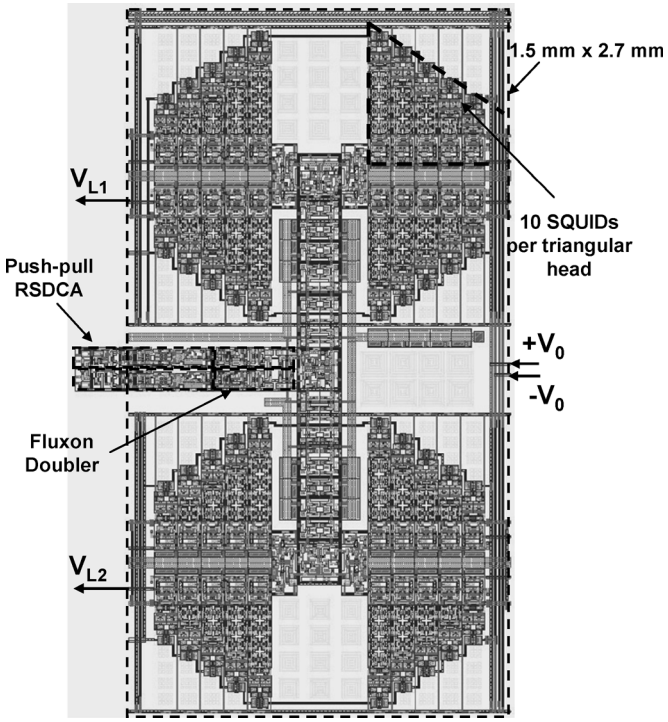

Fig. 12. Layout of half H-Tree amplifier.

driver with triangular heads is shown in Fig. 11. As the control signal reaches the center of the "H", it starts splitting into vertical and horizontal directions. The arrowhead shown in the schematic corresponds to one unit delay. The architecture of the H-Tree driver is same as the one shown in Fig. 4.

For better yield and to lower the bias current requirements, we initially laid out a "Half H-Tree" amplifier (Fig. 12). The SQUID stacks along with the control circuitry occupy 1.5 mm by 2.7 mm area. Each triangular section consists of five control loops with two SQUIDs per loop. Each stack consists of twenty SQUIDs connected in series, with an I_C of 400 μA.

A 5-mm chip containing the Half H-Tree differential digital amplifier was fabricated using the HYPRES 4.5 kA/cm^2 process [9] and tested in liquid helium. Fig. 13 shows the low speed test results with 8 mV differential output voltage.

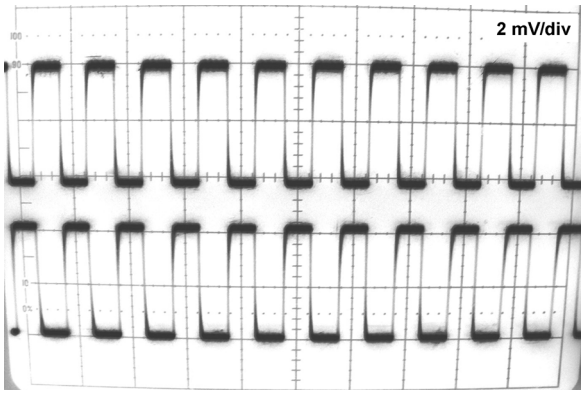

Fig. 13. Low speed test result for the Half H-Tree amplifier. The amplifier exhibits 8 mV differential output.

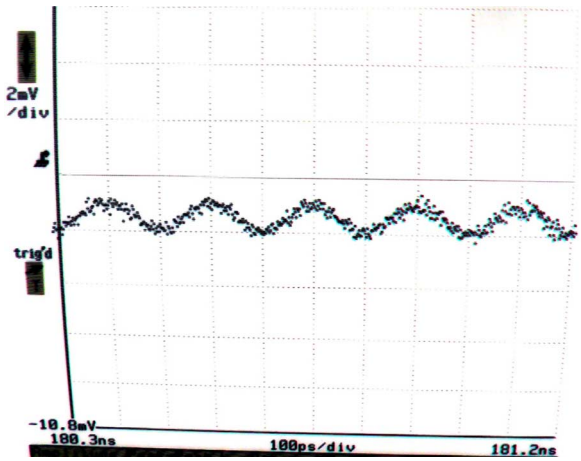

Fig. 14. High speed test result for the half H-Tree amplifier. Only one of the two outputs shown in the figure.

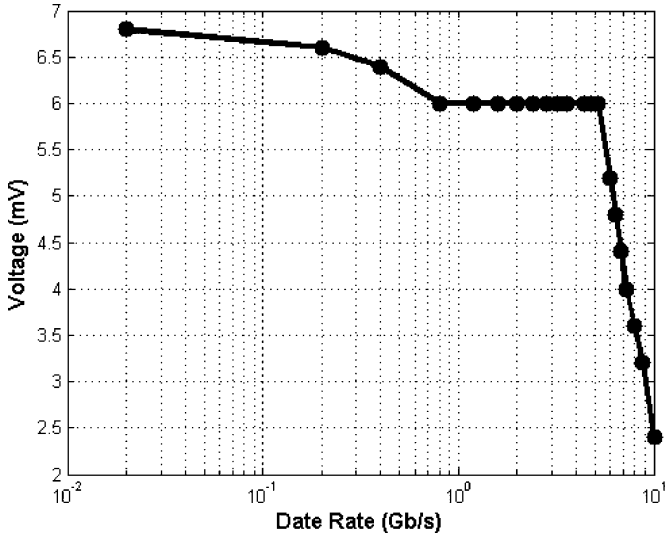

Fig. 15. High speed response of the half H-Tree differential amplifier.

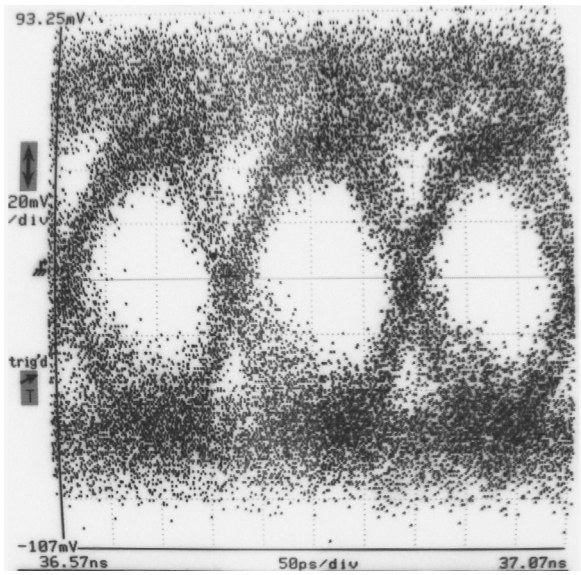

Fig. 16. Eye-diagram measurement for the half H-Tree amplifier. Only one of the differential outputs is followed by the SHF LNA.

Fig. 14 shows the high speed test result for the differential amplifier. Only a single output is shown. A 5 GHz NRZ output corresponds to a 10 Gbps input data rate. The output voltage is 1.2 mV corresponding to differential output voltage of 2.4 mV. Fig. 15 shows the voltage as a function of data rate for the Half H-Tree differential amplifier. The 3-dB cutoff corresponds to 4.67 mV at 6.5 Gbps. The amplifier operates up to 10 Gbps with a 2 mV differential output voltage. However, the speed of the amplifier is lower than expected. The low speed is attributed to higher parasitics in the control loop, which will be improved in future revisions.

Moreover, since fewer fluxons are needed to modulate the SQUIDs, the RSDCA that pumps continuous stream of fluxons can be eliminated, and instead fixed number of fluxons can be injected for each of the SET and RESET signals.

Another set of high speed measurements were carried out to plot the eye-diagram. One of the two H-Tree outputs is further amplified by a cold low noise amplifier (LNA) which was placed about 18 inches from the H-Tree amplifier by modifying our existing cryoprobe. The measurements were performed using two different LNAs, a MITEQ (AFS4-00100800-16-0P-4-CR 0.5–8 GHz), and a SHF (105C 65 KHz–30 GHz) amplifier. The probe height was adjusted such that the H-Tree amplifier was immersed in liquid Helium, while the LNA was located just above the liquid Helium surface, at a temperature of 8 K. The gain of the two LNAs were 45 dB and 33 dB respectively, with a gain flatness of ± 1 dB in this range.

Fig. 16 shows the eye diagram for the half H-Tree amplifier. In this experiment, a single H-Tree output was further amplified by the SHF LNA. The eye-diagram is plotted for a PRBS23 (pseudorandom-binary-sequence, which repeats after $2^{23} - 1$ bits) input, applied at 6 Gbps. The above measurements include contributions due to cable losses, which can be significant, especially at higher data rates. Hence, the H-Tree amplifier can be driven at higher data rates than that suggested by the above eye-diagram measurements. Moreover, using differential outputs will double the voltage swing, and thus, the vertical height of the open-eye.

VI. Ultrafast Differential SFQ-to-DC Digital Amplifier

This differential amplifier consists of a pair of synchronously driven SFQ-to-DC drivers that produce complementary positive and negative voltage waveforms respectively. The SFQ-to-DC converter is the fastest of all superconductor output amplifiers and can be driven to about 16 Gbps input data rate for the HYPRES's first generation fabrication process, with critical current density $J_C = 1\ kA/cm^2$. Typically a high-speed (10 Gbps or more) digital link requires about 1 mV voltage swing for reliable operation with low error rates. Therefore, a single SFQ-to-DC converter with its small output voltage (about 200 μV for the $J_C = 1\ kA/cm^2$ and about 400 μV for the $J_C = 4.5\ kA/cm^2$ fabrication processes) is not used as a high speed output amplifier. By constructing a differential amplifier, we not only double the output voltage swing, but also improve quality of the digital link by rejecting common mode noise. Moreover, both, the output voltage and switching speed scale as the square root of J_C. While the current low-yield state-of-the-art superconductor IC foundry makes it difficult to yield complex circuits in a high J_C process, this simple differential amplifier ($\sim$50 junctions) can be fabricated with higher yield in a high J_C technology. We plan to integrate this amplifier with other complex circuits in a hybrid-J_C process, where the low complexity circuits are fabricated in a high J_C process, but the more complex circuits are fabricated in the low J_C process. Circuit components with different J_Cs can be fabricated on separate chips connected together on a multi-chip-module (MCM) [11] or using the multi-J_C fabrication process that permits components with different J_C to be fabricated on the same chip [12]. We recently demonstrated the proof-of-concept for both the configurations. Thus, we expect the voltage of the differential SFQ-to-DC digital amplifier to be about 800 μV at 32 Gbps for the 4.5 kA/cm^2 process and 1.6 mV at 64 Gbps for the 20 kA/cm^2 processes. Such voltages will be sufficient to drive a second stage cooled semiconductor amplifier. Furthermore, due to its reduced complexity, this ultrafast, differential amplifier consumes proportionately less power and area on chip.

The RS flip-flop (RSFF) (Fig. 17) acts as a pulse density to pulse width modulator (PDM-to-PWM) that takes in SFQ pulses as control inputs (SET and RESET) and produces a PWM current in its storage loop. In response to a SET pulse, the RSFF stores single flux quanta in the storage inductor in form of equivalent current (Φ_0/L), representing state '1'. Absence of the flux quanta represents state '0' and is achieved by the reset pulse at the input. The SFQ-to-DC converter utilizes the current in the storage loop to modulate the SQUID in and out of resistive state and to generate a unipolar output voltage. In state '0', the SQUID is in superconducting state and produces a zero voltage drop, whereas in state '1', the SQUID is in resistive state, producing DC voltage at the output.

The polarity of the output voltage depends on the polarity of the bias current applied to the SQUID. In response to a positive bias current (I_{bias}), a positive output voltage is obtained, whereas a negative bias current ($-I_{bias}$) results in an negative output voltage. However, in response to a negative bias current, the preceding RS flip-flop is optimized differently for proper operation. More specifically, the bias of the JTL stage before the quantizing loop is scaled up to compensate the effect of the negative bias current.

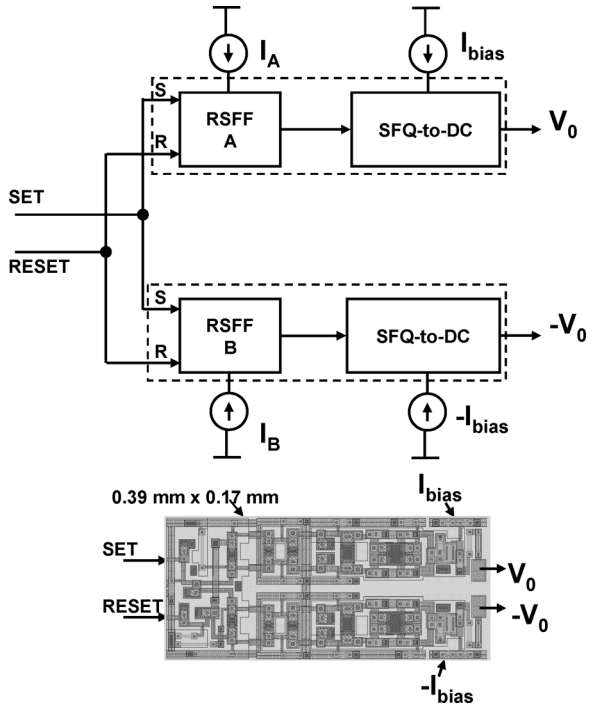

Fig. 17. Differential SFQ-to-DC digital amplifier. Inset below shows the layout of the amplifier.

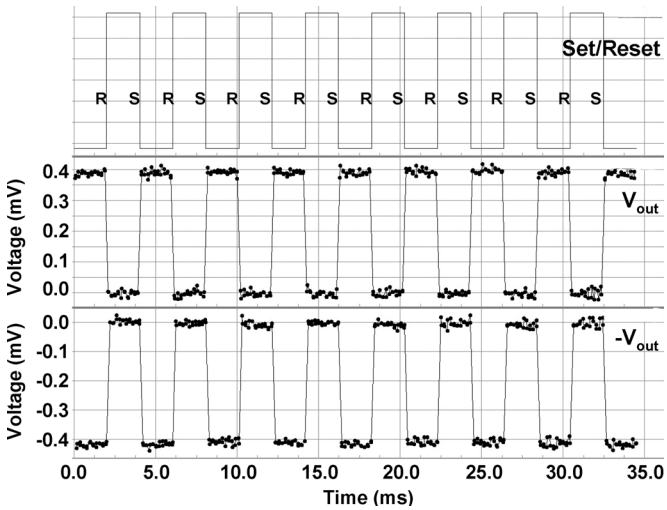

Fig. 18. Low speed test result for differential SFQ-to-DC digital amplifier. The amplifier exhibits 800 μV differential output.

The inset in Fig. 17 shows the layout of the differential SFQ-to-DC amplifier. The driver occupies an area of 0.39 mm $\times$ 0.17 mm. Fig. 18 shows the low speed test results for differential outputs from a 5 mm chip containing the amplifier, and fabricated using the 4.5 kA/cm^2 process. The testing was performed using the automated test setup Octopux [10]. The amplifier produces 800 μV differential output voltage.

To test this amplifier at high speed, a single SFQ-to-DC output is further amplified by a MITEQ amplifier with a 40 dB

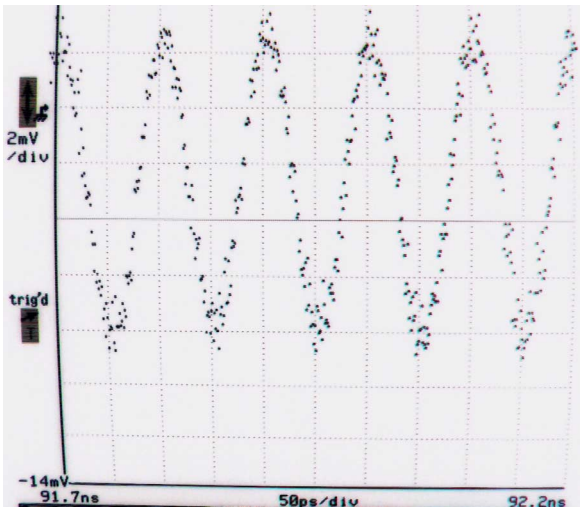

Fig. 19. High speed test result for the differential SFQ-to-DC amplifier. A single output is further amplified by a MITEQ amplifier with a 40 dB gain at room temperature.

TABLE I
AMPLIFIER SUMMARY

Amplifier	Voltage (mV)	Speed (Gbps)	Area mm^2	Type
Single-Ended	2	4	0.2 x 0.94	Unipolar
Pre-Emphasis	2	16	1.08 x 1.8	Bipolar, Differential
Half H-Tree	2	10	1.5 x 2.7	Bipolar, Differential
Trans-impedance	0.8	32 (expected)	0.39 x 0.17	Unipolar, Differential

gain at room temperature. Fig. 19 shows the test result for a 10 GHz NRZ output, corresponding to 20 Gbps input data rate.

The output is 11 mV corresponding to 110 μV of SFQ-to-DC single-ended output. A significant part of the voltage roll off is attributed to the noise in the MITEQ amplifier and to the losses in the cables.

While other superconducting amplifiers based on SQUID stacks are capable of delivering a larger output voltage, they are limited in speed, occupy larger area, and draw excessive bias current. In contrast, the differential SFQ-to-DC amplifier occupies smaller area, draws significantly lower bias current, and can be fabricated in a high-J_C process, enabling high speed operation to a few tens of Gbps, facilitating it use in very high speed data links.

VII. CONCLUSION

We have developed several flavors of switching amplifiers, each optimized for different speed, voltage output, and area. The table below summarizes the amplifier properties (Table I).

ACKNOWLEDGMENT

The authors thank Dmitri Kirichenko and Dr. Alan Kadin for useful discussions, and S. Tolpygo, D. Yohannes, R. Hunt, J. Vivalda, and D. Donnelly for fabricating the chips. A. Inamdar thanks Prof. V. K. Semenov for numerous valuable suggestions and advice.

REFERENCES

[1] J. X. Przybysz, J. H. Kang, S. S. Martinet, and A. H. Worsham, "Interface circuits for input and output of gigabit per second data," in *Extended Abstracts of ISEC'95*, Nagoya, Japan, Sep. 1995, pp. 304–306.

[2] M. Suzuki, M. Maezawa, H. Takato, H. Nakagawa, F. Hirayama, S. Kiryu, M. Aoyagi, T. Sekigawa, and A. Shoji, "An interface circuit for a Josephson—CMOS hybrid digital system," *IEEE Trans. Applied Superconductivity*, vol. 9, pp. 3314–3317, June 1999.

[3] D. F. Schneider, J. C. Lin, S. V. Polonsky, and V. K. Semenov, "Broadband interfacing of superconducting digital systems to room temperature electronics," *IEEE Trans. Appl. Superconductivity*, vol. 5, pp. 3152–3155, June 1995.

[4] O. A. Mukhanov, S. R. Rylov, D. V. Gaidarenko, N. B. Dubash, and V. V. Borzenets, "Josephson output interfaces for RSFQ circuits," *IEEE Trans. Applied Superconductivity*, vol. 7, pp. 2826–2831, June 1997.

[5] Y. Hashimoto, S. Yorozu, T. Miyazaki, Y. Kameda, H. Suzuki, and N. Yoshikawa, "Implementation and experimental evaluation of a cryocooled system prototype for high-throughput SFQ digital application," *IEEE Trans. Appl. Superconductivity*, vol. 17, pp. 546–551, June 2007.

[6] D. Gupta, T. V. Filippov, A. F. Kirichenko, D. E. Kirichenko, I. V. Vernik, A. Sahu, S. Sarwana, P. Schevchenko, A. Talalaevskii, and O. A. Mukhanov, "Digital channelizing radio frequency receiver," *IEEE Trans. Appl. Superconductivity*, vol. 17, pp. 430–437, June 2007.

[7] O. A. Mukhanov, A. Inamdar, T. V. Filippov, A. Sahu, S. Sarwana, and V. K. Semenov, "Superconductor components for direct digital synthesizer," *IEEE Trans. Appl. Superconductivity*, vol. 17, pp. 416–421, June 2007.

[8] Maxim Application Note 643, Pre-Emphasis Improves RS-485 Communications [Online]. Available: http://www.maxim-ic.com/an643

[9] The standard HYPRES, Niobium Integrated Circuit Fabrication Process The process flow and design rules are available online [Online]. Available: http://www.hypres.com

[10] D. Y. Zinoviev and Y. A. Polyakov, "Octopux: An advanced automated setup for testing superconductor circuits," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 3240–3243, June 1997.

[11] A. Inamdar, D. Gupta, T. V. Filippov, I. V. Vernik, A. Talalaevskii, A. Sahu, and S. Sarwana, "Superconductor analog to digital converter for SIGINT applications," in *MILCOM-08*, submitted for publication.

[12] D. Yohannes, A. Inamdar, and S. K. Tolpygo, "Hybrid Josephson critical current density process for multi-rate superconductor integrated circuits," *IEEE Trans. Appl. Superconductivity*, June 2009, to appear in.