Quarter-Rate Superconducting Modulator for Improved High Resolution Analog-to-Digital Converter

Amol Inamdar, Sergey Rylov, Anubhav Sahu, Saad Sarwana, and Deepnarayan Gupta

***Abstract*—We describe the design of a new oversampled analog-to-digital converter (ADC) based on phase modulation-demodulation (PMD) architecture. In a PMD ADC, the analog input signal modulates the phase of a periodic stream of fluxons applied to a modulator circuit for subsequent demodulation in a clocked synchronizer circuit to produce a digital code. The new modulator provides a way to quadruple the average fluxon transport rate, and hence the input dynamic range, by replacing the single junction interferometer with a high-speed symmetric divide-by-4 circuit. The divider acts as a 1:4 asynchronous demultiplexer which distributes incoming fluxons among its four quarter-rate outputs. This four-fold rate reduction, at the modulator output, allows one to increase the ADC maximum input slew rate to 2 fluxons per clock period, achieving 2 additional bits of resolution at the same sampling clock frequency. We have designed and fabricated a quarter-rate ADC front-end and present low frequency test results for the same. The ADC comprises a quarter-rate quantizer which has been successfully tested at an input frequency of 81.92 GHz.**

***Index Terms*—Analog-to-digital converter (ADC), delta modulator, rapid single flux quantum (RSFQ) logic, superconductor integrated circuits.**

I. Introduction

THE relentless quest for higher performance of analog-to-digital converters (ADCs) is fundamental to progress in communications, radar, high-speed instrumentation, and sensor applications. For many applications, ADCs are the critical elements that define the architecture and the performance capabilities of the entire system. Ultrafast switching speed, low power, natural quantization of magnetic flux, quantum accuracy, and low noise of cryogenic superconductor circuits enable fast and accurate data conversion between the analog and digital domains. Based on rapid single-flux quantum (RSFQ) logic, these integrated circuits are capable of achieving performance levels unattainable by any other technology [1]. One of the most critical parameters to characterize the performance of an ADC is its dynamic range. To obtain higher dynamic range, one needs to either increase the maximum signal that can be digitized or decrease the quantization noise. The largest signal amplitude for a delta ADC, which measures the time derivative of the analog signal rather than signal amplitude itself, is inversely proportional to frequency. Therefore, the critical parameter is the maximum slew rate. It defines the maximum value the input signal is allowed to change in each sampling interval. To decrease the quantization noise, one can use a multi-channel synchronizer, which effectively subdivides the clock period, measuring the pulse position more precisely in time [2]. Functionally, this multi-channel synchronizer increases the number of quantization levels. It would appear that the quantization noise can be made arbitrarily smaller by simply increasing the number of synchronizer channels. But this is not true. The thermal noise limits the maximum number of channels that one can use to reduce the clock period before it is no longer significant. The thermal noise has the effect of changing the threshold of the quantizer and thus manifests itself as a source of jitter. For a slowly slewing signal, a small change in threshold can cause a large change in phase. Hence, to minimize the jitter and increase the dynamic range, one needs to increase the slew rate limit of the ADC.

The existing architecture of the phase modulation-demodulation (PMD) ADC with a single junction quantizer [2] uses a two channel synchronizer, the design and results of which have been extensively evaluated and reported [3]. Although minor improvements in design are still possible, for substantial improvement of dynamic range (DR), one must increase the frequency of the sampling clock or increase the number of quantization levels. We have invented a novel ADC modulator that allows us to extend the dynamic range by maximizing the number of channels in the synchronizer to achieve higher number of bits.

II. Limitations of Existing Architecture

The basic concept of the delta ADC based on PMD architecture with a single junction quantizer is illustrated in the Fig. 1. In the absence of analog signal, the single junction SQUID quantizer pulses at the carrier frequency (f_{car}) which is determined by the average fluxon transport rate through the modulator (f_{pump}). When an additional analog input signal is coupled to the quantizer loop, the timing of each output pulse gets advanced or retarded in proportion to the derivative of the analog input. This process encodes the signal derivative into SFQ pulse positions, which need to be decoded by measuring the pulse positions against a time reference. Hence, the phase modulated SFQ pulse stream is passed to a phase demodulator (synchronizer), which is a clocked sampling circuit that generates a '1' or a '0' indicating whether or not an SFQ pulse

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A. Inamdar, A. Sahu, S. Sarwana and D. Gupta are with HYPRES, Inc., Elmsford, NY 10523 USA (e-mail: ainamdar@hypres.com).

S. Rylov is with IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

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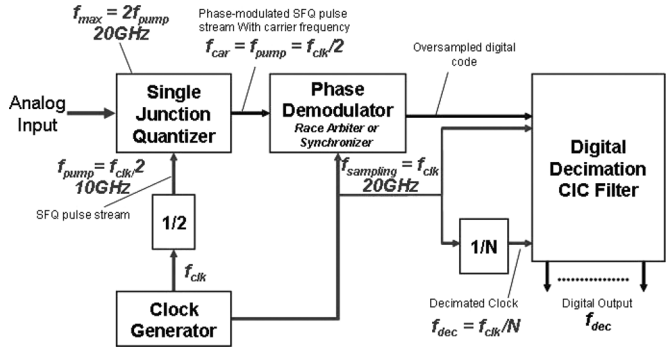

Fig. 1. Original phase modulation-demodulation ADC followed by a digital decimation filter. Numerical values represent ADC parameters for a chip clocked at 20 GHz.

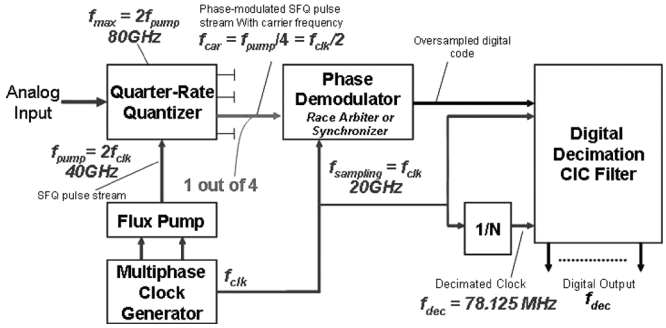

Fig. 2. Multi-rate ADC with quarter-rate quantizer. One out of four quantizer outputs are passed to the synchronizer, which is clocked by one phase of the clock.

arrived during that clock interval. Thus, the synchronizer decodes the pulse position information into numbers (single-bit in the simplest implementation). The oversampled digital data and the corresponding clock from the synchronizer then proceed directly to the decimation filter [4], where it is first integrated at full speed, and then averaged further, reducing the output bandwidth and increasing the effective number of bits. Fig. 1 shows the different frequencies for the standard HYPRES Nb process for Jc equal to 1 $\mathrm{kA/cm^2}$ [5] and a clock frequency of 20 GHz.

The intrinsic slew rate limit for this flux-quantizing ADC is a single flux quantum (Φ_0) in each sampling interval. Therefore, the most natural configuration for the flux pump is to inject fluxons at an average fluxon transport rate (f_{pump}) of $\Phi_0/2$ per sampling period, to accommodate bipolar input signals $\pm\Phi_0/2$ per sampling period. This is done by pumping fluxons at a frequency of $f_{\mathrm{pump}} = f_{\mathrm{clk}}/2$. In order to increase the slew rate limit, the average rate of fluxons through the modulator must be proportionally increased, which necessitates the synchronizer to be clocked at a correspondingly higher frequency which is twice the carrier frequency. The synchronizer clock is further used to clock the digital decimation filter. However, the digital decimation filter being more complex than the ADC itself, forces a limit on the maximum clock speed, which in turn limits the maximum input signal amplitude.

To overcome this limitation, one needs to use a more complex configuration where the quantizer accepts a much higher fluxon pump rate and still outputs the phase modulated pulse stream on a relatively low carrier. The quarter-rate superconducting modulator provides a way to quadruple the average fluxon transport rate, and hence the input dynamic range, by replacing the single junction interferometer with a high-speed symmetric divide-by-4 circuit.

III. Multi-Rate ADC

Similar to the present PMD-ADC with a single junction quantizer, the multi-rate front-end also essentially consists of a clock generator, a flux pump, quantizer, and a synchronizer. However, since the quantizer has been completely changed, some architectural changes need to be implemented. As an example, in the quarter-rate front-end, the single junction quantizer is replaced

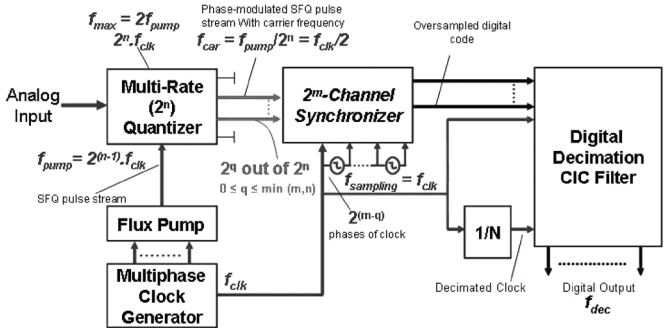

Fig. 3. General architecture of the Multi-rate PMD ADC. The number of phases of the clock used to sample the synchronizer depends on the number of quantizer output carried to the synchronizer.

by a quarter-rate quantizer, which produces four phase modulated SFQ pulse streams at a carrier frequency (f_{car}), 1/4th of the fluxon pump rate (f_{pump}). This necessitates 2 fluxons to be pumped every clock period instead of one in two clock periods (Fig. 2).

More generally, the architecture can be extended to a multi-rate (2^n) quantizer which produces 2^{n} phase modulated pulse streams, 2^{q} of which proceed to a 2^{m}-channel synchronizer (Fig. 3). The phase-modulator accepts a 2^{n} higher fluxon pump rate, and accordingly accommodates an input analog signal with 2^{n} times higher slew rate. Consequently, an improvement of SNR by n-bits (or $2^{2\mathrm{n}}$ in power) compared to the standard architecture can be achieved while still using the same sampling frequency $(f_{sampling})$.

Since the outputs of the quantizer rotate in a cyclical fashion, they are phase locked, and therefore carry correlated signals. Thus, a single output channel, clocked by 2^{m} phases of the clock, is sufficient for phase demodulation. However, since redundant quantizer outputs are available, one can use multiple (2^{q} out of 2^{n}) quantizer outputs, equally divided among 2^{m} synchronizer channels, while being clocked by $2^{(\mathrm{m}-\mathrm{q})}$ phases of the same clock. Since thqe quantization noise on these statistically independent outputs is uncorrelated, additional improvements of the signal-to-noise ratio (SNR) can be obtained by averaging multiple (2^{q} out of 2^{n}) quantizer outputs. However, to do this one needs to use $2^{\mathrm{q}}.2^{\mathrm{m}}$ synchronizer channels, clocked by 2^{m} phases of the clock.

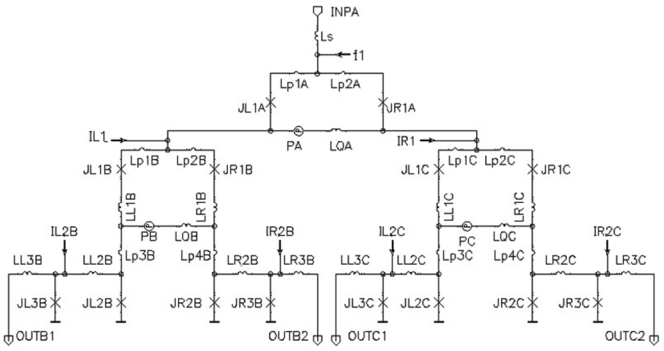

Fig. 4. Quarter-rate quantizer that produces the phase modulated pulse streams on four outputs in a cyclical pattern. The first pulse goes to Output B1, the second to Output C1, the third pulse to Output B2, and the fourth to Output C2. The fifth pulse goes to Output B1 and the pattern continues.

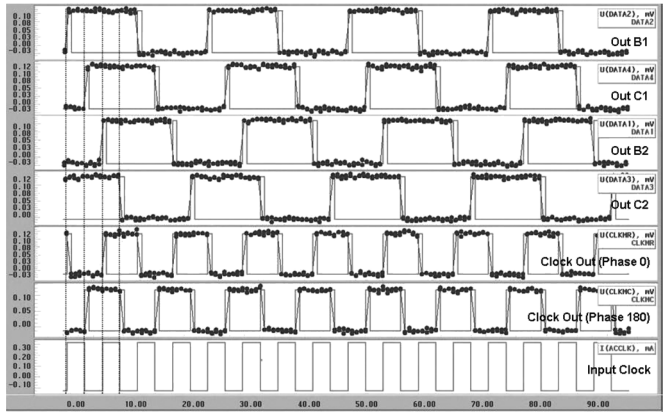

Fig. 5. Low frequency test results for front-end with quarter-rate quantizer. No synchronizers were used. Data from all quantizer outputs are displayed.

A. Quarter-Rate Quantizer

As shown in Fig. 4, the top part of the circuit formed by junctions JL1A and JR1A acts as a 1:2 demultiplexer; distributing pulses arriving at its input alternately to two outputs. Each arm of this demultiplexer is further divided into two arms to form a 1:4 demultiplexer. This quantizer can accept up to four fluxons per clock period, two of which are provided by the flux pump and the remaining two can be provided by the analog input.

The circuit is functionally similar to a tree of toggle flip-flops with complementary outputs (TFFC); each TFFC distributes pulses arriving at its input alternately to two outputs. However the quarter-rate quantizer has some significant advantages over the tree of toggle flip-flops. In case of TFFC, the fastest switching rate is equal to the input rate, whereas in the present case the incoming signal directly divides between the two arms, so that the fastest switching rate is half the input rate. Also unlike TFFC in which asymmetry between two arms is created using a current bias which may lead to unequal switching thresholds, this circuit uses a phase bias to make the switching threshold of each arm perfectly equal. This phase bias (PA, PB and PC in Fig. 4) is implemented as an inductive coupling which can be externally tuned, with the nominal value of π in phase or $\Phi_0/2$ in flux.

The inductances LQA, LQB, LQC act as quantizing inductances. In the top arm, junction JR1A is initially biased by the phase source with the loop phase being equal to π. An input signal of Φ_0 switches the already biased junction JR1A, implying a 2π leap that reverses the direction of circulating current in the quantizing inductance LQA. Junction JL1A is now biased with the loop phase being equal to—π. In the bottom left demultiplexer, junctions JR1B and JL2B are initially biased with the loop phase being equal to π. The switching of JR1A above triggers the switching of the biased junctions in the bottom left demultiplexer giving an output at outB1. This also reverses the direction of circulating current in the quantizing inductance LQB, so as to bias the opposite pair of junctions. The next incoming fluxon now switches Junctions JL1A, triggering a similar sequence of switching in the bottom right demultiplexer such that an output appears at OutC1. The next incoming fluxon delivers an output at outB2 and the subsequent fluxon on outC2 respectively. The circuit thus responds to each incoming fluxon by delivering an output at one of the four channels in a cyclical fashion.

This four-fold rate reduction, at a single modulator output channel, allows one to increase the ADC maximum input slew rate to 2 fluxons per clock period i.e., 4 times higher than the slew rate limit of the PMD-ADC with a single junction quantizer. Consequently, the thermal noise induced jitter of the quarter-rate ADC is reduced by a factor of four. For example, assuming a noise density of 1 $\mu\Phi_0/\sqrt{\text{Hz}}$ and a bandwidth of 10 GHz, the rms noise amplitude is 0.1 flux quantum per clock period. At a slew rate of half flux quantum per clock period, the thermal noise induced jitter is $0.1/0.5 = 0.2$ of the clock period. This results in a 20 ps jitter for a 10 GHz clock allowing one to use a maximum of 5 channels in the synchronizer. On the contrary, slewing at a rate of two fluxons per clock period results in a 5 ps jitter for a 10 GHz clock, assuming the noise density remains the same. This in turn allows one to use 20 channels in the synchronizer. This four fold increase in the number of synchronizer channels results in a 2-bit increase in the SNR.

IV. Test Results

A. Low Frequency Testing

A 5-mm chip containing the quarter-rate quantizer was fabricated using the standard HYPRES Nb process for Jc equal to 1 kA/cm2 [5] and tested in a standard 36-pin test probe in liquid helium. Synchronizers were not used in this test design and all four quantizer outputs were carried to the SFQ/dc monitors. The results of low frequency testing of the quantizer are shown in Fig. 5. The testing was performed using the automated test setup Octopux [6].

Outputs phase 0 and phase 180 represent two phases of the input clock, 180 degrees out of phase. These two phases of clock are merged in the flux pump. OutB1, OutB2, OutC1, OutC2, represent the four quantizer outputs. Since analog signal is not applied, the flux pump acts as the only source of input to the quantizer. As seen, the circuit responds to each incoming fluxon by delivering a fluxon on one of the four outputs in a cyclical fashion.

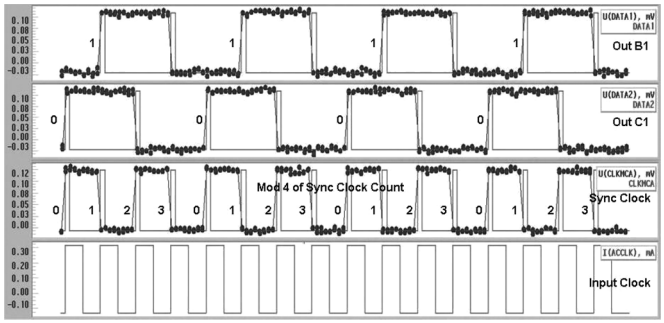

Fig. 6. Low frequency test results for front-end with quarter-rate quantizer. Two of the four outputs from the quantizer are passed to a two-channel synchronizer. No input signal applied. Synchronizer clock is divided into four bins by taking modulo 4 of synchronizer clock count. Data from the quantizer falls in one of the four bins.

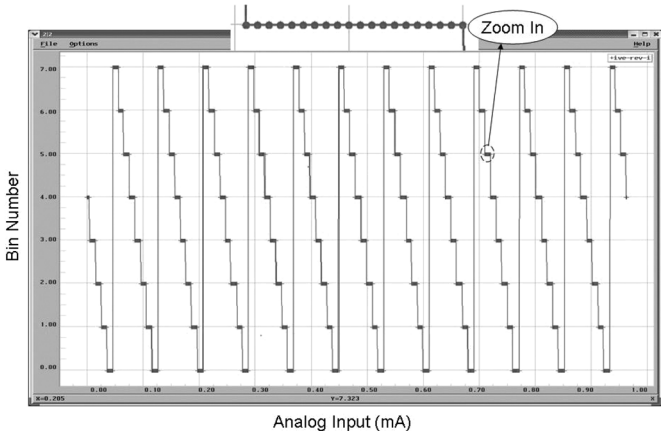

Fig. 7. Low frequency test results for front-end with quarter-rate quantizer and a two-channel synchronizer. A slowly changing ramp is applied as the analog input. Whenever the analog input changes by one flux quantum the outputs change by a single bin at the next synchronizer clock.

To test the front-end at low frequency, a chip was designed with two of the four quantizer outputs going to a 2-channel synchronizer, clocked by one phase of the clock. Fig. 6 shows the test results in the absence of analog input signal. Since the flux pump injects fluxons on the positive and negative edge of the input clock, an output is found on both channels on alternate synchronizer clocks.

As the quantizer has four outputs, the synchronizer clock can be divided into four bins by taking modulo four of the synchronizer clock count. The positive edge transition of the data from both synchronizer channels will lie in one of the four bins (modulo four of the synchronizer clock count). For example, in Fig. 6, the positive edge transitions of OUTB1 lie in bin 1 whereas the positive edge transitions of OUTC1 lie in bin 0. In the absence of analog signal the pulse positions at the output of the phase demodulator are fixed. Hence, the outputs from both the synchronizer channels continue to remain in the same bin and either advance or retard their bin number, in response to the analog input signal.

Fig. 7 shows the test results for a slowly changing ramp applied to the analog input. Since the positive edge transitions of OUTB1 and OUTC1 lie in one of the four bins, the output corresponding to the data from both the channels has been decoded

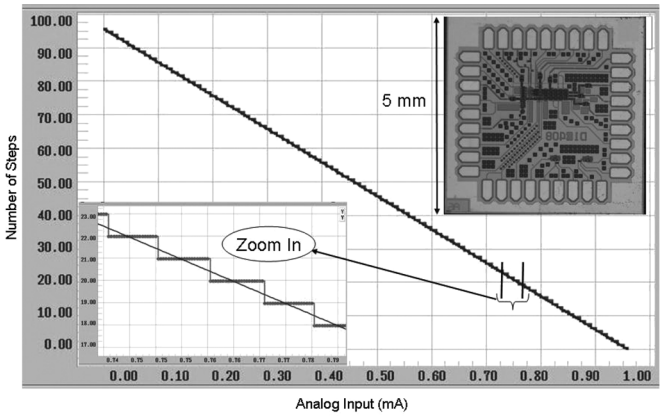

Fig. 8. Signal reconstruction from the quarter-rate front-end. A slowly changing ramp is applied as the analog input. The inset shows the photograph of the chip, comprising the quarter-rate quantizer and a two-channel synchronizer.

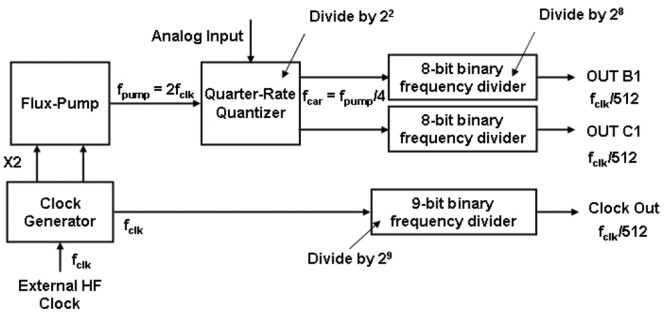

Fig. 9. Block diagram of a chip for high frequency testing of the quarter-rate quantizer.

into 8 bins. For example, the positive edge transition of both channels lying in bin 0 corresponds to output bin 0. One channel in bin 0 and other in bin 1 corresponds to output bin 1 whereas both channels in bin 1 corresponds to output bin 2 and so on. As seen in the inset shown, the output repeatedly falls in the same bin until it receives a fluxon from the analog input. On receiving a fluxon from the analog input the output changes its bin number. As the input signal is changing very slowly, the outputs change by a single bin. The shift in bin position of an output channel equals the number of fluxons injected in the quantizer by the analog input. Hence, the total number of switching due to input signal can be calculated by summing the differences in the bin positions of the output channel. Fig. 8 shows reconstruction of the output data from the synchronizer against the applied ramp.

B. High Frequency Testing

We designed a chip to test the quarter-rate quantizer at high frequency. Fig. 9 shows the block diagram of the same. To enable displaying the data outputs on a scope, their output frequency was decimated by an 8-bit binary counter. Since both phases of the clock are fed to the flux pump, they act as frequency doublers. The quarter-rate quantizer divides the input frequency by four to give a total decimation ratio of 2^9 with respect to the input clock frequency. Similarly one phase of the clock is decimated with a 9-bit binary counter to give the

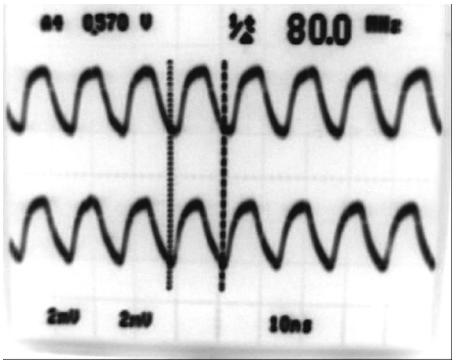

Fig. 10. Oscilloscope traces showing high frequency operation of the quarter-rate quantizer. External clock is applied at a frequency of 40.96 GHz, implying an input frequency of 81.92 GHz to the quantizer. Bottom trace represents the decimated clock output whereas the top trace represents one of the decimated data outputs.

Fig. 11. High Frequency test results for the quarter-rate quantizer. Input clock frequency is 20.48 GHz. In the left figure, bottom trace represents the decimated clock output whereas the top trace represents one of the decimated data outputs. The right figure shows the frequency spectrum of the decimated data output for a span of 20 MHz with the center frequency being 40 MHz. No analog input is applied.

total decimation ratio of 2^9. To obtain the maximum operable frequency of the modulator, an increasingly higher clock signal was applied to the quantizer, with no analog input. In the absence of analog signal, the maximum flux transport rate (f_{max}) is equal to twice the frequency of the external clock signal $(f_{\max} = 2f_{\rm clk})$. Our first goal was to achieve $f_{\max} = 80$ GHz. We increased the external clock frequency and observed the clock and data outputs after the frequency divider. Fig. 10 shows one of the data outputs (B1) and the clock output for an external clock frequency, $f_{\rm clk} = 40.96$ GHz, corresponding to $f_{\max} = 81.92$ GHz.

Although the quarter-rate quantizer itself continued to work at frequencies greater than 81.92 GHz, the losses in cables/connectors supplying the external clock did not permit sufficient signal to be applied to the dc/SFQ converter. Therefore, we over-biased the dc/SFQ converter and found the quantizer to be operational up to a fluxon transport rate of 97 GHz. Further high frequency testing was limited by the test equipment.

Figs. 11 and 12 show the frequency spectra of the data output with no analog input and 4 MHz sinusoidal input respectively. The clock frequency in both cases was 20.48 GHz corresponding to a fluxon pump rate of 40.96 GHz. A single peak at 40 MHz is observed in the frequency spectrum in the absence of analog signal.

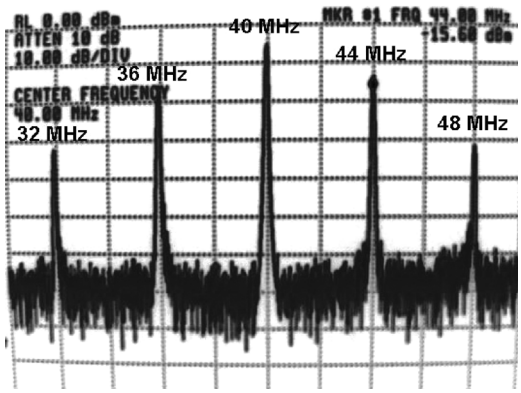

Fig. 12. High frequency test results for the quarter-rate quantizer. Input clock frequency is 20.48 GHz. An input sine wave at 4 MHz is applied.

The frequency spectrum of the data output for a 4 MHz input sine wave contains multiple peaks at $40 \pm 4\mathrm{X}$ MHz, where $\mathrm{X} = 1, 2, 3$, etc.

V. Conclusion

The quarter-rate front-end has been successfully tested at low frequency and is found to be fully operational. The quarter-rate quantizer has been tested at high frequency and is operational up to input frequencies in excess of 80 GHz. This high frequency operation will enable the slew rate limit of the quarter-rate ADC to be four times higher than the ADC with a single junction quantizer. Consequently four times the standard number of channels in a multi-channel synchronizer can be used to give a 2-bit increase in SNR. Increase in SNR can be achieved without increasing the clock frequency of the decimation filter.

Acknowledgment

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