Digital Encoder for RF Transmit Waveform Synthesizer

Amol Inamdar, Deepnarayan Gupta, Saad Sarwana, Anubhav Sahu, and Alan M. Kadin

***Abstract*—We are designing an encoder for conversion of a Nyquist-rate N-bit digital word into a high frequency stream of single-bit data, to enable a novel architecture for a digital waveform synthesizer. The multi-bit to single-bit data conversion is performed by a new encoding scheme called the "staggered thermometer code." Similar to the delta-sigma code, the staggered thermometer code also pushes most of the quantization noise to higher frequencies which can be easily filtered out with a low-pass filter. This encoder, built with elementary RSFQ cells, relies only on the merger of periodic pulse streams of different frequencies, and therefore, is much simpler to implement than a delta-sigma modulator which requires an accumulator and a multi-bit feedback loop. To avoid the permanent energy loss associated with low-pass filtering of high frequency components of the single-bit data stream, we also implement a novel digital circuit that acts as an amplifier by converting the pulse density modulated data stream into a pulse width modulated data stream. This digital amplifier changes the frequency spectrum by concentrating the energy in the fundamental while reducing higher harmonics. We have designed and fabricated a 4-bit and a 7-bit encoder circuit with integrated digital amplifier, and have demonstrated its operation up to a clock speed of 12.8 GHz.**

***Index Terms*—Digital pre-amplifier, digital-RF, digital-to-analog converter, encoder, superconductor integrated circuits.**

I. Introduction

CONVENTIONAL radio frequency (RF) transmission systems for communications and radar are limited, both in performance and cost, by nonlinearities of analog components, such as mixers and amplifiers. Analog component performance varies over temperature, process and age. This is a particular problem for broadband, multi-carrier systems that are increasingly required for modern defense applications. One way to deal with the analog RF components is to eliminate them. However, extending digital technology into the RF domain necessitates ultrafast switching speeds that can be achieved using the Rapid-Single-Flux-Quantum (RSFQ) logic. This will also facilitate development of a digital-RF transmitter architecture that can preserve the digital nature of the signal through part of the power amplifier chain. Fig. 1 contrasts the conventional RF transmitter architecture (a) with digital-RF architecture (b), in which the digital/analog boundary is moved progressively towards the antenna. The digital nature of the rf transmit signal permits the use of highly efficient switching (digital) amplifiers, dramatically improving the power efficiency of the system, while maintaining or improving signal purity.

Manuscript received August 29, 2006. This work was supported in part by the Missile Defense Agency Small Business Technology Transfer Program.

The authors are with HYPRES, Inc., Elmsford, NY 10523 USA (e-mail: ainamdar@hypres.com).

Digital Object Identifier 10.1109/TASC.2007.897317

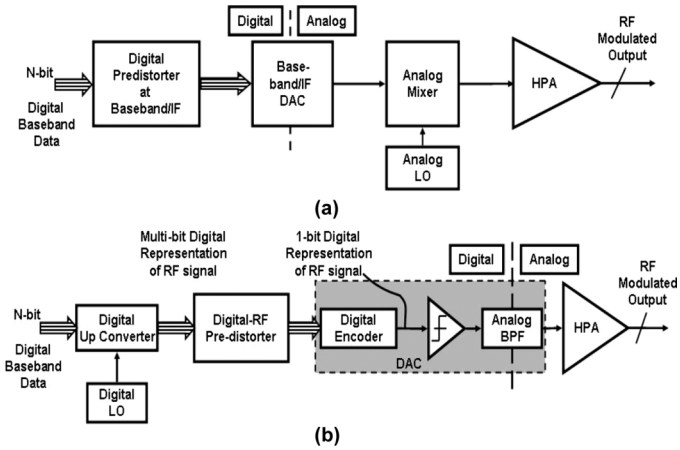

Fig. 1. Conventional and Digital-RF transmitter architectures. (a) Digital-to-analog conversion at baseband or IF. (b) Digital-to-analog conversion at RF with digital-rf encoder.

The block diagram of a digital waveform synthesizer as shown in Fig. 1(b) assumes that one or more digital baseband signals are digitally modulated onto a digital RF carrier to obtain the complete broadband RF signal, represented by an N-bit digital sequence at the Nyquist frequency. This N-bit signal enters the predistorter module, and a predistorted signal at the same sampling rate exits on the right. The N-bit digital-to-analog conversion is composed of an encoder unit that converts the Nyquist-rate N-bit digital words into a high frequency stream of single-bit data; the bandpass filter completes the conversion into the analog domain. The advantage of this approach is that the resultant 1-bit DAC is fundamentally linear but requires extremely high-speed digital circuits. As long as the digital nature of the transmit waveform is maintained, even through the amplification process, the system can remain linear. Here we describe a new encoder algorithm called the "staggered thermometer code" [1] and its corresponding circuit implementation to perform the multi-bit to single-bit conversion. We have also fabricated a 4-bit and 7-bit prototype version of the encoder using the standard HYPRES Nb process for $J_c = 1\ \mathrm{kA/cm^2}$ [2] and report the test results in liquid helium.

II. Staggered Thermometer Code

While there are various methods of generating a 1-bit serial pulse stream from multi-bit binary data, we have developed an encoding scheme—called the *staggered thermometer code* (STC) which lends itself to convenient circuit implementation with existing, proven RSFQ cells. Moreover, the STC has high-frequency quantization noise-shaping properties similar to the widely used delta-sigma code [3].

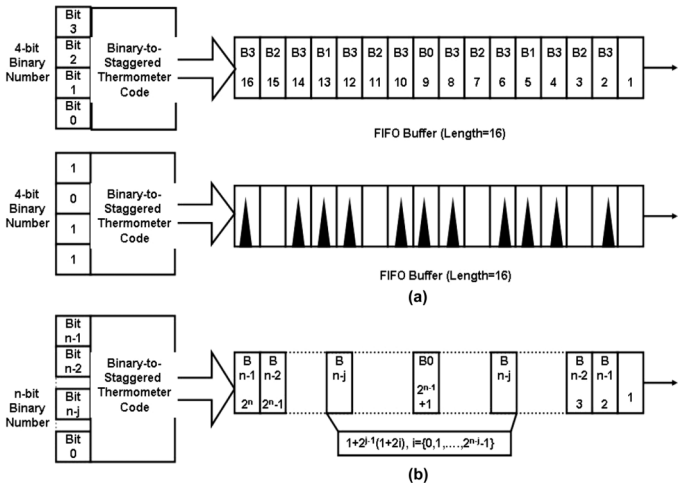

Fig. 2. Example of staggered thermometer code bit assignment algorithm. (Top) The location assignment of a 4-bit binary number to the serial FIFO frame and (a) a numerical example showing the pattern of 11 SFQ pulses in frame length of 16. (b) The location assignment algorithm for an n-bit binary number.

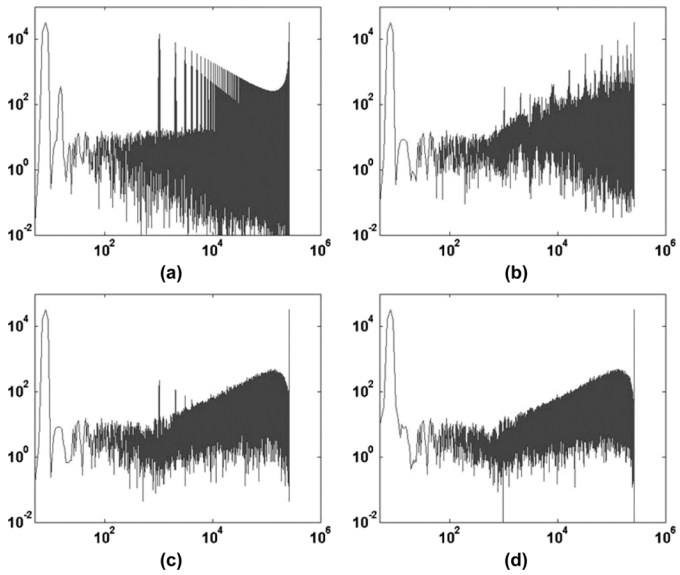

Fig. 3. Simulated frequency spectra (log-log plots) of output pulse trains for an 8-bit sine wave input for (a) conventional thermometer code, (b) staggered thermometer code, (c) delta-sigma with 0th-order interpolator, and (d) delta-sigma with 1st-order interpolator. The sine wave peak is at a frequency of 7 on the left, the input data rate is at 1024, and the output data rate is 2^{18}.

The n-bit encoding consists of a location assignment scheme for '1's and '0's in a sequence of length 2^{n}. The encoder transforms an n-bit binary number of value M into a sequence of equal-weighted 2^{n} 1-bit numbers, where the number of '1's in the sequence is M. For example, a binary word 1011, which has the value eleven (11), should produce a sequence containing 11 '1's and 5 '0's. A standard thermometer code sequence would generate all 11 '1's in series, followed by the 5 '0's. In contrast, the staggered thermometer algorithm distributes the location of these M '1's across the frame of length 2^n, rather than placing them all at the beginning.

The n-bit number is represented as Bits 0 to $(n-1)$. Each bit is assigned a set of locations in the frame of length 2^n, according to its weight (or significance). The most significant bit carries the maximum weight and is assigned 2^{n-1} locations, and each successive significant bit is assigned half as many locations, with the LSB being assigned one location. Together, these fill up 2^n-1 locations, leaving one blank. In the STC algorithm, the MSB, Bit $(n-1)$, occupies every other location, starting from the second location. The next significant bit, Bit $(n-2)$, occupies every 4th location, starting from the third. Bit $(n-j)$ occupies every 2^{j}th location, starting with the $(1+2^{j-1})$th location. Finally, the LSB, Bit 0, occupies the $(1+2^{n-1})$th location.

Fig. 2(a) shows the numerical example of the 4-bit binary number 1011 $(\text{decimal equivalent} = 11)$. The MSB (Bit 3) occupies 8 of the 16 locations starting with the 2nd: locations 2, 4, 6, 8, 10, 12, 14, and 16. The next bit (Bit 2) occupies 4 of the 16 locations starting with the 3rd: locations 3, 7, 11, and 15. The next bit (Bit 1) occupies 2 of the 16 locations starting with the 5th: locations 5 and 13. Finally, the LSB (Bit 0) occupies 1 location, the 9th.

To illustrate the properties of the STC, we show the results of a simple mathematical simulation (in MATLAB), where the frequency spectrum of the output pulse train is computed for the STC and compared in Fig. 3 to that of simulations of the conventional thermometer code (TC) and two examples of delta-sigma $(\Delta\Sigma)$ conversion (SDC). In all of these simulations, the input consists of 1024 samples of an 8-bit offset sine wave with frequency 7 (in arbitrary units), so that 7 periods of the sine wave are present. The output consists of a serial stream of '1's and '0's, at a relative output rate of 2^{18}, corresponding to an output frame length of $2^8 = 256$. The output pulse stream (with a standard Hanning window) is then subject to a fast-Fourier transform (FFT), and the magnitude of the FFT is presented on a log-log plot, showing the frequency spectrum of the output data. All four examples in Fig. 3 show the main sine wave peak on the left, at frequency 7. All of them also show relatively low noise at low frequencies, which generally increases as one moves to increasing frequency, representing noise-shaping. However, there are important differences among the examples that illustrate key aspects of the various converters.

In particular, consider the TC spectrum in Fig. 3(a). Here one clearly sees a set of very large peaks at the frame rate of 1024 and its harmonics. These peaks are due to the strong clustering of '1's and '0's for the TC. If this were to be used in a practical DAC, a very sharp low-pass analog output filter would be required to eliminate these peaks.

In contrast, consider the STC spectrum in Fig. 3(b). The strong clustering of '1's and '0's within the output frames has been replaced with a smoothed distribution across the frames. While peaks at the frame rate and its harmonics are still apparent, they are greatly reduced in power by orders of magnitude, making them much easier to remove with a filter.

The TC and STC spectra are compared in Figs. 3(c) and 3(d) to $\Delta\Sigma$. The $\Delta\Sigma$ first requires a digital interpolation filter to increase the data rate from 1024 to 2^{18}. The simplest 0th-order interpolator (Fig. 3(c)) simply repeats the 8-bit input data at the higher rate; a 1st-order interpolator (Fig. 3(d)) provides linear interpolation between the input data points. Then a 1st-order low-pass $\Delta\Sigma$ algorithm [3] is used to generate the oversampled sequence of '1's and '0's in the output. It is notable that Fig. 3(c) is very similar to Fig. 3(b) up to mid frequency range;

both exhibit peaks of similar magnitude at the data input rate of 1024 (and harmonics). In contrast, this peak is sharply reduced in the $\Delta\Sigma$ output with the higher-order input interpolator shown in Fig. 3(d).

Unlike a $\Delta\Sigma$ encoder, the STC encoder requires no feedback loops or multi-bit subtraction. In fact, relying only on merger of periodic data sequences of different frequencies through different delays, this encoder is substantially simpler to implement in any hardware technology, not just superconductor RSFQ logic. The simplicity of logic implies faster speed. Therefore, this encoder is particularly attractive for implementation in RSFQ logic.

The similarities between $\Delta\Sigma$ and STC can be illustrated by consideration of the code patterns for several special cases. For example, an input level in the center of the input range for a $\Delta\Sigma$ modulator will generate alternating '1's and '0's. The STC is designed to do the same. Similarly, an input level at 1/4th of maximum will generate sequences of '1' followed by three '0's for a delta-sigma, which is again matched in the STC. Not all levels provide identical code patterns, but there is enough overlap to provide qualitatively similar behavior. It is important to emphasize that the STC is *not* a conventional oversampling encoder as discussed in the literature, but its similar functionality suggests that it should be placed in the same class with $\Delta\Sigma$ and related modulators.

III. Encoder Design

The encoder (Fig. 4) comprises primary RSFQ cells such as toggle flip-flops (TFF), latches, NDRO cells (non-destructive RS flip-flop), confluence buffers, splitters and Josephson transmission lines (JTL). The master clock stream is divided by factors of two through a chain of TFFs, punctuated by splitters, for providing access to the pulse streams of different frequencies (the master clock and its binary sub-harmonics). These binary sub-harmonics of the master clock are used to clock the NDRO cell in each bit slice, starting from the MSB. The NDRO cell acts as a switch, passing the input data to the output on clock. This output needs to be delayed appropriately, in order to implement the location assignment algorithm and to avoid bunching of data. Since these delays are binary multiples of the clock period, they can be realized using latches clocked at appropriate frequency of f, $f/2$ and so on. Finally, the appropriately delayed output pulses are merged with a confluence buffer to produce a serial 1-bit code sequence, representing the STC for the input n-bit digital word. The STC is then passed to a pulse-density-to pulse-width-modulation converter that acts as a digital pre-amplifier.

To begin, logic-level simulations were carried out using VHDL to confirm the operation of the circuit by verifying the STC output for various combinations of input data. Simulations were then carried out on a 4-bit encoder using PSCAN [4], to optimize intra-slice and inter-slice clock timings and delays. As shown in Fig. 4, the read clock for the LSB bit-slice, i.e. $f/16$ (also denoting end of frame), is used to reset all the NDRO cells and reload with fresh input data for the next frame. This input for the next frame is stored in a latch and is transferred to the NDRO cells on the reset pulse. In order to ensure scalability and high frequency operation, timing of the reset pulse becomes extremely critical. To avoid any timing error and to minimize

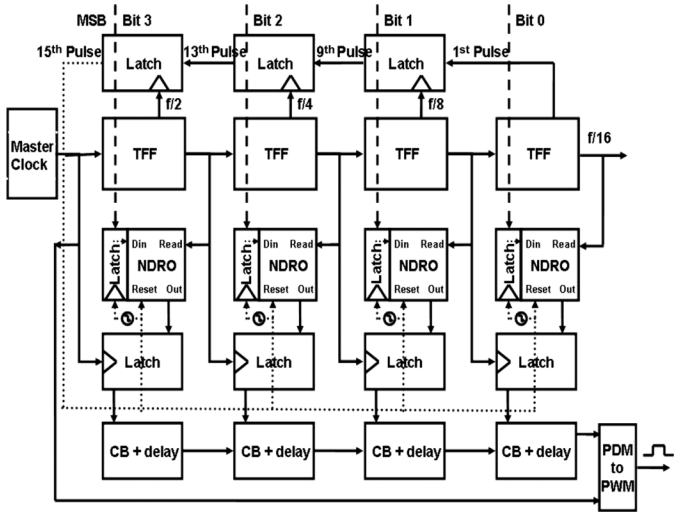

Fig. 4. Conceptual design of 4-bit staggered thermometer encoder with pulse-density to pulse-width converter.

the accumulated jitter on the reset line, the long timing loop between input and output ports of the TFF chain is broken down into several short intervals. For an n-bit encoder this is done by passing the output of the TFF chain through a series of $(n-1)$ latches with each latch being clocked by the output of TFF of the previous bit slice. This way the jitter is reduced to the loop formed by TFF and latch of the first bit slice only [5]. The optimized circuit was laid out in 4-bit and 7-bit versions.

IV. PDM-to-PWM Converter and Digital Amplifier

The output of the encoder circuit is a digital-RF single-bit data stream that contains the desired lower frequency components, which is the RF transmit waveform, in addition to higher frequency harmonics. In our case, the width τ of each single flux quantum (SFQ) pulse is of the order of 3–4 ps. Therefore, the frequency spectrum of the SFQ pulse data stream extends up to hundreds of GHz. These unwanted high frequency components can be removed by subsequent filtering in the amplifier chain. However, most of the energy, present in the high-frequency components, is permanently lost.

To avoid this permanent energy loss, we designed a novel digital circuit that indirectly performs the function of a digital amplifier. This circuit (Fig. 5) converts the pulse-density-modulated (PDM) data stream into a pulse-width-modulated (PWM) data stream, which changes the frequency spectrum by concentrating the energy in the fundamental while reducing higher harmonics. Upon filtering, the new PWM data stream produces the same analog output waveform but with higher power. The power amplification factor is approximately $1/(f\tau)^2$, the inverse square of the PDM duty cycle ratio. The main advantage of this on-chip digital pre-amplifier is that it is virtually noise-free. As shown in Fig. 5, a D flip-flop with complementary outputs produces Set and Reset pulses which are passed to the low voltage amplifier RSDCA (RS flip-flop followed by SFQ-to-DC) to construct the PWM waveform. This digital waveform is then amplified to the 3 mV level by an on-chip SQUID amplifier [6]. In the present test setup, further gain is obtained using semiconductor amplifiers at room temperature.

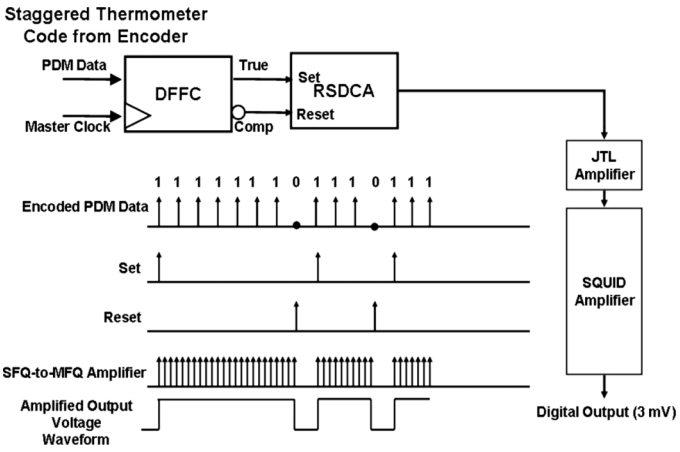

Fig. 5. On-chip digital amplification scheme changes the data format from pulse-density modulation (PDM) to pulse-width modulation (PWM).

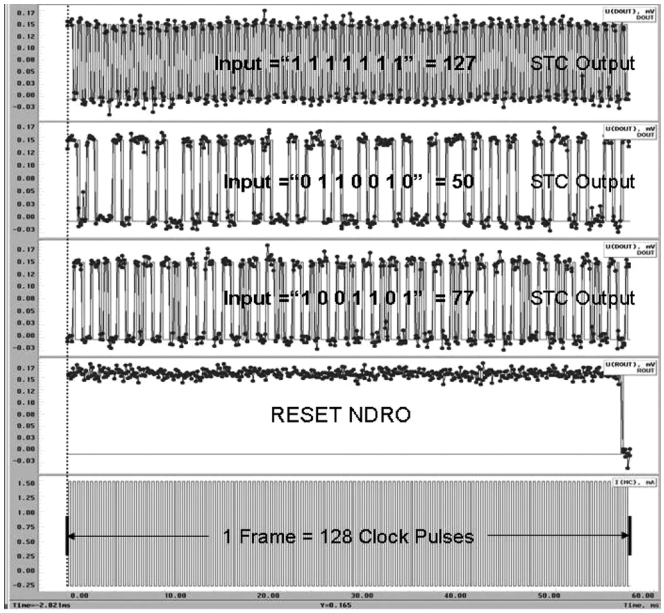

Fig. 6. Low frequency test results (voltage vs. time for a complete frame) for the 7-bit staggered thermometer encoder. The STC outputs are shown in toggle format, before conversion to PWM format. Output codes are shown for three inputs: 127 (all 1's), 50, and 77.

V. Test Results

A 5-mm chip containing a 7-bit encoder was fabricated and tested in a standard 40-pin test probe in liquid helium. The low-frequency (kHz) functional testing was performed using the automated test setup Octopux [7]. The bottom trace in Fig. 6 represents voltage vs. time for one frame, 128 pulses of the master clock. RESET NDRO denotes the reset output which is used to reset the NDRO cells at the end of the frame, as well as to load fresh input for the next frame. The three plots at the top of Fig. 6 show the STC outputs before PWM conversion (in toggle format) corresponding to the static input numbers 77, 50 and 127. All output codes were correctly generated.

As seen the outputs corresponding to input 77 and 50 are complementary, since the binary inputs corresponding to those numbers are '1's complement binary numbers. Also it can be

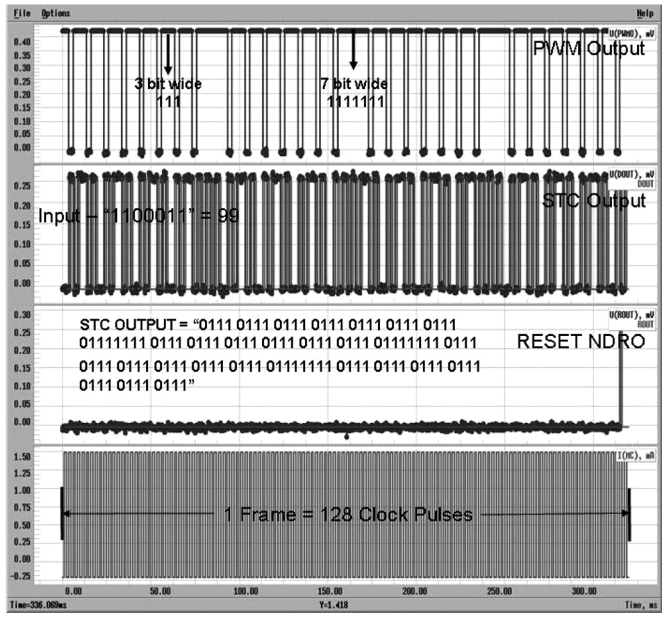

Fig. 7. Low frequency test results for the 7-bit staggered thermometer encoder with PDM-to-PWM converter, for input '110011' (binary 99).

verified that the output corresponding to input 127 is the sum of the outputs corresponding to inputs 77 and 50.

Fig. 7 shows the STC output for the input "1100011" (binary 99) and its corresponding PWM waveform. As seen, the PWM waveform has three-bit-wide patterns and seven-bit-wide patterns as a result of three consecutive '1's and seven consecutive '1's in the STC. The waveform transitions to zero level in response to a zero in the output code.

Fig. 8 shows the frequency spectrum for a static (DC level) input corresponding to the PWM waveform of Fig. 7, in dB vs. frequency over the range up to 205 MHz. A 1.7 GHz, DC coupled, low noise, inverting amplifier with a gain of 46 dB has been used to amplify the on-chip output at room temperature. A master clock at 204.8 MHz was used, corresponding to an input data rate of 1.6 MHz. One can view each '1' in the binary input as generating a periodic pulse sequence, which corresponds to a frequency pattern with a fundamental and harmonics, with an amplitude envelope that is largest for the MSB and smallest for the LSB. Furthermore, since these are square pulses, the envelope for each contribution follows a "sinc" dependence on frequency. The spectrum in Fig. 8 shows contributions of the four "1's" in the input. The contribution due to the MSB lies in the center and is overlapped with contributions from other inputs, particularly the MSB-1. The envelopes due to the first two LSBs are clearly visible below the major peaks.

In order to test the encoder at high frequency, we designed a 4-bit version of the encoder with a 16-bit shift register such that exactly one frame of the 1-bit serial code at high frequency is captured in the shift register. The shift register can then be read out with a low frequency clock. Fig. 9 shows the block diagram of the high frequency test chip. The delay on the clock line in the shift register is much smaller than the delay in the data line so that the incoming data is shifted by one bit on every clock. Application of Trigger 1 sets the TN (TFF with non-destructive readout) cell in state 1 in such a way that the 17th master clock pulse, which is also the first pulse on the next frame, is supplied

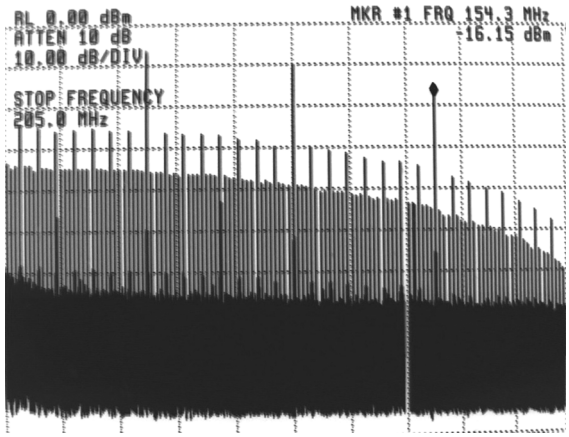

Fig. 8. Power spectrum (dBm vs. frequency) for low-frequency test of 7-bit STC encoder with PWM converter, for input '1100011'. The master clock frequency was 204.8 MHz and the input data rate was 1.6 MHz.

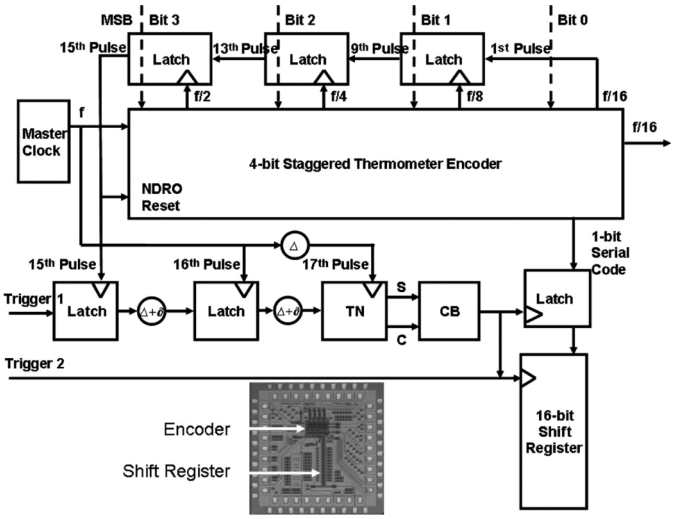

Fig. 9. Block diagram of a 4-bit staggered thermometer encoder for high-frequency testing. The inset at the bottom shows a photograph of a 5 mm chip comprising the encoder and shift register.

as clock to the shift register. In presence of the clock, the shift register is loaded with the serial 1-bit STC, with the data being serially shifted down in the shift register on clock. The second application of Trigger 1 resets the TN cell in such a way that the first pulse of next frame does not reach the clock input of the shift register. Since same set of input is repeated for every frame, exactly one frame of the STC is frozen in the shift register. An additional latch between the serial output and the shift register ensures that the data from the next frame does not reach the shift register. The shift register can now be read at low frequency by Trigger 2 which acts as a low-frequency clock input to the shift register.

Fig. 10 shows the high-frequency test result for the input 1100. The master clock was applied at 12.8 GHz and exactly one frame of data is captured in the shift register. The shift register was then read by a low-frequency clock. The output at the bottom of Fig. 10 shows the contents of the shift register, displaying the proper code conversion in toggle format. At the clock speed of 12.8 GHz, this circuit can digitally synthesize an RF signal with components up to 400 MHz, with 4-bit precision.

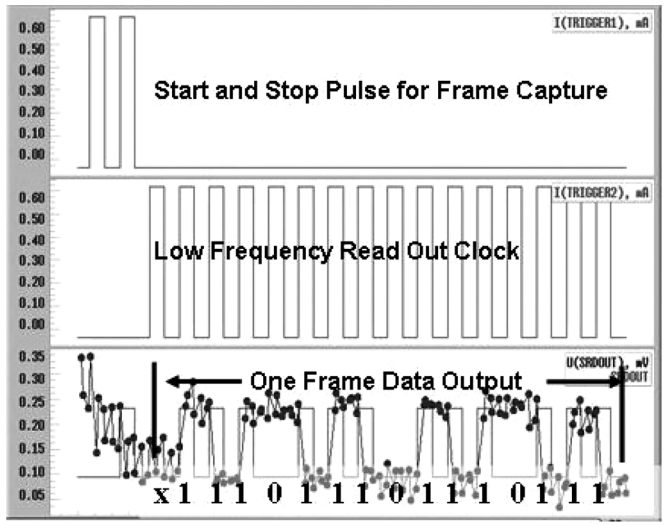

Fig. 10. High-frequency test results (voltage vs. time) for 4-bit staggered thermometer encoder and shift register. The master clock was applied at 12.8 GHz. Input data for '1100' (binary 12) was applied at 800 MHz for every frame. The output data on the bottom shows the contents of the 16-bit shift register, in toggle format, illustrating proper code conversion.

VI. Conclusion

We have successfully designed and tested a 4-bit and 7-bit version of a novel staggered thermometer encoder to convert a Nyquist rate N-bit digital word into a high frequency stream of single-bit data that is faster by a factor of 2^N. We have also successfully implemented an on-chip amplifier for converting the pulse-density-modulated data stream into a pulse-width-modulated data stream. Both circuits are key components for a digital-RF transmit waveform synthesizer.

Acknowledgment

The authors would like to thank Dr. Oleg Mukhanov for useful discussions, and the HYPRES fabrication team for producing the chips.

References

[1] D. Gupta and A. Kadin, "Apparatus and Method for Converting a Multi-Bit Signal to a Single-Bit Pulse Stream," US Patent No. 6,781,435, Aug. 2004.

[2] The Standard HYPRES Nb Process for 1 $\mathrm{kA/cm^2}$ and a Minimum Junction Size of 3 μm The Process Flow and Design Rules are available online: [Online]. Available: http://www.hypres.com

[3] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. Piscataway, NJ: IEEE Press, 1997.

[4] S. V. Polonsky, V. K. Semenov, and P. N. Shevchenko, "PSCAN: Personal superconductor circuit analyzer," *Supercond. Sci. Technol.*, vol. 4, pp. 667–670, Nov. 1991.

[5] J. C. Lin, V. K. Semenov, and K. K. Likharev, "Design of SFQ counting analog-to-digital converter," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2252–2259, June 1995.

[6] O. A. Mukhanov *et al.*, "Josephson output interfaces for RSFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 7, no. 2, pp. 2826–2831, June 1997.

[7] D. Y. Zinoviev and Y. A. Polyakov, "Octopux: An advanced automated setup for testing superconductor circuits," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 3240–3243, June 1997.