Integration of Cryocooled Superconducting Analog-to-Digital Converter and SiGe Output Amplifier

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***Abstract*—HYPRES is developing a prototype digital system comprising a Nb RSFQ analog-to-digital converter (ADC) and SiGe amplifiers on a commercial two-stage cryocooler. This involves the detailed thermal, electrical, and mechanical design of the ADC chip mount, input/output (I/O) cables, and electromagnetic shielding. Our objective is to minimize the heat load on the second (4 K) stage of the cryocooler, in order to ensure stable ADC operation. The design incorporates thermal radiation shields and magnetic shielding for the RSFQ circuit. For the I/O cables, the thermal design must be balanced against the acceptable attenuation of rf lines and resistance of dc bias lines. SiGe heterojunction bipolar transistor (HBT) signal conditioning circuits, placed on the first (60 K) stage of the cryocooler, will amplify the mV-level ADC outputs to V-level (e.g. ECL) outputs for seamless transition to room-temperature electronics. Cooling these HBT circuits lowers noise and improves their high-frequency performance. Demonstration of this prototype should lead the way to commercialization of high-speed digital superconducting systems, for such applications as wireless communication, radars, and switching networks.**

***Index Terms*—Closed-cycle refrigerator, Cryopackaging, Digital Receiver, Cryoelectronics, Thermal Management, Broadband Digital Link.**

I. Introduction

While the superior performance of superconducting digital electronics (SCE) has been demonstrated, no significant market for these has emerged so far. There are several reasons for this lack of commercial success: (1) until recently, no commercial application with a significant market demanded a level of performance that can only be attained with SCE, (2) almost all demonstrations have used liquid helium as a cryogen which is unacceptable for most commercial products, (3) ultra-fast, low-level signals used in SCE are incompatible with room temperature electronics (RTE). Recently, the situation has changed dramatically. The explosive demand for information bandwidth in the commercial and military wireless communication market has created a unique opportunity for superconducting digital electronics in software defined radio (SDR). Reliable, reasonably compact, and affordable 4 K cryocoolers are now available and have been used commercially by HYPRES to cool the Josephson primary voltage standard chip. Finally, improvements in cooled semiconductor low-noise, broadband amplifiers make it feasible to interface SCE with RTE in a manner that is transparent to the user.

In this article, we focus on small-scale SCE digital systems, consisting of a single integrated circuit (IC) or a few ICs on a multi-chip module (MCM), rather than large-scale digital systems. The architecture of a small-scale digital system, such as a digital-RF transceiver for wireless communications [1] is shown in Fig. 1. The superconductor ICs, assumed to be Nb RSFQ circuits, need to be cooled to 4–5 K, which requires a closed-cycle refrigerator (CCR) or cryocooler with at least two temperature stages. The higher the temperature of a cryocooler stage, the higher is its cooling capacity. For example, the cooling capacity of the first stage of our two-stage cryocooler is 30 times that of the second stage (Table 1). The overall size, weight, and power of a cryocooler can be minimized by optimal utilization of the cooling capacity at each stage.

Our design philosophy is to match to the cooling properties of a two-stage cryocooler: only very low power SCE on the second stage, higher power SiGe output amplifiers on the first stage, and minimization of the second stage heat load by diverting most of the conductive and radiative heat from room temperature through thermalization of all cables and radiation

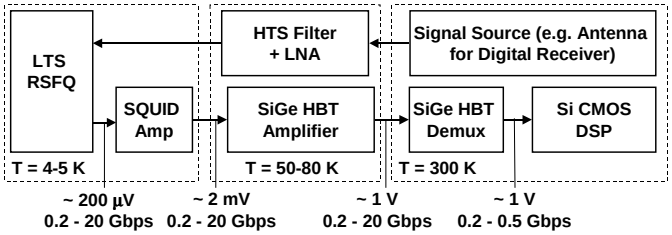

Fig. 1. Architecture of superconducting digital system, such as a digital receiver, integrated on a two-stage cryocooler. Examples of analog input (top) and digital output (bottom) links are shown.

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shield at the first stage. High-bandwidth digital output and analog input links, depicted in Fig. 1, are critical for a digital receiver. High-f_T SiGe heterojunction bipolar transistors (HBTs) may be used for broadband amplification of the high-speed digital outputs from RSFQ circuits. Cooling these amplifiers ensures lower noise and bit error rate and increased gain [2], while taking advantage of the available cooling capacity on the first stage. Moreover, SiGe digital circuits, ranging from simple demultiplexers to more complex digital filters, may be integrated on the first CCR stage to enhance functionality of these systems. The first stage may also host other components. These include analog HTS filters and low-noise amplifiers in the input signal path and lasers, electro-optic or magneto-optic modulators for optical output.

We have chosen to develop the cryopackage for an ADC chip with input sample rate of 20 Gsample/s, and 15-bit output signal [3,4]. This chip, which incorporates a complete programmable digital decimation filter and includes 6000 Josephson junctions, is one of the most complex superconducting digital circuits demonstrated to date. This 1 cm × 1 cm chip with 80 I/O pads also represents the whole spectrum of I/O lines – high-frequency input and clock lines, high-current dc bias lines, high-speed digital output lines – that are required in a complete digital-RF communications receiver and other small-scale digital systems.

II. Two-stage 4 K Cryocooler

We will use a two-stage Gifford-McMahon (G-M) cryocooler, manufactured by Sumitomo Heavy Industries Ltd.. Table 1 lists the properties of this cryocooler. We have measured the refrigeration capacity of this air-cooled cryocooler (SRDK-101D-A11) by applying appropriate heat loads to the first and the second stages, followed by measuring the temperatures of those two stages (Fig. 2). The first and the second stage temperatures, for several different combinations of applied heat loads, are plotted on the x- and y-axes respectively. The measured second stage temperature is indicated next to each point in Fig. 2 for clarity. Our measurements indicate that the cooling capacity of this cryocooler is at least twice that of the manufacturer's published (and guaranteed) specifications.

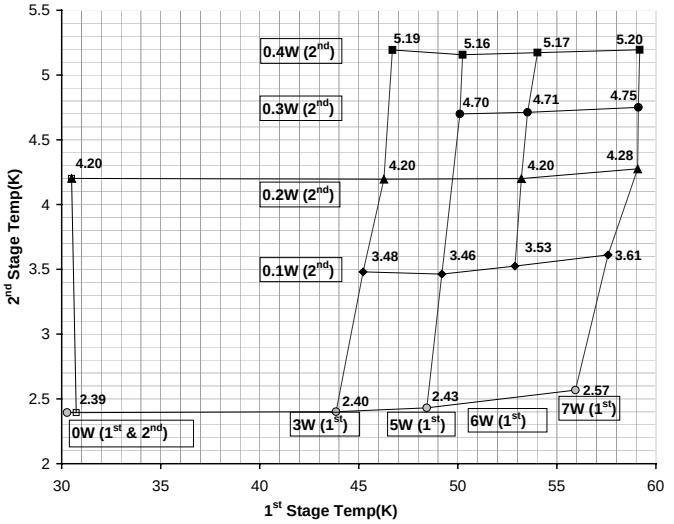

Fig. 2. Measured heat load map of a Sumitomo SRDK-101D-A11 cryocooler. Each point corresponds to a combination of heat loads applied to the first stage (0–7 W) and the second stage (0–0.4 W).

TABLE 1
PROPERTIES OF SUMITOMO SRDK-101D-A11CRYOCOOLER

PARAMETERS		VALUE
Heat lift	Manufacturer Spec	0.1 W at 4.2 K and 5 W at 60K
	Measured	0.2 W at 4.2 K and 6 W at 53K
Compressor input power		1.3 kW, 100±10 V (60 Hz)
Size	Compressor	$0.45 \times 0.385 \times 0.40$ m^3
	Cold Head	$0.13 \times 0.226 \times 0.442$ m^3
Weight	Compressor	42 kg
	Cold Head	7.2 kg

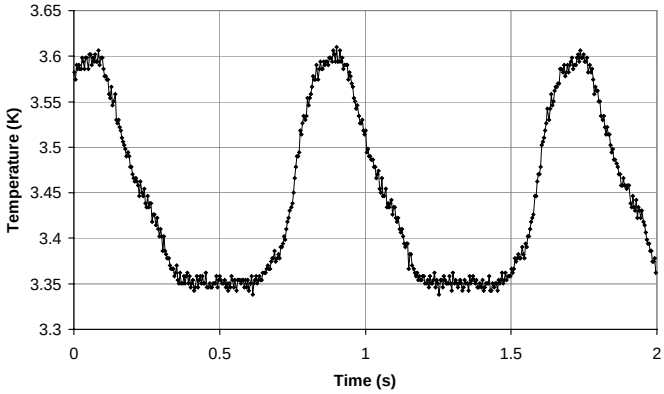

Fig. 3. Measured temperature oscillation of the Sumitomo cryocooler operating with a dc voltage standard chip.

SCE chips are typically tested in a liquid helium bath, which helps maintain a constant operating temperature of 4.2 K. The temperature of a cryocooled system may be subject to both long-term drift and to short-term oscillations. These cryocoolers remove heat by periodic compression and expansion of He gas, resulting in temperature oscillations at the cycle frequency. Typically, the temperature of the second stage has oscillations of 0.2-0.3 K, depending on the heat load (Fig. 3). Resulting fluctuations in the temperature-dependent circuit parameters may be detrimental to the performance of SCE circuits. In order to evaluate the effect of temperature change on circuit performance, we varied the temperature of the helium bath over a range of 4.2 to 4.3 K, while operating the ADC chip with fixed biases and input parameters; no perceptible change in performance was observed.

If necessary, passive damping with a large thermal mass may be used to quell these temperature oscillations. The most effective strategy for damping is to use a small volume of He instead of a large volume of low specific heat metal. The volumetric specific heat of He at 4.2 K is more than three orders of magnitude higher than Cu [5]. Moreover, at higher temperatures, He has much smaller specific heat than metals, orders of magnitude lower than Cu at 300 K, which means cooldown times are considerably reduced. Reduction of the temperature oscillation, by a factor of 10 has been demonstrated for a two-stage G-M cooler, employing passive damping with a small mass of He extracted from the He supply line of the compressor [5].

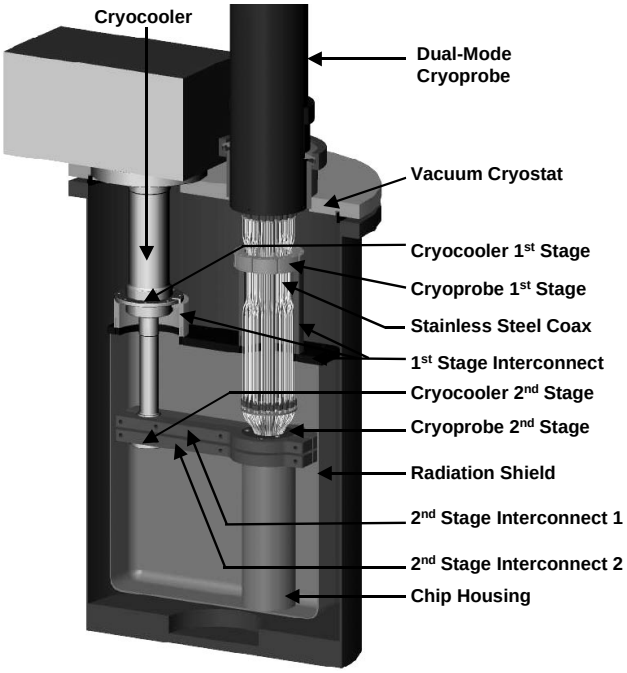

Fig. 4. Cut-away view of the complete cryopackage assembly.

III. Cryopackaging Approach: Dual-Mode Cryoprobe

Most SCE circuit demonstrations have been performed only with liquid He immersion test probes. HYPRES has recently developed a cryocooled system for the primary Josephson voltage standard chip, which is now available commercially, and which functions at least as well as its He-immersion counterpart [6]. Still, the large number of broadband I/O lines in the ADC chip requires a completely new cryogenic design.

To ensure smooth transition from this test environment to a cryocooled, chip-specific configuration, we have designed a dual-mode cryoprobe. This dual-mode probe can either be attached to a cryocooler using detachable thermal links or immersed in liquid He, permitting convenient comparison of chip performance in the cryocooler environment and the liquid He environment with the same input/output (I/O) cable configuration. Moreover, it introduces modularity in cryopackaging by separating the electrical module (the probe) from the cryogenic module (the cooler). Subsequently, a 'cold bus' that is supported by one or more cryocoolers may cool a number of electrical modules.

In this off-axis cryopackage, we have sacrificed the compactness of the traditional axial designs, where the entire package is centered on the cryocooler axis and I/O cables are integrated with the cold stages, to gain flexibility that is essential at the development stage. For example, a thermal damping module can be attached under the second stage without interfering with the cryoprobe. Upon successful development of the cryopackage, we can transfer the design to axial integration for small-scale applications, such as stand-alone digital-RF transceivers in communications base-stations. On the other hand, we will be able to expand on the modular architecture to transition to large-scale application, such as digital systems behind large antenna arrays.

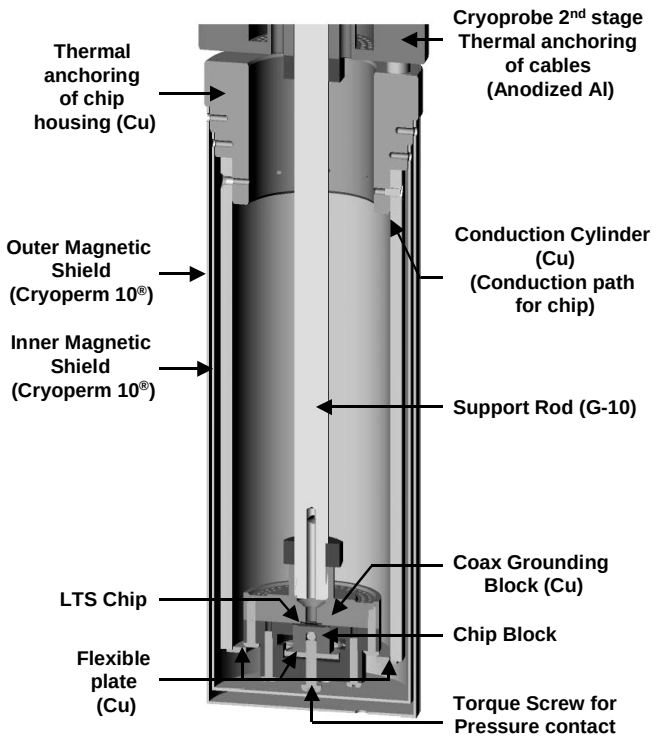

Fig. 5. The construction details of the chip housing.

Fig. 4 shows a cut-away view of the complete cryopackage. The two stages of the cryoprobe are thermally linked to the two corresponding stages of the cryocooler. The main purpose of these two stages is to provide thermal anchoring of I/O cables and for the radiation shield. The chip housing is separately attached to the second stage of the cryocooler. The chip housing (Fig. 5) comprises a copper conduction cylinder, surrounded by two magnetic shields, and a chip mount. The chip is placed on a flexible circuit board with matching pads, and contact is made by applying pressure on a copper block placed on the other side of the chip.

IV. Minimizing Heat Load: Choice of I/O Cables

Superconducting ICs dissipate very little power. The power dissipation of a 14-bit analog-to-digital converter circuit with about 6000 Josephson junctions is 1.2 mW. The cryocooler heat load is dominated by heat conduction through I/O lines between SCE and RTE, Joule heating in dc bias lines and thermal radiation. Thermalization of all cables and radiation shields to intermediate temperature stages minimizes the heat load at the coldest temperature stage. In our current system, there is only one intermediate temperature stage at 50 K.

To design I/O cables for an integrated cryopackage, we must consider both electrical and thermal properties of various cables and find an optimum configuration. The lower the thermal conductance of a cable the better it is from the thermal perspective. This implies high resistance cables, since the thermal conductance of a metallic line is inversely proportional to the electrical resistance. On the contrary, high electrical resistance gives high Joule heating for dc bias lines and high attenuation for ac I/O lines. Therefore, each I/O design must be customized to find the right balance between

the two conflicting requirements. In our case, the primary constraints are: (1) the cooling capacity of the cryocooler, and (2) the ability to transfer the mV-level digital outputs to room temperature without substantial loss of signal quality. We also took into account various secondary considerations, such as availability, cost, and ease of mechanical assembly for our cable design.

The I/O cables can be divided into four categories: (1) high-speed (>1 Gbps), (2) medium-speed (10 Mbps to 1 Gbps), (3) high current dc bias, (4) low-speed and low-current lines. The division between high- and medium-speed lines is driven by the attenuation of flexible ribbon and coaxial cables. For example, the total heat load on a stage at temperature T_2 due to a bias line with resistance R, carrying a current I, from temperature T_1 can be estimated by adding the Joule heating ($\dot{Q}_J$) and the conduction heating ($\dot{Q}_C$) terms as $\dot{Q} = \dot{Q}_J + \dot{Q}_C = I^2 R + L\overline{T}\Delta T / R$, where L = $(\pi k_B/e)^2/3$ = 24.5 nWΩ/K^2 is the Lorenz number, $\overline{T}$ is the mean temperature and ΔT is the temperature difference. The optimum resistance, corresponding to the minimum total heat load, can be obtained by various wire configurations. We have done complete finite-element modeling of the entire dc bias line, comprising twisted pairs and coaxial sections, for the ADC chip with the r.m.s. value (35 mA) of its bias current. Fig. 6 shows the temperature profile between the first and the second stages.

In our design, we have chosen coaxial cables for both high- and medium-speed lines. The coaxial cables are divided into three sections, the middle section being a short length of stainless steel (SS) coaxial cable that has a high thermal resistance, and a bottom section of non-magnetic Cu coaxial cable for penetration into the magnetically-shielded chip housing. For the dual-mode probe, the tri-section cable consists of a first section of 1 m long, 1.19 mm outer diameter UT-47C (Cu/Cu), a 0.2 m long, 0.86 mm outer diameter second section of UT-34SS-SS (SS/SS), and a 0.14 m third section of UT-47C (Cu/Cu). For the high-frequency input signal and clock lines, we chose more expensive Gilbert-Corning GPPO connectors that are rated up to 60 GHz.

Fig. 7 shows the frequency dependence of the attenuation of this cable — 2.7, 7.4, and 12.2 dB at 1, 10, and 20 GHz

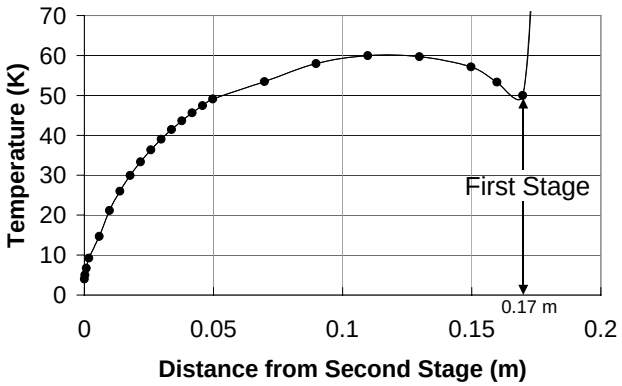

Fig. 6. Finite element calculation of temperature profile of current-bias line between first and second stages of cryocooler. 32 AWG phosphor-bronze twisted pair extends 50 mm above and 150 mm below the 50 K heat sink.

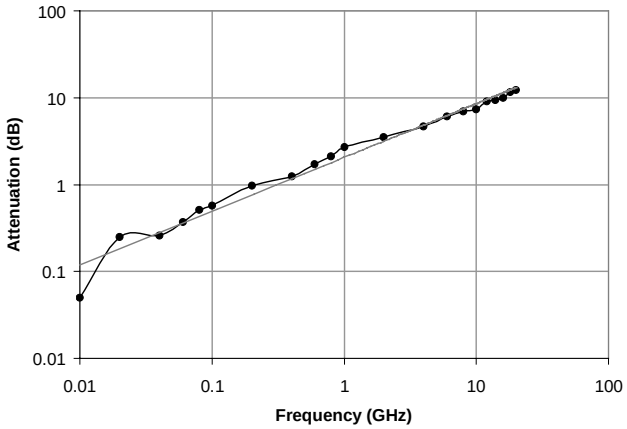

Fig. 7. Measured attenuation of the tri-section cable with GPPO connectors as a function of frequency.

respectively. For the medium-speed digital data lines, MMCX connectors were used owing to their considerably lower cost. Both types of connector are much smaller than standard SMA connectors and facilitate compact packaging. Flexible BeCu microstrip ribbon cables were also considered for medium-speed output lines. At 1 GHz, electrical attenuation and heat conduction of these ribbon cables were measured to be nearly identical to the tri-section coax cable. Both GPPO and MMCX connectors are manufactured to accommodate UT-47 semi-rigid cable, but we have developed a method for joining them to UT-34 cable by using suitable shims. We tested these modified connector assemblies both at room temperature and at liquid nitrogen temperature and determined that they performed to within specification for both reflection and attenuation. No change in performance was observed at liquid nitrogen temperature. The criterion for choice of cabling was to choose an attenuation value acceptable for the digital output of the ADC, which resulted in an acceptable heat load to the cryocooler. The chosen 3-section combination gives a calculated 3.5 dB power loss at 1 GHz.

A one-dimensional finite-element thermal model of the three-section coaxial cable was developed; this took into account temperature-dependent thermal and electrical conductivities, Joule heating and radiative heat exchange. In modeling the temperature difference between the inner (core) and the outer (shield) conductors, we have not assumed that the Teflon dielectric is in good thermal contact with outer conductor; heat transfer may be via radiation, solid conduction by direct contact, conduction by low-pressure residual gases in the annular gap. However, in the absence of sufficient published experimental data to support a reliable model of any conductive radial heat transfer, only the radiative transfer was considered and represents a calculable worst case. Fig. 8 shows the temperature profile of this composite coaxial cable.

V. Calculation of Cryocooler Heat Load

The heat load on the second cryocooler stage was calculated for the ADC chip [3]. Table 2 lists and adds up contributions from all the sources of heat for the dual-mode probe. The thermal radiation to the second stage is from the

radiation shield, which is thermally sunk to the first stage at 50 K. If we take both surfaces to be ideal black bodies, then the heat transfer will be ~ 25 mW, which will be greatly reduced by the standard use of low-emissivity surfaces. The total heat load is well within the refrigeration capacity of the Sumitomo cooler.

So far in this design, the first stage is used only for thermalization of cables and shields. The calculated total heat load from I/O cables to the first stage is 0.85 W: 0.47 W for the UT-47C and 50 mm UT-34 coax. combination, 0.38 W for the UT-47C and 50 mm bronze twisted pair combination, corresponding to high-speed and dc bias lines respectively. The heat load from room temperature radiation is also significant due to the relatively large surface area of the shield.

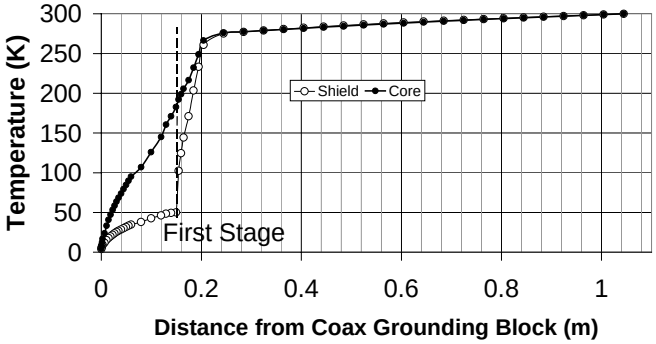

Fig. 8. Calculated temperature profile of composite coaxial cable spanning room temperature to 4K. Warm section is 0.8 m long UT-47-C and cold section is UT-34-SS-SS, extending 0.05 m above the 50K heat sink and 0.15 m below it, to a second short UT-47-C section which is assumed to be at 4 K (distance = 0.14 m). Radial heat exchange is by radiation only.

TABLE 2
CALCULATED SECOND STAGE HEAT LOAD FOR HYPRES ADC [3]

Source of Heat			**Heat Load (mW)**
Thermal Radiation from 50K (worst case estimate)			**<25**
Conduction from support rod between 50K and 4K			**5**
ADC Chip			**1.2**
I/O Cables	**Heat per Line (mW)**	**No. of Lines**	**53.5**
DC Current Bias Lines (32 AWG Bronze lines carrying 35 mA)	0.45	30 pairs	26.6
DC Voltage Monitors + Others (32 AWG phosphor bronze)	0.1	10 pairs	2.1
20 GHz Clock Input (UT-34-SS-SS coax.)	0.65	1	0.65
1 GHz Digital High Speed Output Lines (UT-34-SS-SS coax.)	0.65	28	18.2
Output Clock lines (300 MHz)	0.65	2	1.3
Extra High Speed Lines	0.65	7	4.6
Total Heat Load			**<86**

VI. DIGITAL OUTPUT LINK: COOLED SIGE AMPLIFIER

The digital output link from SCE to standard RTE requires amplification by almost three orders of magnitude with a bandwidth in the GHz range. The needed multi-THz gain-bandwidth product is beyond any transistor technology. Fortunately, we can take advantage of nonlinear amplification, which is not subject to the same gain-bandwidth limitation, due to the digital nature of the signal. In the circuit described below, we use three linear gain stages, amplifying from 1 mV to 80 mV, followed by a nonlinear Schmidt trigger to reach 800 mV standard ECL levels (Fig. 9). Still, a very high cutoff frequency (f_T) is required for a digital link up to 10-20 Gbps.

SiGe Heterojunction Bipolar Transistor (HBT) devices have been developed to produce some of the fastest devices in production using Silicon technology. Recently IBM announced that 207 GHz f_T and 285 GHz f_{max} are achievable for this device [7]. As an additional motivation for using SiGe, the relevant parameters, β, f_T, and f_{max}, all appear to improve monotonically with decreasing temperature, at least down to 77 K [8]. Even SiGe HBT amplifiers that are not optimized for cryogenic operation in any way perform better at 77 K than at 300 K. We have used design techniques, developed by Cressler [9] to implement SiGe HBT circuits that will work both at room temperature and liquid nitrogen temperature.

In order to provide a seamless interface between LTS circuits and room temperature DSP, a composite linear-nonlinear amplifier chain was designed to scale from ±1 mV differential output of the SQUID amplifier [10] to 800 mV p-p ECL signal levels. The linear part of this composite amplifier [adapted from ref. 11] consists of three cascaded differential amplifier stages, isolated with input and output emitter followers at either end. Each of these stages contains a pair of differentially connected transimpedance circuits (Fig. 10) with optimized peaking. The peaking effect in the amplifier transimpedance gain function is necessary to maximize the amplifier bandwidth [11]. A high input impedance nonlinear amplifier, which is functionally similar to a low-frequency Schmidt trigger (Fig. 11), provides the final stage of extremely high gain and pulse shaping. The Schmidt trigger was modified to be compatible with fully differential current steering logic. This circuit, designed for the IBM 5HP (f_T = 47 GHz at 298 K) BiCMOS fabrication process through MOSIS [12], is expected to operate with a bandwidth greater than 10 and 15 GHz at 298 K and 77 K respectively. Fig. 12 shows the layout of the amplifier test chip.

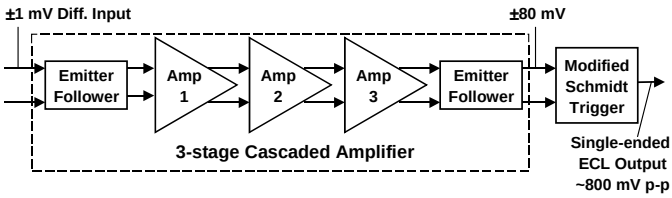

Fig. 9. A SiGe HBT amplifier chain, consisting of a three-stage cascaded differential amplifier with emitter follower buffers and a modified Schmidt trigger, designed to convert the mV-level differential digital output from LTS chips to V-level single-ended ECL signal.

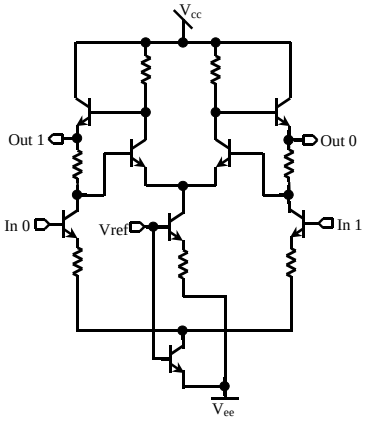

Fig. 10. Transimpedance amplifier circuit diagram.

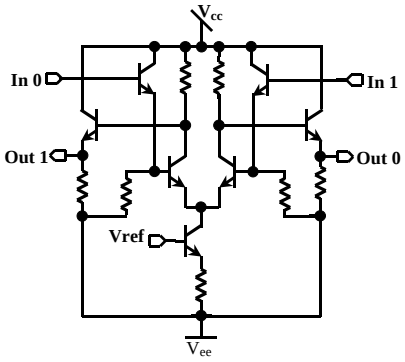

Fig. 11. Modified Schmidt trigger circuit diagram.

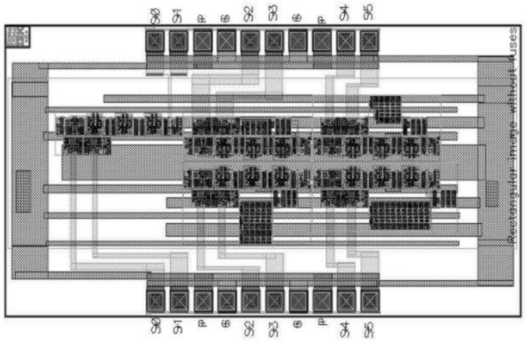

Fig. 12. A 3.2 mm × 1.6 mm test chip with 5 complete amplifier chains and associated test circuitry, including different ring oscillators, was designed for the IBM 5HP SiGe process.

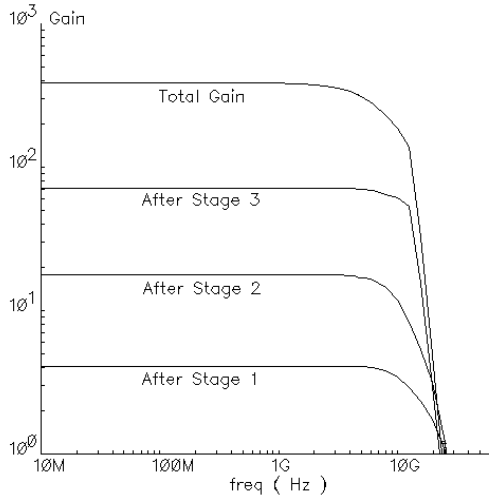

Fig. 13. Simulated frequency characteristics of the amplifier chain at room temperature, 298K; the final bandwidth is 6.4 GHz.

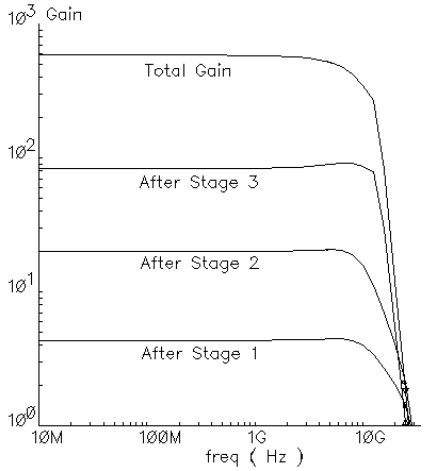

Fig. 14. Simulated frequency characteristics of the amplifier chain at 218K; the final bandwidth is 8.1 GHz.

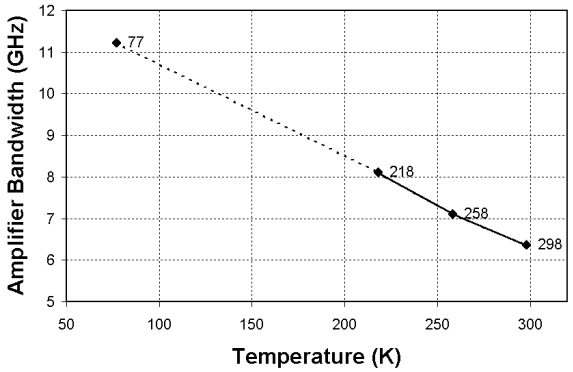

Fig. 15. Estimated increase of bandwidth with decreasing temperature. The extrapolated final bandwidth at 77K is 11.2 GHz.

Fig. 13 and Fig. 14 show the pass-band characteristics of the SiGe amplifier chain at T = 298K and T =218 K respectively. In addition to the total gain of the amplifier chain, the cumulative gains after each of the three linear stages are shown. The bandwidth of the composite amplifier chain increases from 6.4 GHz at room temperature to 8.1 GHz at 218K. A linear extrapolation of amplifier bandwidth to 77 K predicts a bandwidth of 11.2 GHz (Fig. 15), which is consistent with the expected increase [9]. In general, the

minimum bandwidth needed in a bit rate of f_b is about 3/4 f_b [13].

Fig. 16 shows the simulated time-domain response of the amplifier chain at 298 K for a 2 mV digital input signal with 100 ps bit width. The outputs before and after the Schmidt trigger are shown, indicating some roll-off of final amplitude at this frequency. However, it is believed that the cryocooled amplifier will achieve the full gain to ECL level up to 10 Gbps.

The power dissipation of the composite amplifier circuit, including additional output pad drivers that are not shown in Fig. 9, is 200 mW. Several such amplifier channels will be needed to provide the digital output interface for a small-scale LTS system. For example, the ADC chip [3] requires 15 amplifier channels – one each for the 14 digitized output bits and one for the decimated clock output – that correspond to an additional heat load of 3 W on the first stage.

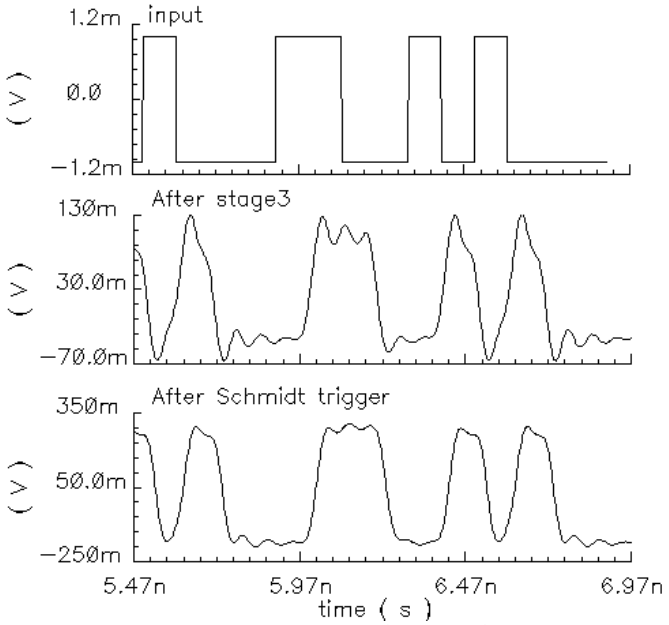

Fig. 16 Simulated time-domain response of the amplifier chain to 10 Gbps NRZ data pattern, showing the input (top), the output after the third stage of linear amplification (middle), and the final output after the Schmidt trigger (bottom).

VII. Conclusion

We have designed a prototype cryopackage for a small-scale superconducting digital electronics system. More specifically, we are integrating a complex RSFQ circuit, a high-resolution ADC, in a two-stage commercial cryocooler. Our development strategy follows two tracks: (1) developing a dual-mode cryoprobe for smooth transition from liquid helium test environment to the cryocooled environment, and (2) developing a high-speed digital link to ensure seamless integration with standard room temperature electronics. With careful thermal design, we accommodate the heat load for this 80-lead system on a 4 K stage with less than 100 mW of available heat lift. In order to achieve this it is essential to thermalize all I/O cables and radiation shield on the first (50-60 K) stage intercepting most of the heat conducted from room temperature. The first stage also has additional cooling capacity that can be utilized by interface electronics, such as semiconductor amplifiers. The temperature oscillations on the second stage are significant (~0.25 K) but can be damped to acceptable levels, if necessary. For the high-speed digital link we have custom-designed, cascaded SiGe HBT amplifiers. Simulations indicate that SiGe interface amplifiers can effectively condition mV-level digital signals to V-level ECL signals, up to 6 GHz at room temperature and even higher at low temperature. The dual mode cryoprobe is being fabricated at High Precision Devices and the SiGe amplifier chips have been submitted for fabrication at IBM Microelectronics Division.

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