A Superconductive Flash Digitizer with On-Chip Memory

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***Abstract*-- Recording transient physical phenomena such as short electromagnetic pulses requires a very wide- band digitizer. We have successfully designed, fabricated, and tested a superconductive flash digitizer circuit using Nb trilayer technology. The digitizer consists of a 6-bit flash analog-to-digital converter (ADC), a set of on-chip switches to start and stop data acquisition, and a bank of acquisition shift-registers for on-chip memory. A 5-MHz clock reads the data out to room-temperature electronics for analysis. We have used this digitizer to acquire multi-GHz sine waves. We have also recorded the details of short single pulses containing both a short rise time (~100 ps) and structure with greater than a 10 GHz instantaneous bandwidth.**

I. Introduction

One of the most obvious and commercially viable applications of a wide-band ADC is the front end of a transient digitizer. The unique properties of Nb superconductive technology enable extremely high-performance ADCs. The same Nb trilayer technology can be used to fabricate the digital acquisition circuitry necessary to handle the data from such an ADC, thereby producing a monolithic implementation of a superconductive transient digitizer. The addition of low-speed room-temperature interface electronics provides a complete data path in which analog signals with bandwidths greater than 10 GHz can be digitized, recorded in real time, stored temporarily on chip, then read out for analysis.

There are several applications in which a wide-band digitizer would greatly enhance measurement capabilities. For instance, recording single-shot laser pulses for studying Inertial Confinement Fusion (ICF) requires a digitizer with multi-GHz bandwidth and adequate memory storage. These pulses can have bandwidths greater than 10 GHz. Commercially available digitizers either have inadequate bandwidth, or are prohibitively expensive. Applications such as resolving multiple hits for particle detectors, measuring the beam profile for particle accelerators, and measuring signals in high-performance computers will benefit from the wide-bandwidth and high clock rate of a superconductive digitizer.

We have successfully demonstrated a monolithic digitizer chip with a 6-bit flash ADC and 32 words of on-chip memory. Our initial results demonstrate greater than 10 GHz bandwidth, real-time memory acquisition, and a sampling rate of up to16 GigaSamples/s (GSa/s).

We are developing this technology to meet the needs of the ICF and particle physics communities as well as for the R&D community-at-large. Our near-term goal is a self-triggered transient digitizer in a very simple cryogenic package.

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The transient digitizer will have an input bandwidth well in excess of 10 GHz, and a maximum sampling rate of 40 GSa/s. The resolution is projected to be 6 effective bits at input bandwidth of 10 GHz. The digitizer will be able to record up to a 25 ns data record length at a clock rate of 20 GHz.

The bandwidth specification far surpasses that of any other transient digitizer based on semiconductor ADCs. The sampling rate is both commensurate with the Nyquist criterion and appropriate for applications such as laser diagnostics. This performance is not approachable in the near future by any other digitizer based on ADCs.

The digitizer front end has already demonstrated the bandwidth requirement, and sampling up to 40 GSa/s has also been demonstrated. The path to obtaining the required resolution and data record lengths will be discussed below.

II. Architecture and Principle of Operation

The transient digitizer consists of a monolithic chip on a passive silicon substrate, and an electronics interface to room-temperature storage and analysis tools. The superconductive digitizer chip contains a flash ADC, a set of digital switches to start and stop data acquisition, and a bank of acquisition shift-registers (ASRs) for data storage. The system is completed by room-temperature electronics to acquire and analyze the data produced by the chip.

A block diagram of a transient digitizer system is shown in Fig. 1. The ADC, which has been clocked up to 20 GSa/s, acquires data continuously. A very simple triggering scheme was implemented to simplify the initial demonstration.

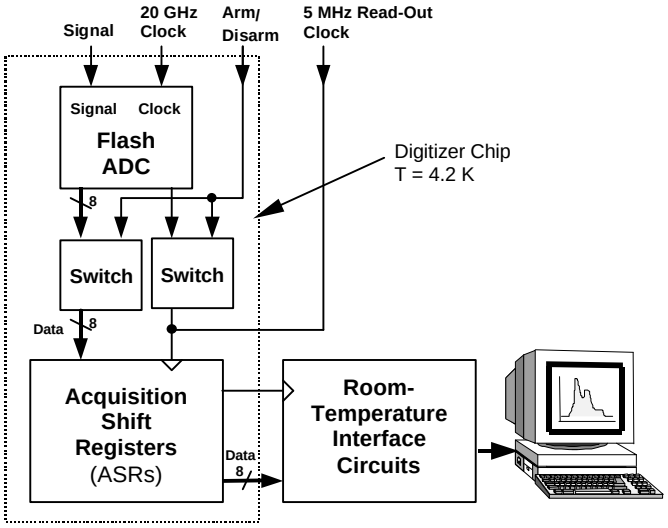

Fig. 1. This block diagram represents the components of an 8-bit version of a transient digitizer for converting analog waveforms to digital data and storing those data for analysis. All components except for the room-temperature interface circuits and the computer are contained on a monolithic cryogenically cooled chip.

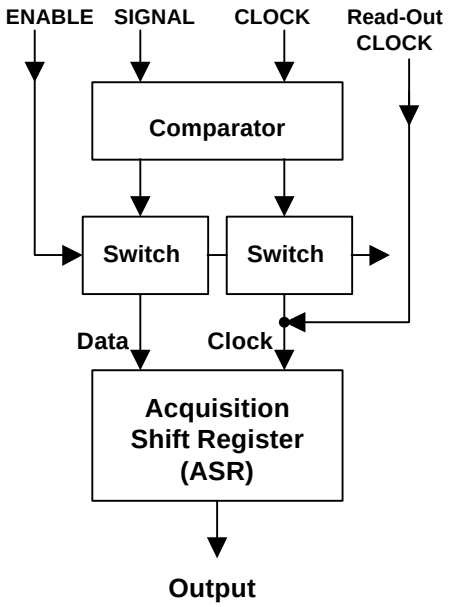

Fig. 2. Schematic diagram of one bit slice of the transient digitizer, showing the how the signal is digitized, and how the data acquisition is controlled by ENABLE and Read-Out CLOCK pulses.

The data path through the transient digitizer is described by the bit slice shown in Fig. 2. The signal is digitized by the comparator, stored in a latch, and then clocked out. Both the high-speed CLOCK and DATA pulses are sent through switches, which are controlled by an ENABLE pulse. Acquisition starts when the enable pulse rises. When the enable pulse falls, the switches open to discontinue the passage of high-speed CLOCK and DATA pulses. The DATA that are already loaded into the ASRs are off-loaded to room temperature electronics using 32 5-MHz Read-Out CLOCK pulses.

All digital circuits in the transient digitizer chip, including the ADC comparators, acquisition switches and shift registers, were designed using Rapid Single Flux Quantum (RSFQ) logic [1]. RSFQ logic is especially well suited to the transient digitizer because of its ability to read out the state of the comparator and manipulate data at the high clock rates required for this project.

We are extending these capabilities in advanced designs, to produce a commercial product. The transient digitizer product will sample at rates up to 40 GSa/s by time-interleaving two ADCs. We have already demonstrated 2 ns of on-chip memory when running at 16 GSa/s, and have already fabricated chips capable of 8 ns of on-chip memory at that speed. Our transient digitizer will be able to store more than 12.5 ns of data when operated at 40 GSa/s, and more than 25 ns of data at 20 GSa/s. In addition, the digitizer will contain circuits for self-triggering and delaying the acquisition start time. The transient digitizer product will also have control circuitry for automatic set-up and self-calibration.

In the following sections, we discuss each of the major transient digitizer components before discussing the experimental results and plans for reaching our performance goals.

A. Flash ADC

The flash ADC used in the transient digitizer demonstration is a Gray-code design [2] with six active comparators in a linear array. The signal is delivered by an R2R ladder such that each successive comparator in the array gets half of the remaining signal.

Our previous comparator was based on the Quantum Flux Parametron (QFP). We have replaced it with an RSFQ design [3]. The QFP comparator required too large an exciter current, and also exhibited significant noise problems when operated at high speed. The RSFQ comparator in Fig. 3 only needs enough clock current to switch the appropriate junction of a decision-making junction pair of junctions, resulting in less cross-talk on chip.

As in the QFP design, the RSFQ design uses a 2-spoke SQUID wheel (a two-leaf phase tree) [4], [5] containing two quantizing junctions. When the quantum-mechanical phase between these junctions is adjusted by the phase bias to equal π (half a flux quantum), the combination acts as if it were a very small junction. This reduces the effective LI_0 product of the comparator circuit, and thus helps to linearize the circuit dynamics. A 1-pH shunt inductor in parallel with input transformer inductance reduces the total inductance of the circuit.

This comparator exhibits dynamic distortions. These threshold distortions are manifested as unequal “0” and “1” regions. The magnitude of this effect depends on the slew rate. This effect is described schematically in Fig. 4 for a linearly ramped input signal. For a large positive slew rate, the “1” regions predominate, whereas the “0” regions predominate for large negative slew rates. These threshold distortions are not noticeable at low speed, but without corrective engineering, high-speed operation is not effective.

These dynamic distortions arise from intrinsic *L/R* delays internal to the comparator circuit, which are in turn dependent on the junction phases. The dependence on the *sign* of the slew rate originate in these phase-dependent time constants, which causes the comparator to lag or lead the CLOCK more depending on the sign of the current in the SQUID wheel.

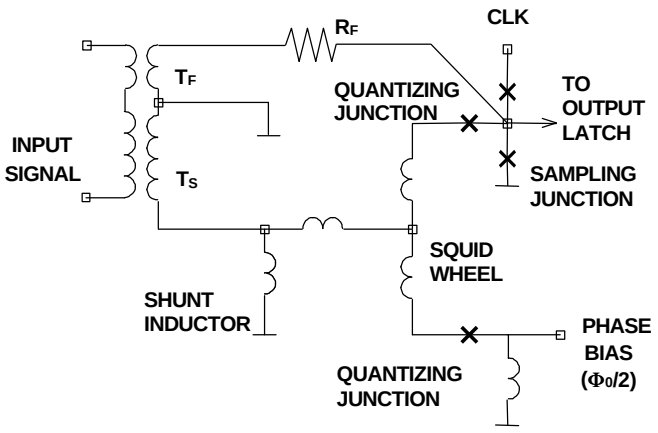

Fig. 3. Schematic diagram of RSFQ comparator cell, showing the input transformer T_S, the feedback transformer T_F, the feedback resistor R_F, the SQUID wheel with its two quantizing junctions. The decision-making junction pair consists of the clock junction and the sampling junction.

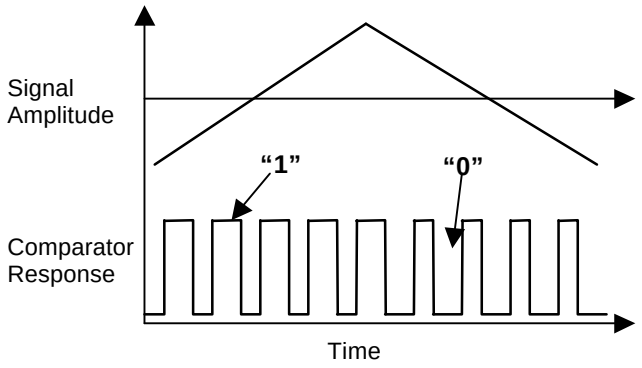

Fig. 4. The comparator response at high slew rates exhibits dynamic distortions. The "duty factor", which is the fraction during which the comparator outputs a "1", is larger for positive slew rates, and smaller for negative slew rates.

A simple feedback circuit (shown in Fig. 3) reduces these distortions. A voltage proportional to the slew rate is *subtracted* from the decision-making node. This method has been shown to enable better operation at high slew rates.

B. Acquisition Switches

Two switches control the acquisition process for each bit. One switch controls high-frequency CLOCK pulses, while the other controls DATA pulses. Each switch set is composed of one dual-output DC/SFQ converter and two Non-Destructive Read-Out (NDRO) cells [6], as shown in Fig. 5. The rising edge of the ENABLE pulse causes the DC/SFQ converter to produce a pulse from port 1. These pulses set the state of the NDRO switch equal to "1". The CLOCK and DATA pulses entering the input port read out the state of the switch. The falling edge of the ENABLE pulse causes the DC/SFQ converter to set the NDRO cells to "0", thereby shutting down the acquisition process.

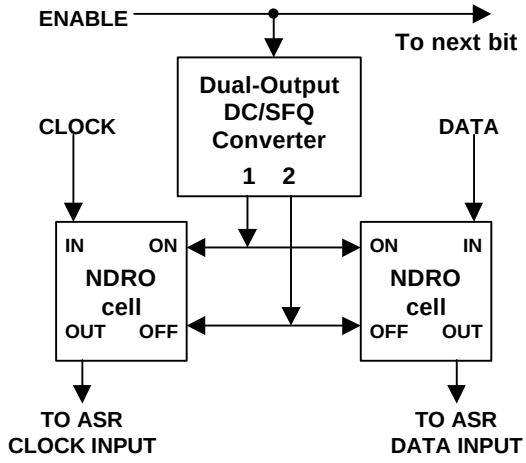

Fig. 5. This block diagram describes the acquisition switch design. The dual-output DC/SFQ converter produces an SFQ pulse from port 1 on the rising edge of the ENABLE pulse, and another SFQ pulse from port 2 on the falling edge. The pulses from port 1 are split and applied to the ON port of the NDRO cell. The port 2 pulses are also split, and are applied to the OFF port of the NDRO cell.

C. Acquisition Shift Register

The acquisition shift registers were assembled using a Destructive Read-Out (DRO) cell. This cell is of a rather standard design, but is fairly compact (40μm × 120 μm). These cells had previously been tested up to 20 GHz in shift registers up to 32 cells in length.

D. Output circuits

During the read-out procedure, CLOCK and DATA pulses passed by the ASR were used to respectively reset and set a standard HYPRES cell containing an RS-flip flop and an SFQ/DC converter. Because of the very short time between resetting and setting the flip-flop, the output appears as non-return-to-zero data on a slow oscilloscope. The output voltage from the SFQ/DC converter was approximately 0.3 mV.

E. Room-Temperature Interface

The room-temperature interface circuits were originally designed for the HYPRES high-resolution ADC project [7]. These circuits can accept the low-level outputs of the SFQ/DC converters without pre-amplification. The electronic interface was implemented with a VME crate containing one clock-receiver card and two data-receiver cards (with 4 20-MS/s data channels per card). The interface box converted the ADC data to standard TTL levels.

The data were transmitted to a PC-based ADC evaluation station containing a 50 MS/s NCI logic analyzer card and custom Visual Basic software running under MS Windows™. The software instructs the logic analyzer to acquire data, unload the data to computer memory, and then display, reconstruct and analyze the data.

III. Experimental Results

A. Flash ADC Test Results

We have previously measured and reported the performance of single RSFQ comparators [3] using "beat-frequency" tests [2]. We found the threshold transition width is approximately 1 ps. This sets a lower limit on the "aperture uncertainty", or the accuracy of *when* sampling is accomplished. We have demonstrated the wide bandwidth of our comparators in beat-frequency tests up to 30 GHz.

We have also used beat frequency tests to measure the high-speed performance of a 5-bit Gray-Code ADC [2]. Figures 6 and 7 show the ADC tested with a 1.000001 GHz signal and at a clock rate of 1.000000 GHz. Fig. 6 displays a 5-bit reconstruction of the Gray-coded data bits and the digital comparator outputs. Fig. 7 shows the same circuit operated with a 5 times larger input signal to measure the dynamic range. The reconstruction is wrapped to allow the display of all transitions. The least significant bit (LSB) has at least 80 useful transitions at 1 GHz, which could provide more than 6 effective bits of Gray-code resolution. An ADC with 8 of these comparators interleaved in an advanced architecture (as discussed below) would have 640 thresholds, which is more than enough for 9 bits of resolution at 1 GHz.

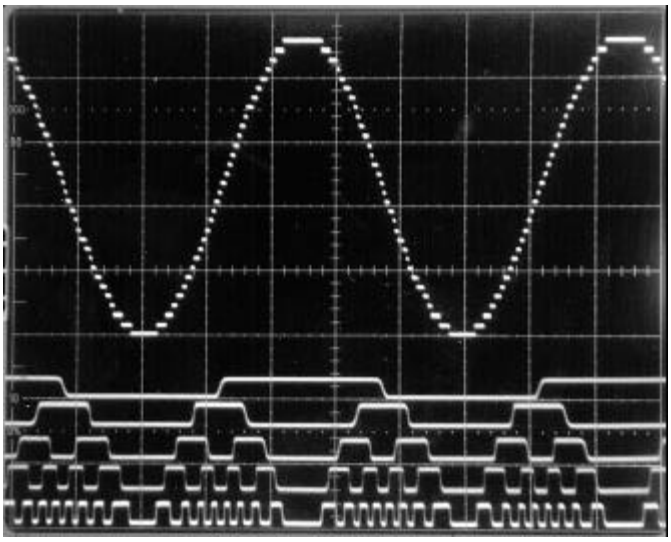

Fig. 6. This 'scope photo shows a 5-bit reconstruction of a 1.000001 GHz sine wave at full-scale deflection. The Gray-scale comparator outputs are shown in ascending order (LSB to the Most Significant Bit, or MSB) at the bottom.

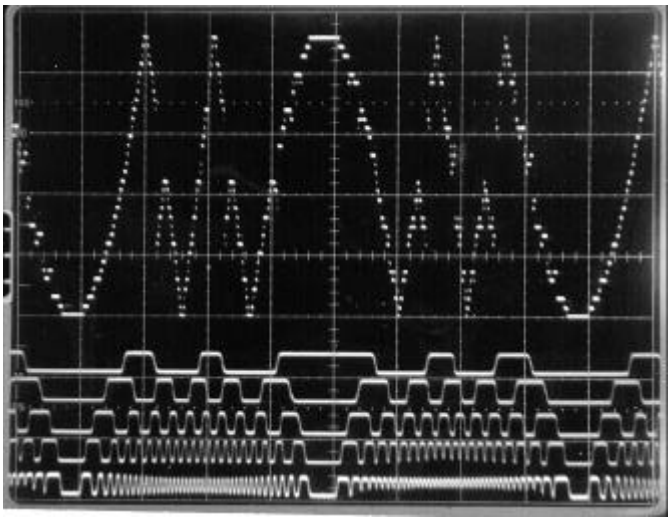

Fig. 7. This beat-frequency test is identical to that of Fig. 6, but the amplitude has been increased beyond full scale, resulting in a folded reconstruction. There are 80 useful transitions at this slew rate.

Threshold distortion limits the maximum toggle rate and the ultimate ADC resolution. By optimizing the feedback resistor, we increased the maximum toggle rate to 120 thresholds/ns. This is within about a factor of two of our goal.

The major performance advantages of this flash ADC are its ultra-wide bandwidth and high clock rate. Fig. 8 shows a beat frequency test at 20 GHz with a 3-bit reconstruction. These data clearly demonstrate that the ADC has wide input bandwidth and may be clocked at its target rate of 20 GHz. Such wide input bandwidths have not been demonstrated by semiconductor ADCs. The almost 4 effective bits at 12 GHz is within about a factor four of our performance target at that frequency (6 effective bits at an instantaneous bandwidth of 10 GHz).

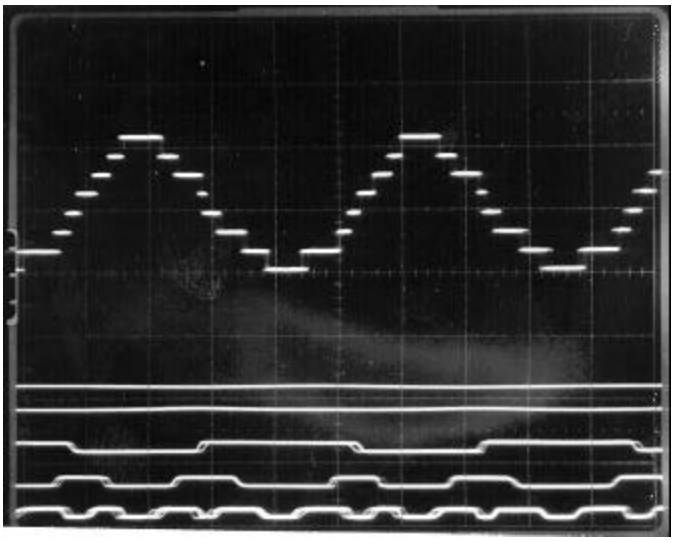

Fig. 8 This 'scope photo shows a 3-bit reconstruction of a 19.999995 GHz sine wave clocked at 20.000000 GHz. These data demonstrate the extremely wide input bandwidth of the flash ADC.

B. Transient Digitizer Test Results

A 1 cm × 1 cm digitizer chip (shown in Fig. 9) was designed to contain two 6-bit transient digitizers. The design was implemented using HYPRES library cells appropriate for a current density of 2.5 kA/cm^2. The chips were fabricated using the standard HYPRES 10-layer 2.5 kA/cm^2 process[8].

The flash ADC is essentially a six-bit version of the ADC used in the beat-frequency tests. For each bit, a switch set (see Fig. 5) and a 32-stage acquisition shift register were attached to the appropriate comparator CLOCK and DATA output ports.

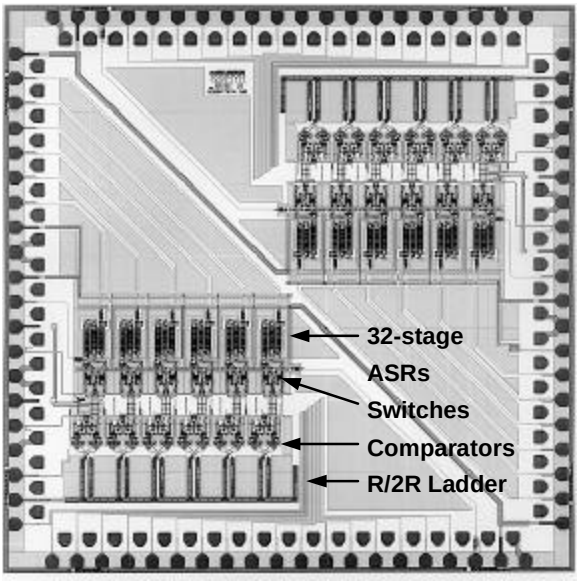

Fig. 9. This layout shows the 1 cm × 1 cm chip used in the first single-pulse capture of a multi-GHz waveform by a superconductive transient digitizer. Each chip contains two complete transient digitizer circuits. We have also produced chips with 128-stage ASRs, and eventually will increase the length to at least 512.

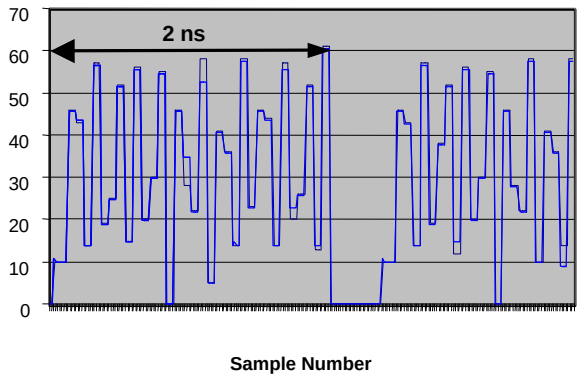

Fig. 10 This acquisition of 6.25 GHz sine waves shows the characteristic "fish-scale" effect coming from incommensurate input and clock frequencies (12.5 complete sine waves were sampled). Two acquisitions are plotted here one atop the other. The two data sets differ in only a few places. Each low-temperature point was sampled 4 times at room temperature.

An HP 80000 was used as a master controller. The HP80000 generated the ENABLE pulse to arm the acquisition circuits. After the falling edge of the ENABLE pulse halted acquisition, 32 pulses were produced to read the data. An HP 83712A frequency synthesizer generated the high-frequency sinusoidal clock input.

Fig 10 shows single-shot acquisitions of 6.25 GHz sine waves digitized at 16 GSa/s. These data were taken without optimizing the ADC thresholds, so the resolution is somewhat less than 3 effective bits. This test proved that the acquisition switches and shift registers worked at these high speeds. Optimizing the ADC by using interleaved LSB comparators and other techniques will markedly improve the resolution.

A single-shot pulse was also digitized. The pulse was generated using a wide pulse from the HP 80000 pattern generator, along with a 10-cm length of shorted cable. Fig. 11(a) shows the raw data (solid line) from the 32-stage shift-register memory for an 8 GSa/s acquisition, using a 4 ns enable pulse.

A sampling 'scope measurement of the pulse (plotted as points) is superimposed on the transient data. Fig. 11(b) shows similar data taken for a 2 ns ENABLE pulse, and a sampling rate of 16 GSa/s.

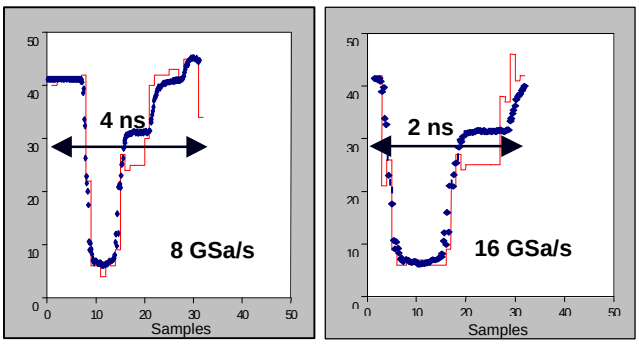

Fig. 11(a). The data digitized at 8 GSa/s shows the structure of the original pulse (solid line). A sampling 'scope measurement of the same pulse is superimposed (points). The ENABLE overlapped the measured pulse by 4 ns to make this measurement. (b) The pulse digitized at 16 GSa/s zooms in on the middle 2 ns (solid line). A sampling 'scope measurement of the pulse is superimposed (points). A 2 ns ENABLE pulse was used for this measurement.

This is the first time real-time superconductive flash ADC data have been recorded. At least some of the discrepancies between the transient digitizer and the sampling oscilloscope data arise from ADC distortions. We anticipated such errors from our previous high-speed flash beat-frequency, and have developed a new ADC architecture to eliminate them.

IV. Improved Architecture for Higher Resolution

With perfect comparators, the Gray-Code flash ADC is the most effective architecture. However, when comparator threshold distortions are present, there is a marked decrease in ADC resolution. Architectural improvements, including redundant comparators and real-time digital error-correction logic, can restore much of the lost performance.

A. Interleaving LSB Thresholds

Dynamic threshold distortion occurs in the LSB comparators at high slew rates. Lowering the LI_0 product and introducing feedback help to linearize the comparator response, but there is a maximum limit where the thresholds will begin to wash out. By interleaving several identical comparator thresholds, using XOR logic to combine pairs of thresholds, then XORing those thresholds, new thresholds for additional bits of resolution can be synthesized. The architecture for implementing the XOR logic is shown in Fig. 12. We have successfully combined thresholds of up to 8 comparators up to 8 GHz. Fig. 13 shows that at 4 GHz, threshold distortions make the third synthesized bit ineffective

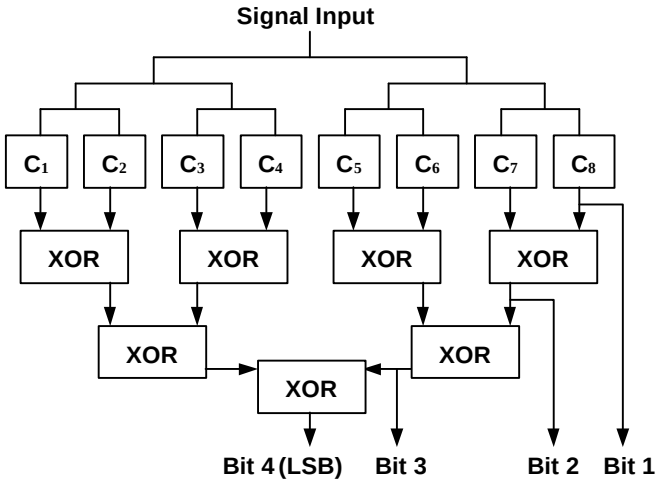

Fig. 13 The thresholds of eight comparators can be interleaved and combined using RSFQ XOR gates operating at the clock frequency.

B. Look-Back Digital Error Correction for MSB Thresholds

The MSB comparators receive the smallest fraction of signal current, resulting in the widest "gray zone" near the threshold. By interleaving the thresholds of two comparators per bit, and using real-time RSFQ digital logic, the comparator furthest away from its gray zone can be chosen [9]. The algorithm uses the output from the previous bit to choose the correct comparator, hence the name "look-back logic". We have demonstrated all components for real-time error correction.

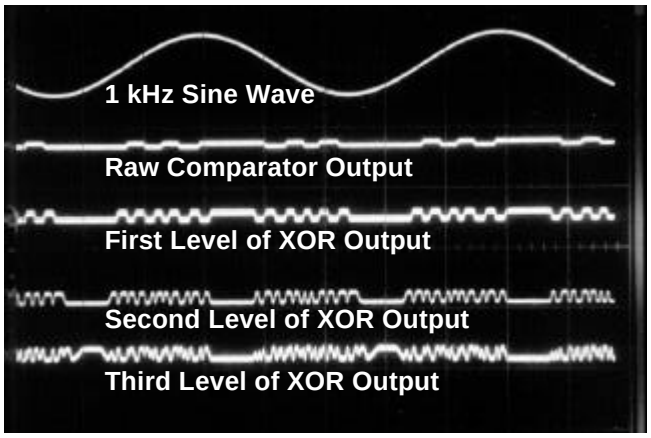

Fig. 13 This beat-frequency test demonstrates LSB synthesis by threshold-interleaving eight comparator thresholds, and combining those thresholds using real-time XOR logic. The signal is a 4.000000 GHz sine wave; the clock is a 4.0000001 GHz sine wave. At these slew rates, threshold distortion makes the third level of interleaving ineffective.

C. Signal and Clock Path

The advanced ADC architecture is shown in Fig. 14. The interleaved LSB comparators on the left side synthesize additional bits. All look-back logic is based on the Bit 3 output. Bit 3 determines which of the Bit 4 comparator outputs is error-free. The selected Bit 4 output determines which Bit 5 comparator is error-free, and so on. A single clock line and a single signal line has been designed to split their respective signals to the dual set of comparators for each bit.

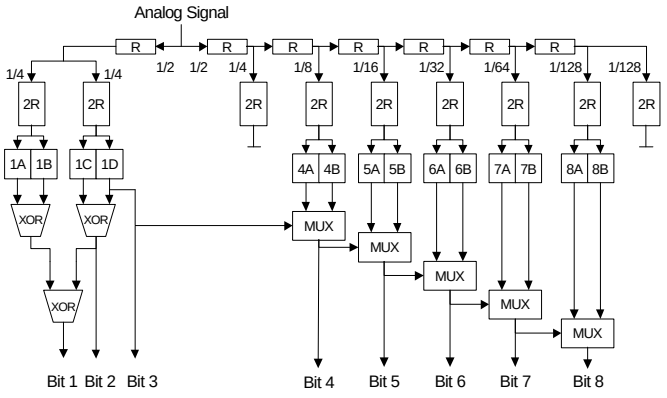

Fig. 14 This ADC architecture includes redundant comparators and digital logic to correct ADC errors in real time. Bits 1 and 2 are synthesized from a set of four comparators with interleaved thresholds. Bits 4-8 each utilize two comparators, and look-back digital error correction.

V. Conclusion and Discussion

We have successfully designed, fabricated and demonstrated a complete transient digitizer system consisting of a superconductive flash ADC, on-chip acquisition hardware, a room-temperature interface and the appropriate software to digitally reconstruct the input signal. The technological performance of all major components has been measured:

The wide bandwidth of the digitizer front end has been demonstrated in beat-frequency tests up to 30 GHz. The bandwidth of ADC test chips has been shown to far exceed 10 GHz (the 3 dB point is at ~16 GHz). All of the digital hardware, including digital switches and shift registers has been operated up to 20 GHz.

We have successfully used the transient digitizer containing these components to measure both sine waves and short pulses. The reconstruction of digitized pulse in Figures. 8, 10 and 11 demonstrates the wide bandwidth of the transient digitizer's ADC front end.

This transient digitizer has attained a level of performance that demonstrates it is potentially useful to workers in a wide variety of fields, including pulsed-laser diagnostics and internal-confinement fusion. It should be emphasized these results were achieved using an extremely simple ADC architecture, and relatively coarse 3-μm lithography.

Specific performance improvements have been identified, and are in development. The result will be a transient digitizer with a near-term performance of at least 6 effective bits at 10 GHz, and 8 effective bits at 2.5 GHz. Moreover, by using our simple 10-layer chip technology, the price of the digitizer will be very competitive.

Acknowledgment

The authors would to the HYPRES fabrication team (Dave Donnelly, Rick Hunt, Roy Patt, Ted Ross, and John Vivalda) for their expertise in producing the chips used in this project.

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