SUPERCONDUCTOR ANALOG TO DIGITAL CONVERTER FOR SIGINT APPLICATIONS

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ABSTRACT

Superconductor analog-to-digital converters (ADC) offer high sensitivity and large dynamic range. We report recent advances in the low-pass phase-modulation-demodulation (PMD) oversampled analog-to-digital converter (ADC). The oversampled data from the PMD front-end are passed along with sampling clock to an on-chip digital filter. In the past, the maximum frequency of operation of such chips were limited by that of the digital decimation filter (DDF) to about 30 GHz. Recently, we have designed a chip that allows the PMD front-end to be clocked twice as fast as the DDF, resulting in sampling rates of 46.08 GHz and 29.44 GHz for chips with critical current densities of 4.5 and 1 kA/cm^2 respectively. We have also designed a new PMD front-end, with a quarter-rate quantizer (QRQ) that allows 18-20 dB extension of dynamic range. We are also pursuing a subranging ADC design with two PMD front-ends connected with fluxon amplifier and subtractor circuitry that promises a dynamic range extension by 25-30 dB. We report signal-to-noise ratio and spur-free dynamic range measurement results for various ADC chips, and project performance for future improvements.

INTRODUCTION

THE increasingly complex electromagnetic spectrum in commercial and military frequency space presents SIGINT applications on board ship with a correspondingly demanding dynamic range requirement. SIGINT systems must digest the energy generated on board, while looking at the farthest possible range for new emissions. Just one radar can dominate an analog to digital converter's signal to noise ratio, leaving no bits for a clean representation of other signals, from either on or off the ship. This problem has become continuously more demanding as the spectrum on and off the ship have become more complex, leaving a virtually insatiable desire for dynamic range in analog to digital converters. Ultrafast switching speed, low power, natural quantization of magnetic flux, quantum accuracy, and low noise of cryogenic superconductor circuits enable fast and accurate data conversion between the analog and digital domains. Based on rapid single-flux quantum (RSFQ) logic, these integrated circuits are capable of achieving performance levels unattainable by any other technology [1]. Over the last decade, results on design and evaluation of a superconductor ADC based on the phase modulation-demodulation (PMD) architecture [2] were reported. Starting from testing of single PMD ADC modulators integrated with an on-chip digital decimation filter with room temperature data acquisition system [3], we have made steady progress in building complete cryo-cooled digital receiver prototypes [4,5].

One of the most critical parameters to characterize the performance of an ADC is its dynamic range. Dynamic range of the ADC is bound by the maximum signal that can be digitized and the quantization noise. For a delta ADC, the maximum signal amplitude at a given frequency is limited by the maximum slew rate. To decrease the quantization noise, one can use a multi-channel synchronizer, which effectively subdivides the clock period, measuring the pulse position more precisely in time [2]. Functionally, this multi-channel synchronizer increases the number of quantization levels, making the least significant bit (LSB) smaller. However, the thermal noise limits the maximum number of channels that one can use to reduce the clock period before it is no longer significant. Thus, for a given noise floor, to increase the dynamic range one needs to increase the slew rate limit of the ADC. This paper presents several architectural modifications that are being implemented to further enhance the dynamic range of the ADC.

ORIGINAL ADC ARCHITECTURE

The basic concept of the delta ADC based on PMD architecture with a single junction quantizer is illustrated in the Figure 1. In the absence of analog signal, the single junction SQUID quantizer pulses at the carrier frequency (f_{car}) which is determined by the average fluxon transport rate through the modulator (f_{pump}). When an additional analog input signal is coupled to the quantizer loop, the timing of each output pulse gets advanced or retarded in proportion to the derivative of the analog input. This process encodes the signal derivative into SFQ pulse positions, which need

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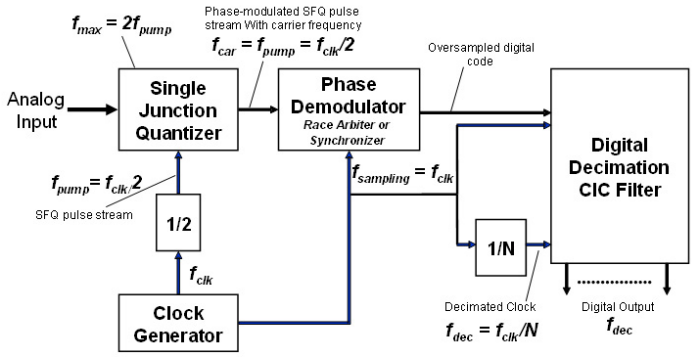

Figure 1. Original Phase Modulation-demodulation ADC followed by a digital decimation filter.

to be decoded by measuring the pulse positions against a time reference. Hence the phase modulated SFQ pulse stream is passed to a phase demodulator (synchronizer), which is a clocked sampling circuit that generates a '1' or a '0' indicating whether or not an SFQ pulse arrived during that clock interval. Thus, the synchronizer decodes the pulse position information into numbers (single-bit in the simplest implementation). The oversampled digital data and the corresponding clock from the synchronizer then proceed directly to the decimation filter [6], where it is first integrated at full speed, and then averaged further, reducing the output bandwidth and increasing the effective number of bits.

The test results for this ADC sampled at 29.44 GHz and decimated by 256 are to be reported in [7]. For a 10 MHz signal, the spur-free dynamic range (SFDR) in the Nyquist band is 97.11 dB and the signal-to-noise ratio (SNR) is 78.2 dB translating into 12.7 effective number of bits [ENOB = (SNR–1.76)/6.02]. Additional averaging in the 10 MHz band gives SNR of 89.15 dB or 14.5 ENOBs.

Although, impressive performance has been achieved by this ADC, further improvements are hindered by the process limitations. In the original design, the modulator sampling clock is also used to clock the digital decimation filter. However, the filter is much more complex than the ADC itself, and forces a limit on the maximum clock speed, which in turn limits the slew-rate and hence the maximum input signal amplitude.

The following section details some of the architectural modifications being pursued to overcome these limitations.

APPROACHES FOR HIGHER DYNAMIC RANGE

Figure 2 shows the envisioned low-pass ADC development strategy. The performance of a proven ADC chip design, which has been fabricated and measured, serves as the baseline design. We then present several improved architectures and project performance enhancement for each compared to the baseline performance. The tags on each architectural block in Figure 2 represent its progress status in the design chain. For example, *Built* represents an ADC

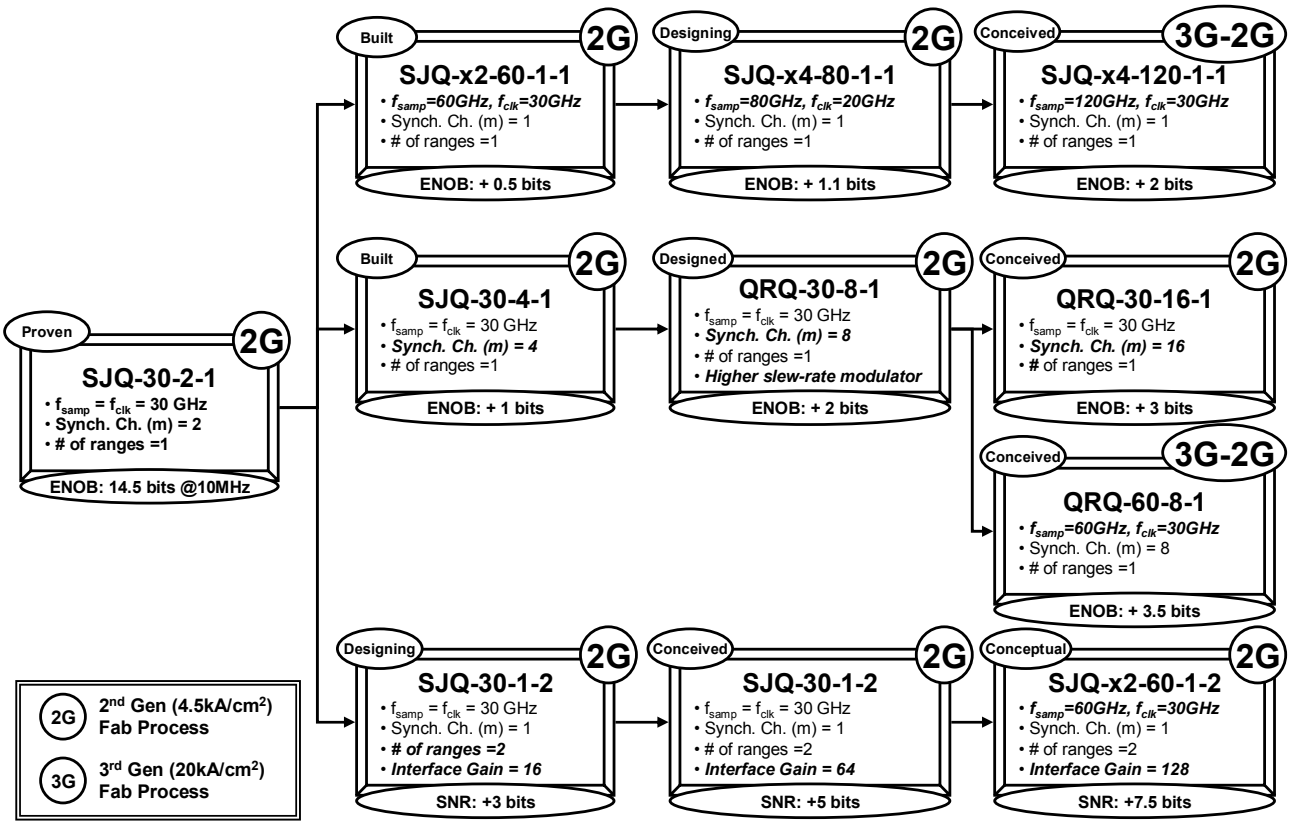

Figure 2. Envisioned strategy for Low-Pass ADC development

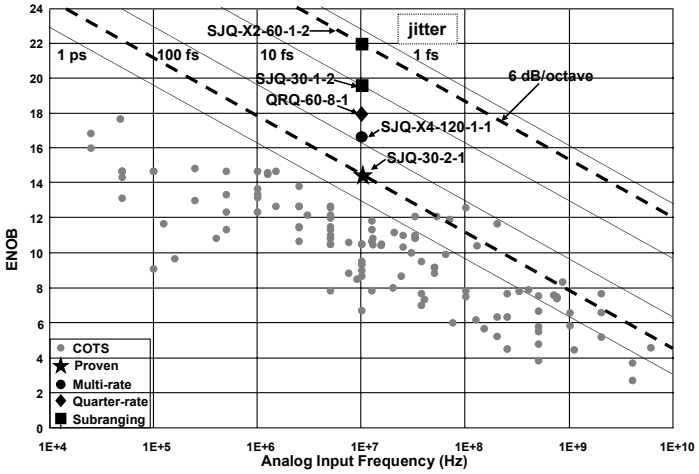

Figure 3. Demonstrated performance of our proven design and projected performance from improved architectures is shown along with the state-of-the-art ADC data from Bob Walden.

that is designed and fabricated, but not tested; *Designed* represents an ADC that has been designed but needs to be fabricated; *Conceived* represents matured ideas on an ADC that needs to be designed, and so on. All performance figures for the ADC are quoted for a 10 MHz input signal frequency; the SNR is projected for a 10 MHz bandwidth. The proven design is a single junction quantizer ADC based on PMD architecture (SJQ-30-2-1), sampled (f_{samp}) at 30 GHz, using a 2-channel synchronizer ($m=2$) with one (1) range, i.e a single modulator architecture. As mentioned earlier, the measured performance of this baseline design is 14.52 ENOBs in a 10 MHz bandwidth. Figure 3 shows the performance of the proven design and projected enhancements from improved designs with the state-of-the-art ADC data from Bob Walden. For our first order delta ADC, the 6 dB per octave slope shows the decrease in SNR with increase in the input signal frequency. There is also a 3 dB per octave performance degradation with increase in bandwidth [2].

In the sections below, we describe the improvements being pursued including the Hybrid critical current density (J_C) fabrication process, the multi-rate ADC, quarter-rate ADC, and the subranging ADC.

A. Hybrid Critical Current Density Fabrication Process

The switching speeds of Josephson junctions scale as the square root of the process critical current density (J_c), for optimized critically damped Josephson junctions with current levels held fixed. Thus by migrating to a higher J_c process, the sampling speed of the modulator can be increased. Every doubling of the sampling frequency gives additional 9 dB in SNR. However, the relative immaturity of the fabrication process results in low yield circuits, making it difficult to get reproducible results on complex

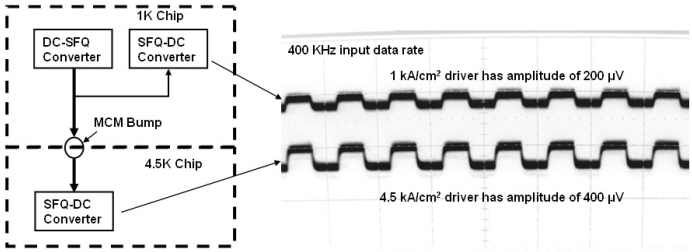

Figure 4. Block diagram of the hybrid J_c test chip (left) and low frequency test results (right). Doubling of output voltage observed on the driver fabricated in the 4.5 kA/cm^2 process relative to the driver in 1 kA/cm^2 process.

circuits such as a second-order decimation filter (~ 2500 Junctions). On the other hand, the relatively simple (~ 200 Junctions) front-end can be fabricated with higher yield in a high J_c fabrication process. Thus, enhanced performance can be achieved by fabricating the front-end in high J_c technology, while continuing to fabricate the complex circuits in more mature, lower J_c technology. The clock rate transition between different sections of the circuit requires demultiplexing of the modulator output to multiple streams. We envisage using the hybrid J_c approach (3G-2G) such that the front-end is fabricated using HYPRES' 3rd generation (3G) fabrication process with 20 kA/cm^2 critical current density, whereas complex circuits like decimation filter continue to be fabricated using the 2nd generation (2G) fabrication process with 4.5 kA/cm^2 critical current density process [8].

In order to demonstrate the hybrid J_c concept, we have initially used the simple SFQ to DC driver as the test bed. The data to the driver is provided by DC to SFQ circuits fabricated on a separate chip, in the 1st generation (1 kA/cm^2) process. The driver is fabricated on another chip, in the 4.5 kA/cm^2 fabrication process. The two chips are connected on a multi-chip module (MCM). The output voltage of the driver in the high J_c process is expected to double relative to the driver in the low J_c process.

Figure 4 (right) shows the low frequency test results for the hybrid J_c drivers. As expected, the output voltage for the driver in 4.5 kA/cm^2 process is 400 μV, twice higher than the driver in 1 kA/cm^2 process.

B. Multi-Rate ADC

Once again, the basic idea of a multi-rate ADC is to use different clock rates for sampling of the modulator (f_{samp}) and the digital filter (f_{clk}). The front-end, being a much simpler circuit can be yielded to operate at much higher sampling frequencies than decimation filters (~ 30 GHz for 2G process). To provide a rate transition between different clocks, the ADC synchronizer output is demultiplexed into a set of N lower rate data streams each at f_{samp} /N. An increase of the ADC clock frequency enables 1.5 bits/octave

performance enhancement. However, so far we designed a demultiplexed (N = 2) ADC with only a single channel synchronizer (m = 1) that results in 1-bit performance degradation compared to the original ADC with m = 2. We project that this ADC (SJQ-X2-60-1-1) will operate at sampling frequency of 60 GHz, twice the sampling frequency of the proven design, enabling resultant performance enhancement of 0.5 bits in an equivalent bandwidth. Infact, a preliminary version of this chip has been operational at sampling frequency of 46.08 GHz, with the decimation filter clocked at half the sampling frequency. The complete characterization of the ADC is still in progress and will be reported in [7]. The front-end can be clocked at even higher frequencies. We expect the front-end to be sampled up to 80 GHz. Extending the multi-rate architecture to N = 4, this implementation (SJQ-X4-80-1-1), could provide 1.1 bit performance enhancement. We are in the process of designing such an ADC. We further conceive implementing the ADC with the hybrid J_c approach (SJQ-X4-120-1-1). With f_{clk} limited at 30 GHz, the front-end can now be clocked at 120 GHz, enabling 2-bit performance enhancement.

C. Quarter-Rate ADC

Every doubling of the synchronizer channels gives an additional bit in SNR. Thus, the ADC with 4-channel synchronizer (SJQ-30-4-1) should enable a 1-bit performance enhancement, provided that the intrinsic flux noise floor remains below the LSB. We have improved ADC transformer design to increase mutual inductance while lowering the secondary inductance to get a lower intrinsic noise floor.

Another independent approach to dynamic range enhancement is to increase the slew-rate limit ($\Phi_0 f_{\text{pump}}$, where $\Phi_0 = h/2e$=2.07 fWb) of the modulator by increasing the fluxon pump rate (f_{pump}). The quarter-rate quantizer (QRQ) modulator quadruples the f_{pump} compared to the single-junction quantizer (SJQ). However, this also increases the quantization step by a factor of 4. Assuming that the intrinsic flux noise floor (~ 1 $\mu\Phi_0/\sqrt{\text{Hz}}$) remains the same as the SJQ front-end, we have to quadruple the number of synchronizer channels (m) to get the expected 12 dB increase in dynamic range. In addition to increasing the maximum fluxon transport rate ($f_{max} = 2f_{pump}$), the QRQ front-end demultiplexes the phase-modulated SFQ pulse stream into 4 quarter-rate outputs to facilitate interface with the synchronizer circuit clocked at $f_{clk} = f_{pump}/2$ [9].

The quantizer itself has been tested and found operational up to maximum fluxon transport rates of over 80 GHz [9]. We are currently in the process of designing the ADC with QRQ and 8-channel (m = 8) synchronizer (QRQ-30-8-1) and anticipate a 2-bit performance enhancement from increase in m. The improved transformer design and hence reduced noise floor helps us conceive implementation of the ADC with 16 synchronizer channels (QRQ-30-16-1), enabling a 3-bit performance enhancement. We further conceive implementation of the ADC using the hybrid J_c approach (QRQ-60-8-1), enabling sampling frequency of 60 GHz. However, the relative immaturity of the 3G fabrication process will probably restrict us to m = 8 in the near future. Each of the synchronizer outputs is demultiplexed by two thereby leaving the filter clock frequency unchanged. A total performance enhancement of 3.5 bits is anticipated.

D. Subranging ADC

All of the above approaches use a single range. The subranging approach, widely used in high-performance ADC designs, use multiple ranges to increase dynamic range. In a subranging ADC with two ranges, the signal to be digitized is split between a coarse ADC and a fine ADC. The coarse ADC output is converted back to analog, and subtracted from the input before applying the residue to the fine ADC. The outputs from the coarse and fine ADCs form the most significant bits (MSB) and least significant bits (LSB) of the subranging architecture. Our subranging ADC implementation takes advantage of the oversampled digital data (typically, 1-bit) to simplify the requirement for the digital-to-analog conversion between ranges. The coarse ADC output is a clocked stream of SFQ pulses. Therefore, we use a passive, multi-port superconductor transformer to directly accept and integrate the digitized coarse ADC output, while subtracting it from the analog input with high linearity, and coupling the residual flux into the second (fine) ADC modulator. Another requirement for the subranging ADC is precise gain and time delay matching.

Figure 5 shows the block diagram of the subranging ADC for realization in superconductor RSFQ technology. The coarse and fine ADCs are delta ADCs based on the phase modulation-demodulation (PMD) architecture. The delta ADCs, being slew rate limited, sets an upper bound on the maximum input signal that can be applied. The superconducting subranging architecture enables extension of dynamic range by extending the slew rate limit of an individual ADC modulator. The slew rate of the input signal is K times higher than the maximum slew rate limit of the coarse ADC. To prevent slew rate violation, the input signal to the coarse ADC is attenuated by a factor K. The modulator generates an oversampled 1-bit differential code that represents the discrete derivative of the input signal. This 1-bit oversampled code needs to be integrated to reconstruct the digital equivalent of the input signal. This integrated output is averaged further and read out at the

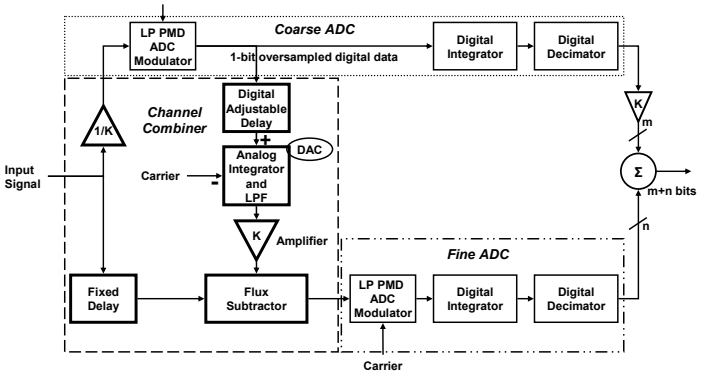

Figure 5. Superconducting implementation of the subranging ADC.

decimated rate to reduce the output bandwidth and increase the ENOB. The output is further amplified by a factor of *K* to compensate for the attenuation at the input of the coarse ADC. These bits form the most significant bits (MSB) of the subranging ADC. Before subtracting from the analog input signal, the digitized derivative from the coarse ADC must be integrated and converted back to analog, both of which is done with superconductor passives. In addition, the signal must be further amplified by the interface gain *K* to match the full-scale input. The remaining error signal is then digitized by the fine ADC to get the LSBs. The digital output of the fine ADC is later summed with that of the coarse ADC to yield a digital output with a larger dynamic range (more ENOB).

The key component in the combiner circuit is the flux subtractor, where the coarse ADC output is integrated and subtracted from the incoming signal (at the same time) to generate the residue signal. Furthermore, the output of the coarse PMD ADC contains the carrier which needs to be subtracted before being fed to the flux subtractor circuit. Moreover, since the 1-bit coarse ADC output contains quantization noise up to very high frequencies (half the sampling frequency), the output needs to be low pass filtered in order to reject the out of band quantization noise. Thus, the feedback DAC must perform carrier subtraction, analog integration of coarse ADC output, low pass filtering to reject quantization noise using superconductor analog filter structure, and amplification to match input signal power using *K*-times amplifier circuit.

The coarse ADC output must be delay matched with the input signal before subtraction in order to minimize the residue. Given unavoidable delays in various parts of the circuit, compensating delays must be inserted to maintain proper timing. A digital adjustable delay, using a controllable shift register can be used for this compensation. In this way, we should be able to adjust for any unforeseen delays in the circuit. Moreover, low-pass filtering of the coarse ADC output causes a change in the phase and magnitude response of ADC output. Hence, in order to optimize the match, the amplitude and phase of the input signal component going to the combiner circuit needs to be adjusted. Further digital adjustment will be necessary before combining the digital outputs of the two channels to account for non-ideal amplification in the gain circuit, as well as other delays. However, this digital adjustment may be accomplished at room-temperature. The ability to provide perfect matching on both analog and digital ends will determine the overall performance of the systems.

We developed a functional MATLAB Simulink model for the subranging architecture and carried out simulations to anticipate the improvement in performance over the traditional low-pass phase modulation-demodulation ADC. Figure 6 shows the power spectrum for the phase modulation-demodulation delta ADC and phase modulation-demodulation subranging delta ADC. The spectrum is for 9.6875 MHz sine wave being sampled at 20.48GHz and decimated by a factor of 256. The second order lowpass Bessel filter with cutoff frequency of 80 MHz is used to reject out of band quantization noise. The coarse ADC output is amplified by a factor of 128 before being subtracted from the input signal and feed to the fine ADC. As seen from Figure 6, the noise floor of the subranging ADC is significantly lower then that of the regular low-pass PMD ADC. Similarly, Figure 7 plots the SNR for the PMD ADC and the subranging architecture vs. the signal power in dBFs. To justify the accuracy of simulation, measured results for the PMD ADC are plotted. The measured results are in close agreement with the simulated performance. The subranging ADC shows a 32 dB gain in SNR at signal power close to the slew rate limit. The simulation does not take into account implementation losses like the imperfections in phase delay matching which might drop the

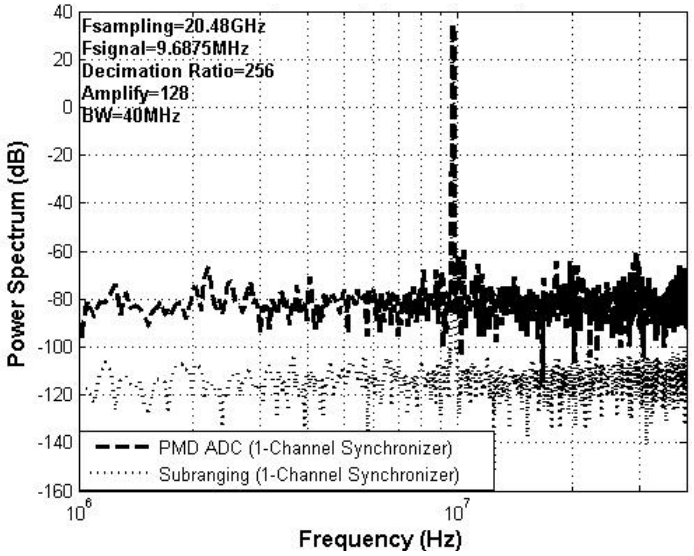

Figure 6. Spectrum from single modulator delta ADC and from subranging ADC. Traces for both the ADCs overlap at the signal frequency.

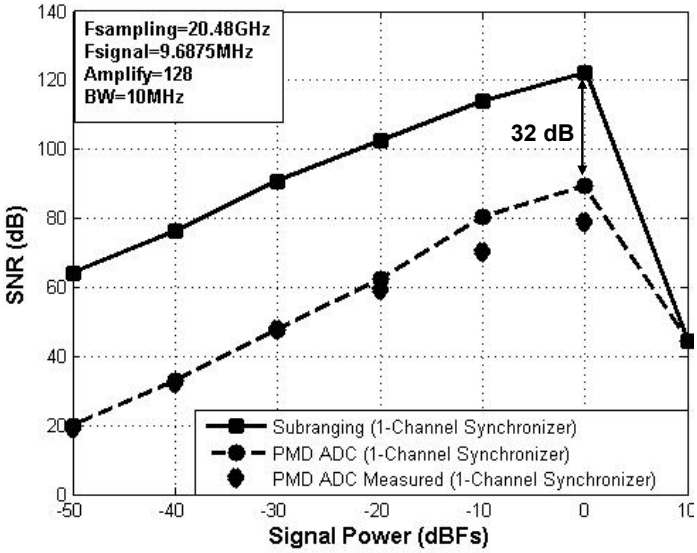

Figure 7. SNR for a single modulator delta ADC and subranging ADC versus signal power. Measured performance of the single modulator ADC plotted for comparison.

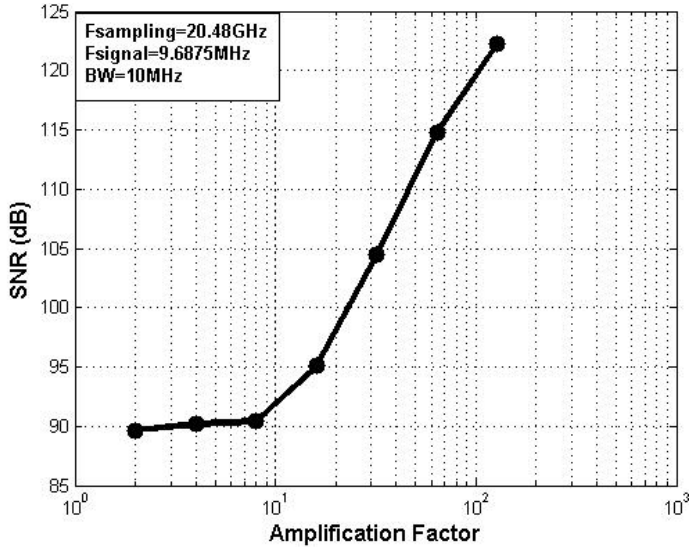

Figure 8. SNR of subranging ADC as a function of Amplification of the coarse ADC output.

projected gain in performance. Figure 8 plots the SNR as a function of the amplification factor of the coarse ADC output. For lower amplification values (up to 8), the performance of the subranging ADC is similar to that of the single modulator ADC. One plausible explanation is the amplitude attenuation in the lowpass filter nullifies any performance enhancement. For simulation we used the simple bessel filter from the simulink tool box. Improved design of the analog filter, reducing the passband attenuation will enable enhanced SNR even for lower amplification ratios.

For the subranging ADC, use of a single channel synchronizer results in 1-bit performance degradation compared to m=2. We are currently in the process of designing a two(2) range subranging ADC with interface gain (K) of 16 (SJQ-30-1-2). A 3-bit resultant performance enhancement is anticipated. The conceived implementation of the ADC with an interface gain of 64 will enable 5-bit gain in the dynamic range. The other design approaches, such as hybrid Jc, multi-rate, QRQ, are all complementary to the subranging architecture. A further conceptual implementation with multi-rate (X2) ADCs will enable 60 GHz sampling frequency (SJQ-X2-60-1-2). Such a design with an interface gain of 128 will result in 7.5 bits performance enhancement.

These projected performance enhancements may be limited by thermal noise, clock jitter, and comparator gray zone. In Figure 3, we have plotted the projected performance points along with the aperture jitter limits. For superconductor ADCs operating at 4 K, thermal noise limits are more than 18 dB lower than room-temperature (300 K) ADCs. Walden [10] gives thermal noise limits for 2000 and 50 ohms effective resistances, which lump together the effect of all noises. Our effective resistance may very well be lower than 50 ohms. Superconductor electronics also offers low-jitter oscillators which may be used to clock ADCs. Jitter of a long Josephson junction clock source has been measured in the 5-10 fs range [11].

CONCLUSIONS

We have presented several credible paths to enhance the performance of the existing low pass PMD ADC with a 2-channel synchronizer. The hybrid J_c approach enables increasing the modulator sampling frequency by fabricating it with a higher-J_c process while the more complex decimation filter is fabricated with a higher-yield lower-J_c process. Performance enhancement of 1.5 bits/octave is enabled. The multi-rate ADC enables increasing the modulator sampling frequency at the expense of a synchronizer channel. A 2-bit performance enhancement has been conceived using this approach. The quarter-rate ADC quadruples the input slew-rate limit. With a corresponding increase in the number of synchronizer channels, up to 3.5 bits performance enhancement has been conceived with the QRQ design. The subranging ADC uses two ADC modulators with an interface gain to increase the total slew-rate limit. Up to 7.5 bits performance enhancement has been conceptualized using this approach.

ACKNOWLEDGEMENTS

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