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Abstract—Many applications of superconductor integrated circuits may require a small part of the circuit to work at the highest possible clock frequency, e.g. an ADC in the receiver front-end, while more complex parts of the circuits may work at a lower frequency, e.g. a digital filter. Since the maximum clock frequency is proportional to the square root of the Josephson critical current density ($J_c$), such circuits can be realized as multi-$J_c$ circuits containing trilayers with different $J_c$'s. A fabrication technology will be presented enabling a single chip to accommodate circuits optimized for different critical current densities. Details of the multi-$J_c$ process will be discussed as well as the typical circuit implementations and test results.

Index Terms—ADC, high voltage driver, MCM, multi-$J_c$, multi-rate, SERDES, superconductor integrated circuits.

I. INTRODUCTION

Existing conventional superconductor electronics fabrication processes have enabled routine fabrication of complex digital-RF receiver circuits with tens of thousands of Josephson junctions (JJs). A number of digital-RF circuits have been successfully demonstrated to work up to 30 GHz operating frequency, fabricated by a process with a medium critical current density ($J_c$) ($4.5 \text{kA/cm}^2$) JJs [1], [2]. In order to double the operating speed, the critical current density of JJs needs to be increased at least by a factor of four. For complex circuits the transition from lower to higher-$J_c$ process can be challenging in the frameworks of the conventional fabrication process, given the fact that yield diminishes significantly with $J_c$ [3], [4]. A multi-$J_c$ process, which can be implemented on a number of designs extending from as small as a single junction to as big as a chip in the same wafer, offers a host of advantages over conventional fabrication process that would make the transition from low to high-$J_c$ process smooth. Some of the advantages include:

a) **Optimum multi-rate complex circuits.** A multi-$J_c$ process would narrow the gap of the operating speed versus complexity of circuits by providing a means to implement different parts of a given circuit with different critical current densities. An example of such a multi-rate implementation is a digital-RF receiver having its front-end (with hundreds of JJs) made in a high-$J_c$ process that enables faster sampling rate, while the more complex part (digital filter with more than ten thousand JJs) made in a lower-$J_c$ process. For a first order delta modulator, every doubling of sampling frequency gives an additional 9 dB in signal-to-noise ratio (SNR). The clock rate transition between different sections of the circuit requires de-multiplexing of the modulator output to multiple streams [5]. Ultimately, the multi-$J_c$ implementation would make the ADC work at much higher rate and allow it to be fabricated with practically viable yield. The optimum multi-rate digital RF circuits design strategy would be to clock the ADC faster for higher SNR and keep complex digital channelizer circuit at lower-$J_c$ (more mature) processes, and use SERDES (SERializer DESerializer) design approach to route data and clock.

b) **Higher amplitude and faster output voltage drivers.** Output voltage amplifiers (with less than a hundred of JJs) of a digital circuit can be implemented in an even higher-$J_c$ process (e.g., $50 \text{kA/cm}^2$ and beyond), increasing the output voltage to the maximum possible ($>1.6 \text{mV}$) as well as the maximum possible output data rate ($>100 \text{Gb/s}$). Both the output voltage and the data rate scale proportionally with the square root of $J_c$ [6]. Higher speed digital links with SERDES design strategy would enable simpler cryo-packaging, lower heat load and simpler data interface to room temperature electronics.

c) **Additional multi-scheme.** Implementing multi-project, multi-chip approach on the same wafer is one of the cost effective solutions for superconductor electronics. Multi-$J_c$ implementation would add one more dimension to the scheme. The three dimensional scheme would now allow the fabrication of a number of different chips for a number of projects with a variety of critical current densities on the same wafer. Such a scheme would drive down the cost of research and development by cutting the fabrication cost significantly. Moreover, simpler on-chip implementation can replace a hybrid-$J_c$ multichip module (MCM) into a single multi-$J_c$ chip where space is not a constraint.

d) **New venues:** RSFQ control circuit for superconducting quantum computing circuits could be implemented on the same chip using a multi-$J_c$ process. The two extreme $J_c$'s, $30 \text{A/cm}^2$ for quantum computing and at least $1.0 \text{kA/cm}^2$ for RSFQ circuits, can be conveniently designed and fabricated on the same chip. Moreover, multi-$J_c$ quantum computing chips can be processed...
alongside RSFQ chips with the addition of a few extra masks for the junction and resistor layers. Combining these two processes together would result in a considerable decrease in the number of fabrications steps. Besides the standard trilayer (Nb/Al/AlOx/Nb) implemented in HYPRES processes, multi-Jc process now provides the means for implementing and testing new trilayers for high speed RSFQ applications, such as with co-sputtered Nb-Si barrier [7], or NbTiN/GaN/Nb/TiN [8] to name a few.

Fig. 1 shows a digital RF receiver circuit implemented with tri-Jc process, exploiting some of the advantages above. In this paper we will give details of the multi-Jc process from design and fabrication perspective, proof of concept implementation and results.

II. MULTIJc FABRICATION PROCESS

Conventional HYPRES fabrication process implements 12 physical layers using 13 photomasks with an overall 44 fabrication steps to make circuits in 30 A/cm², 1 kA/cm² and 4.5 kA/cm² [10]. For an n - Jc (n = dual, tri, etc.,...) process the number of physical layers in the structure remains the same whereas the number of photomasks increases by n, and the extra processing steps by 8 x n. In Fig. 2 the layout of the three additional masks required to make the tri-Jc digital RF transmitter (Fig. 1) is shown.

The first mask, T1, is a dark-field mask for defining the lowest-Jc area. T2 and T3 are clear-field masks needed to define areas for medium and high-Jc processes respectively.

From design perspective, the designer has the liberty of using arbitrary shapes to allocate different regions to the different Jc’s, subjected to the following design rules:

- Areas defined by the clear field mask must be completely inside the areas defined by the dark field mask. The minimum spacing between the two areas is 1 μm everywhere, with the exception of a few predetermined overlap areas intended to provide the necessary electrical continuity between different regions, e.g. as shown in Fig. 2. No wire crossing the overlap areas is allowed. This rule protects against interlayer shorts for the lines crossing the overlap.

These overlaps may not be necessary if there are enough I0 contact holes (see cross-section in Fig. 4 for layers description) connecting different trilayers through the ground metal layer M0.

- Since the base electrodes of the n different trilayers on the wafer and the n different resistor materials are not continuous everywhere, no M1 and R2 feature is allowed to cross the boundary of the regions of different Jc. The minimum separation between the boundary and the M1 and/or R2 features is 2 μm.

- Depending on the design, circuits may not be tied together for biasing on the same bus.

- All Josephson junctions in the areas with different Jc on the wafer are defined at the same lithography step, using the counter electrode mask I1C (lowest-Jc process), so the junctions for the medium and high-Jc areas need to be appropriately scaled and placed in I1C.

On the fabrication side the key is the "lift-off process". Following the completion of M0 and I0 layers Fig. 3(b), "image reversal" photolithography is done using the dark field mask—T1. This clears the photoresist in the dark areas of the photomask and creates a negative slope of the photoresist edge (mushroom-shape) for the trilayer lift-off. In order to reduce out-gassing and improve adhesion, the resist is hard-baked for 10 min at 110°C and the patterned wafer is cleaned in oxygen plasma for 30 s before the first (lowest-Jc) trilayer deposition.

After the deposition the wafer, is soaked in acetone for a few hours to lift-off the trilayer and, cleaned in the ultrasonic bath. This step places the lowest-Jc trilayer on the areas defined by T1 mask. The next step is again an image reversal photolithography using the clear field mask T2, which will cover everything except the islands on the wafer dedicated for the medium-Jc process, Fig. 3(c). The deposition and lift-off of medium-Jc trilayer is done in a similar fashion to the low-Jc trilayer. The process is repeated again using the clear field mask T3 for the highest-Jc trilayer, and so on if more than three current densities are used. The success of the lift-off process is heavily dependent on the image reversal photolithography, which creates a resist profile that prevents continuous edge coverage during metal deposition. That coupled with a reasonably thick photoresist (in
our case 10 times thicker than the trilayer thickness), results in a relatively easy lift-off process.

After all the trilayers have been deposited and lifted-off, the wafer is ready for the junction counter electrode definition step. This step and the next three processing steps (anodization and junction base electrode definition) are exactly the same as in the conventional fabrication process [9]. The cross-section of the thin films after these steps is shown in Fig. 3(d). Special attention must be paid for the definition of the resistors, since in principle each \( J_c \) region may require different resistor materials. The allocation is done in exactly the same way as for the trilayers, using the T1, T2 and T3 masks while depositing the appropriate material for respective region.

For the case considered in Fig. 1, the material of choice for the different regions could be molybdenum for the lowest-\( J_c \) process, molybdenum nitride of different thickness and composition for the medium and highest-\( J_c \) processes [3]. The junctions in the highest-\( J_c \) process could well be self-shunted; be that as it may, resistor material would still be needed to make the bias-resistors for the circuit in the highest-\( J_c \) region. The resistors are then defined using the R2-mask as in the conventional process and etched at the same time using reactive ion etching. In the case of different etch rate, etch conditions or different materials (e.g., gold-palladium for quantum computing circuits), there will be a need for separate R2 masks for the different regions. The rest of the fabrication steps (11B, I2, M3, R3) remain the same as in the conventional fabrication process, whereas M2 and M2-A need to be consolidated together so as to appropriately define the matching resistors in the different regions. The final cross-section of the driver-receiver pair between the regions with different \( J_c \) is shown in Fig. 4.

III. CIRCUIT IMPLEMENTATION

To test the viability of the multi-\( J_c \) process, the concept has been implemented as dual-\( J_c \) process using HYPRES’ current processes \((1.0 \text{ kA/cm}^2 \text{ for low-} J_c \text{ and } 4.5 \text{ kA/cm}^2 \text{ for high-} J_c \text{ part})\). The test structures that have been fabricated include:

I. An array of 100 unshunted JJs connected in series along one line covering about half of the active width of chip. The array was placed on both the low- and high-\( J_c \) parts. Besides critical current density targeting information, the structure has been instrumental in uncovering the effect of multi-\( J_c \) on junction quality. Five series arrays of 30 shunted JJs different sizes were used for determining the critical current density. These are purely analog diagnostic circuits.

II. As a transition to digital domain and to test the maximum operating frequency, a digital frequency divider circuit has been implemented in both parts. This, like any other standard benchmark test, is based on the divide by two operation of the T-flip flop. While the circuit is digital, the test is analog (the average input and output voltages are measured as a function of circuit bias).

III. To test the digital domain and the transfer of data within the multi-\( J_c \) circuits, we have designed a chip containing a DC-to-SFQ converter fabricated in the \( 1.0 \text{ kA/cm}^2 \) process, which provides data to the amplifier circuit fabricated in the \( 4.5 \text{ kA/cm}^2 \) process. The interface between circuit-components fabricated in different \( J_c \) is provided via passive transmission lines. Both the output speed and voltage of the amplifiers are expected to double for the high-\( J_c \) process.

All of the above test structures were assembled in two \( 5 \times 5 \) mm chips as shown in Fig. 5.

IV. TEST RESULTS

The multi-\( J_c \) process was implemented on 14 out of the 310 chips on the wafer. Fig. 6 contains the results obtained from the array of 100 unshunted JJs. The arrays were of sizes from 1.0 to 3.0 PSCAN [10] units placed on both the low and high-\( J_c \) areas. The Josephson junction quality was not affected by the multi-\( J_c \) process, as indicated by \( V_m \) of 13 mV and 42 mV for the high and low-\( J_c \), respectively.

All the results of our measurements, done in automated setup—OCTOPUX [11], indicate that there is no difference...
between junctions made by conventional process and that of the multi-Jc process both in terms of quality and uniformity.

Fig. 7 summarizes the results obtained from the digital frequency divider (DFD) circuit for benchmark test of the maximum operating frequency. The T-Flip-Flop (TFF) circuit employed has an additional inductively coupled bias (skew-bias) to tune the quantizing inductor of the circuit. For DFD circuit results shown in Fig. 7 the optimum skew bias was found to be 0.65 mA and 0.25 mA for the high and low-Jc, respectively. The TFF-bias was then scanned to obtain the margin of operation of the DFD. Fig. 8 shows the low speed test results for the differential SFQ-to-DC amplifier [8] fabricated by the multi-Jc process. A sinusoidal signal applied to the DC-to-SFQ generates two data phases that act as SET and RESET pulses for the amplifier. Additional SFQ-to-DC monitors are fabricated in the 1.0 kA/cm² process to monitor the SET and RESET pulses as well as to verify the voltage doubling from the amplifier fabricated in the 4.5 kA/cm² process. As seen in Fig. 8, the voltage output from the differential amplifier in the higher-Jc process is twice the voltage output from the amplifier fabricated in the lower-Jc process.

V. CONCLUSION AND FUTURE DEVELOPMENT

We have successfully developed a multi-Jc process that would enable circuits optimized for different critical current densities to be fabricated together on the same wafer. The process has been successfully tested as a dual-Jc process on circuits designed for 1.0 kA/cm² and 4.5 kA/cm² critical current densities. A number of chips for the 1.0–4.5 kA/cm² dual-Jc have been fabricated and tested, including analog and digital diagnostics, DFDs, etc.

Next generation of multi-Jc circuits optimized for 4.5 and 20.0 kA/cm² dual-Jc include: circuits for analog-to-digital conversion, high voltage drivers, digital frequency dividers, 4-stage counter, digital and analog diagnostic chips are being fabricated.

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REFERENCES


