# HIGH PERFORMANCE, ALL DIGITAL RF RECEIVER TESTED AT 7.5 GIGAHERTZ

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## ABSTRACT

*Wireless applications would be less expensive, more flexible, and more robust if they had more digital and less analog circuitry. The problem is implementing digital signal processing at radio frequencies. Conventional data converters (ADCs and DACs) and digital circuits are simply not fast enough, especially at SATCOM frequencies. However, superconductors can provide ultra fast mixed signal and digital circuits with the linearity and dynamic range required for true direct, digital-RF processing. These superconducting circuits are digital ICs based on Josephson junctions and "rapid-single-flux-quantum" logic (RSFQ), where simple circuit switching speeds up to 750 GHz have been demonstrated. This permits direct conversion between analog RF and digital baseband signals, replacing frequency and protocol-specific analog hardware with flexible digital processors. HYPRES recently developed and delivered an X-band All Digital RF Receiver (XADR) prototype system for the US Army CERDEC and PM DCATS. The concept of this ADR is to replace the entire analog RF receive chain between the antenna and the baseband demodulator with a high performance digital RF equivalent. The first XADR prototype system has been successfully demonstrated at the Joint SATCOM engineering Center (JSEC). End to end link testing, over the satellite has been successfully completed using an existing AN/GSC-39 X-band earth terminal, an XTAR satellite, the X-band ADR and a SATCOM modem.*

## INTRODUCTION

Future military and commercial radio frequency (RF) systems demand better utilization of the RF spectrum, moving towards higher frequency, greater bandwidth, and greater flexibility to accommodate diverse modalities (e.g. voice, data, video, detection and ranging, electronic countermeasures). This requires extension of digital processing to the traditionally analog RF domain. Superconductor rapid single flux quantum (RSFQ) electronics, featuring ultrafast digital logic and high-linearity analog-to-digital converters, allows direct conversion of RF signals and digital processing of the digitized RF signal up to SATCOM frequencies [1]. Recently, a family of digital-RF receivers (called ADRs), comprising an oversampled delta or delta-sigma modulator performing analog-to-digital conversion and a digital channelizer circuit performing digital down-conversion and filtering, have been realized using superconductor integrated circuit technology [2]. Among these, the one with the highest input frequency is the X-band digital-RF receiver (called XADR).

Until now, these ADR chips were tested in the laboratory, primarily by immersion in a liquid helium dewar, and evaluated with input signals generated from test equipment. We have built a complete system prototype by integrating the XADR chip with a commercial cryogen-free closed cycle refrigerator (called cryocooler). Here, we report the first demonstration of this superconductor digital-RF receiver prototype with live X-band satellite signals at the Joint SATCOM Engineering Center (JSEC).

## X-BAND DIGITAL-RF RECEIVER

Direct digitization of X-band SATCOM signals is performed by a single 1-cm$^2$ superconductor integrated circuit, called the XADR chip (Fig. 1).

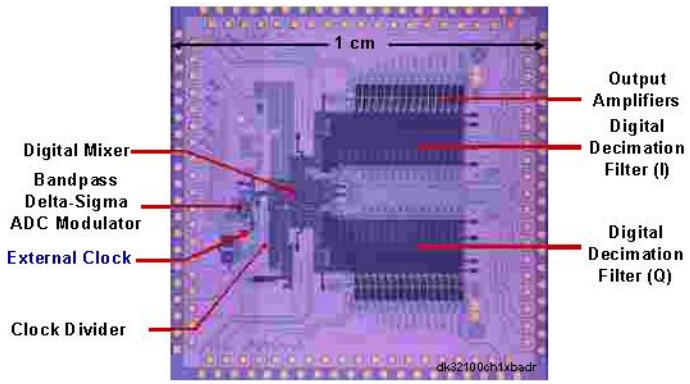


*Fig. 1. Single-chip digital-RF X-band receiver (XADR).*

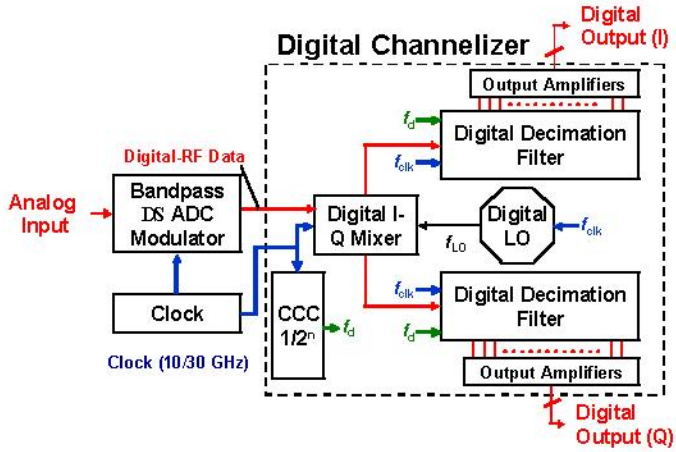


*Fig. 2. Block Diagram of the XADR chip.*

Based on this XADR chip, we have developed a satellite communication digital receiver demonstrator. The chip is cooled by a commercial two-stage closed-cycle refrigerator (Sumitomo SRDK-100) to about 4 K. The chip (Fig. 2) comprises a bandpass second-order delta-sigma analog-to-digital converter (ΔΣ ADC) circuit, and a digital channelizer circuit, both clocked by a common high-frequency clock ($f_{clk}$). Analog RF input is applied directly to the ΔΣ ADC modulator, and is converted into an oversampled single-bit data stream. The channelizer circuit digitally down converts and filters this digital-RF data stream to produce a pair of digital in-phase ($I$) and quadrature ($Q$) words at a reduced (decimated) output clock rate of $f_d = f_{clk}/2^n$, where $2^n$ is the decimation ratio. Digital $I$ and $Q$ mixing is performed by multiplying the ADC output by two digital local oscillator streams with exactly 90° phase difference, derived from the ADC sampling clock. In this design, the local oscillator frequency is $1/4^{th}$ of the clock frequency. The multi-bit digital I and Q outputs of the decimation filters are amplified to about 2 mV with a set of on-chip drivers. The chip consumes less than 4 mW of power, far less than the cooling capacity (200 mW @ 4.2 K) of the commercial cryocooler.

These mV-level digital I and Q outputs, along with the corresponding clock signal ($f_d$), are amplified by a set of custom-designed high-gain amplifiers to about 3.3 V. The signals are then acquired using a commercial circuit board with field programmable gate array (FPGA) chips. We have built a programmable data acquisition interface that can also function as a second-level channelizer for extraction of sub-bands. In addition to acquiring the digital I and Q data, the interface board permits their transfer to any back-end signal processor, such as a digital MODEM. The block diagram of the XADR demonstrator unit is shown in Fig. 3.

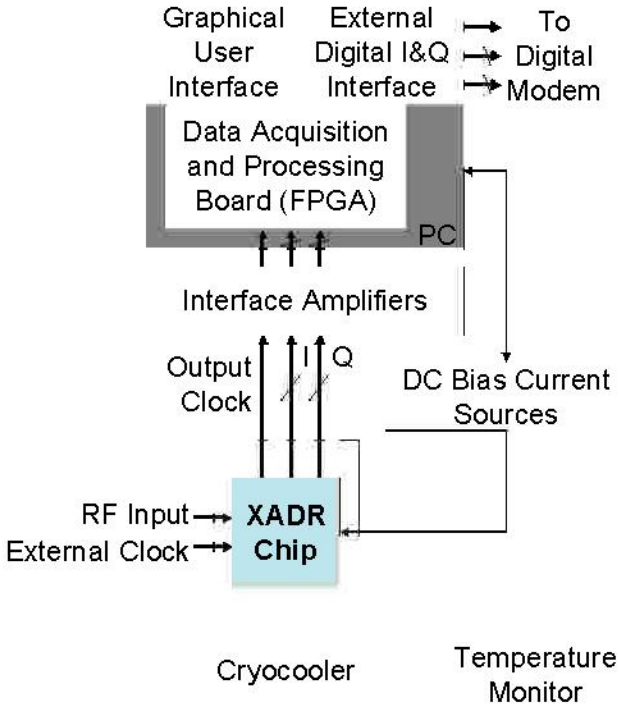


*Fig. 3. Block diagram of the XADR system prototype.*

## SUPERCONDUCTOR BANDPASS DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTER DESIGN

A bandpass ADC was chosen to minimize the quantization noise in the band-of-interest (7.25-7.75 GHz). The ADC modulator is a continuous-time bandpass delta-sigma modulator with two lumped LC resonators. In this implementation of the bandpass ADC, the first and the second resonators were designed to be 7.4 GHz and 7.6 GHz respectively. The quality factor of the resonator was estimated to be around 100. We introduced a string of junctions as a tunable inductor for possible tuning of the resonant frequency, but did not use it in this test.

One of the unique features of the superconductor delta-sigma ADC modulators is implicit feedback: when the bottom junction (J2) of the two-junction clocked comparator switches, it subtracts a single flux quantum (SFQ, $\Phi_0$ = 2.07 fWb) from the input while producing a digital output SFQ pulse. Therefore, no explicit feedback loop is needed to construct a first-order ADC modulator. A second-order modulator was designed to improve signal-to-noise ratio (SNR) by further suppression of quantization noise. Fig. 4 and Fig. 5 show a block diagram and the corresponding schematic diagram of our second-order ADC modulator. The feedback path includes Josephson transmission lines (JTLs) as active delay elements in addition to a D flip-flop to control the phase of the feedback signal.

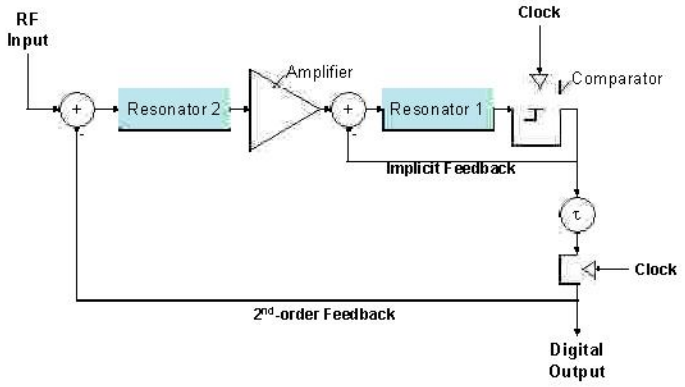


*Fig. 4. Block diagram of the second-order bandpass DS ADC modulator.*

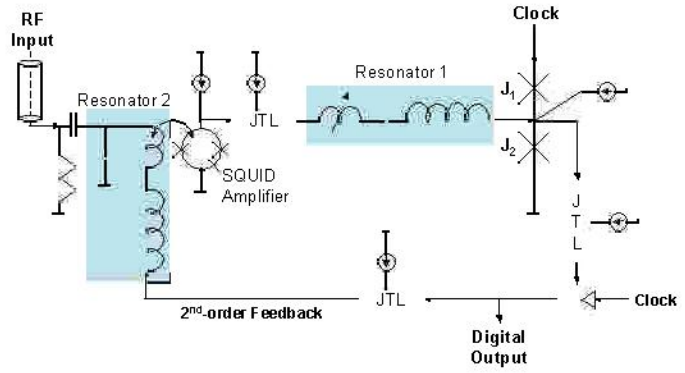


*Fig. 5 Schematic diagram of the second-order bandpass DS ADC modulator.*

In its simplest implementation, the clock frequency for a bandpass ΔΣ ADC is chosen to be $f_{clk} = 4f_0$, *where* $f_0$ *is the center of the band-of-interest.* For X-band, this clock frequency is about 30 GHz. One can also use a lower clock frequency with some performance penalty. In this scheme, called RF undersampling, we take advantage of the sampling process that replicates the input analog frequency band, centered at $f_0$, translated by multiples of the sampling frequency ($f_{clk}$). In general, the sampled spectrum consists of an infinite number of band replicas at $\pm f_0 \pm nf_{clk}$, where n = 0, 1, 2, …, but we are primarily interested in the first Nyquist zone $0 < f < f_{clk}/2$. For $f_{clk} > f_0 > f_{clk}/2$, the band center is shifted from $f_0$ to $f_{clk} - f_0$. We will then need to apply a digital local oscillator at that frequency ($f_{LO} = f_{clk} - f_0$) to mix it down to baseband. Furthermore, the local oscillator should be a submultiple of the clock frequency to prevent unwanted mixer artifacts, preferably by a factor divisible by 4 to ensure convenient generation of in-phase and quadrature components. Under these constraints, the clock frequency is given by $f_{clk} - f_0 = f_{clk}/4$, *or* $f_{clk} = 4f_0/3$, which for X-band is about 10 GHz. We designed two versions of the XADR chip, for fabrication using our first-generation (1 kA/cm$^2$) and second-generation (4.5 kA/cm$^2$) processes, for target clock frequencies of 10 GHz and 30 GHz respectively.

## DIGITAL-RECEIVER DEMONSTRATION

In collaboration with L-3 Communications, we have successfully interfaced the superconductor X-band digital-RF receiver with L-3's 3rd generation digital modem, which was specially configured to accept and demodulate digital I and Q digital data. The complete receiver system demonstrator unit was tested with live satellite signals at HYPRES first, and then at the Joint Satellite Engineering Center (JSEC) in Ft. Monmouth, NJ, where it received signals from the XTAR satellite at the GSC-39 terminal.

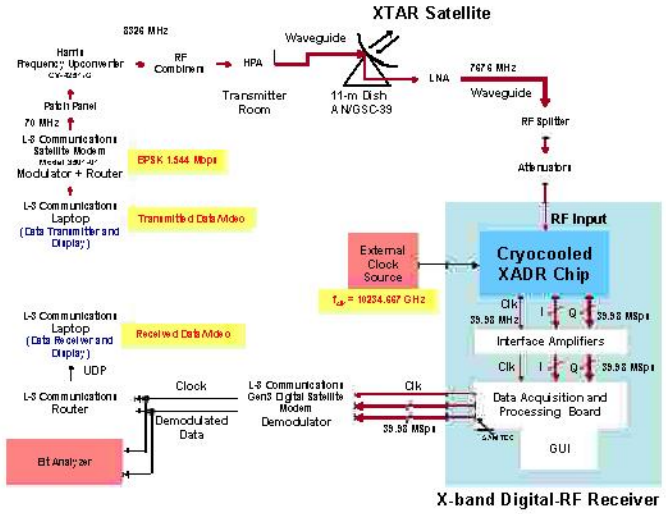


*Fig. 6. Configuration for the X-band Digital-RF.*

The setup for the demonstration is shown in Fig. 6 above. We started by generating a data enriched RF stream, originating from a typical user data stream from a computer feeding into a modulator through a typical router. We chose an uncoded binary phase shift keying (BPSK) modulation onto a 70-MHz intermediate frequency (IF) carrier at a modulation rate of 1544 kbps (T1). From there, the signal was injected into a two-stage frequency up-converter. The first stage heterodyne mixer performed mixing of the 70 MHz (modem output) with an internally oscillated 630 MHz, producing the sum (700 MHz) and the difference (570 MHz) frequencies in addition to frequency components at the inputs of the mixer. The signal was then band pass filtered to allow only the sum (700 MHz) to continue. The signal then traversed to another heterodyne mixer that again produced the sum, the difference and the two original inputs but having one primary difference: the internal oscillating input for this second stage mixer was tunable ranging from 7.2 GHz to 7.7 GHz with the filtered output ranging from 7.9 GHz to 8.4 GHz. From here the analog signal is data enriched X-band. For our test, we chose the center frequency to be 8326 MHz.

The modulated X-band RF signal was amplified to high power using a traveling wave tube (TWT) amplifier. The amplified signal then traversed a low-loss waveguide to an antenna, with an effective gain of 57 dB, and was radiated to space with a circular polarization. The loss to the satellite, approximately 22,380 miles away, is 202 dB. On the satellite, the signal was amplified, frequency shifted down by 650 MHz, to a range of 7.25 to 7.75 GHz, and amplified again before being transmitted back down to earth. Departing the satellite, the signal underwent circular polarization again and another 202 dB of loss. The signal was collected by the 57 dB gain aperture much in the same fashion as it was transmitted except its lower frequency and opposite polarization. Immediately upon arrival, the signal was amplified by a 73 dB low-noise amplifier (LNA). The signal then traversed more waveguide to a bank of RF splitters and a set of fixed and variable attenuators before being applied to the X-band digital-RF receiver. For our chosen carrier, the input RF signal was $f_0$ = 7676 MHz.

The XADR chip sampled the 7.676-GHz analog RF input directly with an applied $f_{clk} = 4 f_0 / 3 = 10.234667$ GHz, and digitally down converted down to baseband. The decimation filter ratio was 256, and consequently, the output (decimated) clock rate was $f_d = f_{clk}/256 = 39.98$ MHz. The output digital I and Q data at 39.98 Msample/s were amplified and passed through the FPGA data acquisition board and interface to the L-3 digital modem. Upon demodulation, the signal was passed through the router in its packet form to be acquired and displayed by the destination computer. We also acquired the data from the data acquisition and processing board and performed

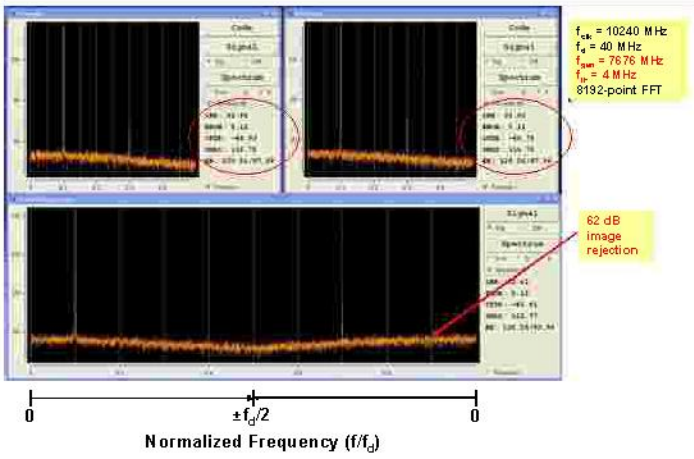


*Fig. 7 The graphical user interface displays the spectra of the digital I (top left) and Q (top right) outputs shown along with that of I+jQ (bottom).*

Fig. 7 shows the performance of the XADR chip in terms of signal-to-noise ratio (SNR) and spur-free dynamic range (SFDR) over the 40 MHz band with a single-tone RF input signal. In addition to testing with pseudo-random patterns, we demonstrated the XADR system with live transmission and reception of a video file. The spectrum (Fig. 8) shows the digitally down-converted signal-of-interest on either side of $f = 0$.

During this demonstration, there were other communication signals present in the same band. The closest in frequency was a transmission centered at 7679 MHz, from GSC-39 to a small mobile terminal, with 10 dB more power than our signal-of-interest. These signals were also digitized by the XADR chip, and could be extracted from the same digitized data using a set of second-level channelizers [2]. In other words, the ADR permits extraction of multiple sub-bands from a broad digitized band. Also, the XADR chip supports much higher data rates than the 1.544 Mbps used for the live demonstration based on available satellite bandwidth. In the laboratory, we have digitized X-band carriers modulated at rates up to 6.5 Mbps, limited by the available modulator equipment.

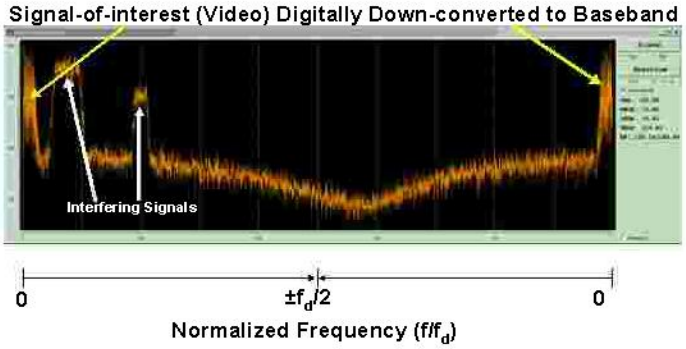


*Fig. 8 The spectrum of the received signal of interest with the input being a 7676 MHz signal modulated at 1.544 Mbps with a packetized video file. The XADR also captured other signals in the same transmitted band, at 7.679 and 7.684 GHz respectively. The clock frequency is 10234.667 MHz.*

We also noted that the level of noise received from the antenna was significantly higher (by about 20 dB) than the ADC quantization noise floor. We estimated the total losses between the receive LNA and the RF input port of the cryopackage unit to be 70-72 dB. This does not include the RF cable loss inside the cryopackage, between the input port at room temperature and the 4-K chip, which was not minimized to keep the conductive heat load on the cryocooler low. Therefore, we expect that this XADR system could be placed directly behind the antenna, eliminating the need for amplification.

Finally, better performance is expected from an XADR chip clocked at higher frequency. Fig. 9 shows the spectrum of a 7.653 GHz RF input signal that has been

digitized at $f_{clk} = 4 f_{LO}$ = 30.592 GHz and digitally down-converted to 5 MHz. The decimation ratio is 256 and the output sampling rate is 119.5 MHz. Compared to the results obtained with 10 GHz clock, both SNR and SFDR are higher over a larger bandwidth.

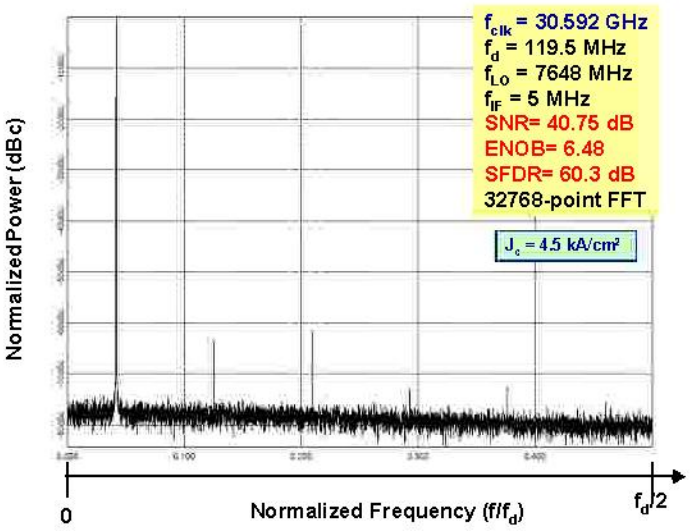


*Fig. 9 Spectrum of the digitized output from an XADR chip clocked above 30 GHz. The applied analog input signal is 7.653 GHz.*

## CONCLUSION

We have developed and demonstrated a complete digital receiver prototype system, featuring direct digitization of X-band Military Satellite Communications (MILSATCOM) signals. A superconductor integrated circuit chip, consisting of a bandpass delta-sigma ADC modulator and a digital channelizing circuit both clocked above 10 GHz, was used to convert RF signals in the 7.25-7.75 GHz range to digital and perform down-conversion and filtering completely in digital domain. This system was interfaced with a MIL-STD-188-165A modem, and was used to demonstrate live data and video traffic in an existing Army Earth Terminal, i.e., AN/GSC-39 terminal over a live Satellite link. It has achieved initial Technology Readiness Level (TRL) 6 capability by operating in a relevant environment. More testing will be performed in the near future when the optimized version of the XADR chip to be clocked at 30 GHz is ready for system integration.

The X-band ADR concept is just a first stepping stone toward an All-Digital-RF Transceiver (ADT) architecture for future SATCOM Earth Terminals. The overall goal of the ADT is a true software-defined SATCOM Earth Terminal, which will provide direct RF digitization of the whole satellite payload bandwidth for all incoming signal carriers from the antenna and consolidate all digital-RF distributions from the antenna into a single all-digital software-defined platform from RF to baseband. In terms of increased capability, this will allow us to have programmable and flexible multi-band multi-mode communications across multiple satellite transponders or different satellite payloads simultaneously. In terms of increased performance, this will allows us to have greater G/T improvement on the receive-side and greater power efficiency on the transmit side, due to the intrinsic low noise temperature and direct digital-RF processing using superconducting digital circuits. In terms of program acquisition and logistic cost, this will eliminate multiple racks of legacy equipment, such as, IF cablings, analog RF switch panels, analog IF up/down converters, and analog IF modems. Fig. 10 below shows the concept of the multi-band All Digital-RF transceiver architecture for future SATCOM earth terminal.

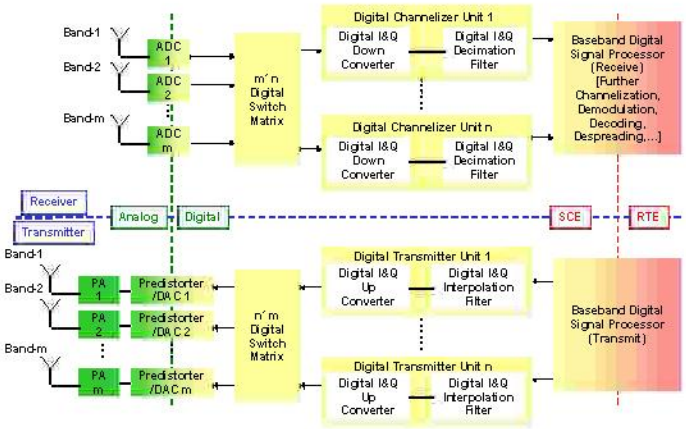


*Fig. 10 Multi-band, multi-channel digital-RF receiver architecture.*

## ACKNOWLEDGMENT

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