Integrated Millimeter/Submillimeter Superconducting Digital Spectrometer

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***Abstract*—Compact mm/submm integrated spectrometers are required for radio-astronomical research, remote monitoring of the Earth atmosphere and environmental monitoring for hazardous materials of chemical and biological origin. Assembled on a multi-chip module the all superconducting integrated spectrometer offers integration of thin film analog components such as a mixer, superconducting local oscillator and an intermediate frequency SQUID amplifier together with superconducting digital circuitry. A Rapid Single Flux Quantum (RSFQ) 128-bit autocorrelator formed by 16-bit autocorrelator and a 112-bit programmable shift register that adjusts the data delay in increments of 16, is used for digitizing of the down converted signals and real-time digital processing. Experimental results showing both operation of components and the way to their successful integration are presented.**

***Index Terms*—Compact and sensitive spectrometer, multichip module, remote monitoring, superconductor digital electronics.**

I. Introduction

THE Superconducting Integrated Spectrometer (SISP) offers a unique integration of different planar components such as a SIS (superconductor-insulator-superconductor) mixer, a superconducting local oscillator (LO), an intermediate frequency (IF) SQUID amplifier, and the circuits for digitizing of the down converted signals and real-time digital processing.

The SIS mixer is the device of choice for a low noise front-end detector at frequencies from 100 GHz to over 1 THz. Since the noise temperature of an SIS mixer is ultimately limited only by the fundamental quantum value hf/k [1], SIS heterodyne receivers have been successfully used in radio astronomy for observation of spectra with the lowest possible noise temperature in the mm and sub-mm wave range.

Many applications lack a compact and easily tunable submm LO. At frequencies above 30 GHz there is a steep increase in the cost and complexity of solid state radiation sources. Gunn diodes are widely used as LO. They have the highest fundamental frequency of operation among commercially available mm wave sources up to $\sim$100 GHz. Extension to higher frequencies requires low efficiency harmonic generators. Moreover, Gunn diode sources are voltage tunable over a range typically less than $\pm 10\%$ of the resonant frequency of the oscillator. This tuning range is inadequate for many applications.

An RF amplifier, which may be attached to the IF port of the SIS mixer, is very attractive since it helps to avoid losses of the long cable. A semiconducting IF amplifier integrated with SIS mixer has a drawback of significant heat load. This makes an RF amplifier based on a SQUID that has a low power consumption, small size and "natural" compatibility with any superconductor based structure a natural choice for integration with the SIS mixer.

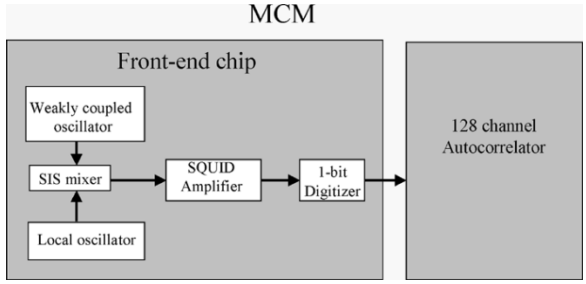

Fig. 1. The block diagram of integrated spectrometer mounted on MCM module. See text for details.

A 128-bit autocorrelator formed by 16-bit autocorrelator and a 112-bit programmable shift register that adjusts the data delay in increments of 16 is used as a backend device for a fully integrated spectrometer. The concept is based on employing ultrafast RSFQ elements in a digital correlator architecture that is well developed for semiconductor circuitry. The first version of a fully integrated 16-channel RSFQ autocorrelator operating at 11 GHz has been already realized [3].

Although the concept of an integrated spectrometer is not new (see review by Koshelets and Shitov [2] and references therein), the main efforts in its development targeted the successful on-chip integration of such *analog* components as LO and SIS mixer with quasioptical antenna [2]. In this paper we focus on integration on a multi-chip module (MCM) of superconducting thin film *analog* components (LO, mixer, and IF amplifier) together with superconducting *digital* RSFQ circuitry that offers a real breakthrough.

II. Integrated Digital Spectrometer

Fig. 1 shows the block diagram of the integrated spectrometer under development. The superconducting part of the receiver consists of two chips mounted on a MCM.

This chip die sizes are 5 and 10 mm. The first 5 mm chip of the spectrometer, the "front-end" chip, has the local oscillator together with the SIS mixer and impedance matching structure for better power delivery and to tune out the SIS junction capacitance. For easy testability we are developing a self-contained spectrometer, e.g. no actual outside signal is investigated and this outside signal is modeled by an on-chip oscillator, very similar to the LO only with weaker coupling to mixer. The mixed-

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down signal is digitized by 1-bit digitizer (modulator). The typical noise temperature of the 1-bit digitizer is of order of few hundred K, which is significantly higher than the noise temperature of about 40 K at 475 GHz for a reference SIS mixer pumped by an external local oscillator [2]. Therefore, an IF amplifier with a power gain G_A of about 10 dB and a noise temperature T_N of about 100 K necessary to achieve the best possible overall noise temperature is designed on the same front-end chip.

The second 10 mm chip has a digital-signal processing circuit, a 128-channel autocorrelator formed by 16-lag autocorrelator and 112-bit programmable delay shift register (PRSR). The PRSR acts as programmable (in increments of 16) delay line; data flow from 16-lag autocorrelator to the PRSR and then come back.

III. Front-End Chip

Unidirectional fluxon (flux quantum $\Phi_0 = \mathrm{h/2e}$) propagation in a long Josephson tunnel junction (LJJ) is used as a way to achieve a practical and compact on-chip LO. A Josephson junction is defined as "long" when its physical length $\mathrm{L} \gg \lambda_\mathrm{j}$ and the width $\mathrm{W} \ll \lambda_\mathrm{j}$, where Josephson penetration depth λ_j is the characteristic dimension of an unperturbed fluxon. A fluxon in a long Josephson junction (LJJ) carries a magnetic flux equal to one flux quantum Φ_0. A dc magnetic field H is applied in the plane of the junction. With increasing the external magnetic field, the screening current at the junction edge becomes unstable and forms a closed loop, which enters the interior of the junction. Fluxons are continuously generated at one junction end, and accelerated by the bias current toward the other end. Here the reflections generate a regular standing wave pattern resulting in emitted radiation.

The oscillation frequency is described by the formula: $f = V_{dc}/\Phi_0 = ud\mu_0 H/\Phi_0$, where d is the magnetic thickness of the junction and μ_0 is the permeability free space. The average velocity u of fluxons is proportional to the bias current.

The oscillation frequency can be tuned over the wide range by changing the applied field, by varying the fluxon density in the junction, and by changing the bias current.

All circuits in this paper are fabricated using the standard HYPRES 3 $\mu\mathrm{m}$ 1 $\mathrm{kA/cm^2}$ process [4]. Fig. 2 shows the layout of the chip that incorporates all front-end structures. The chip consisted of the following major parts: the LO in the form of long Josephson junction, SIS mixer, weakly coupled LJJ to model external signal, various transformers for better impedance matching of SIS mixer to LJJ's, SQUID amplifier, and digital circuitry with bandpass delta-sigma modulator to test this structure as a whole. The LJJs/mixer circuitry is designed for better matching for the frequency of 350 GHz. The IF SQUID amplifier has been designed for the 1 GHz bandwidth. LO LJJ and weakly coupled LJJ have to be adjusted within 1 GHz difference around 350 GHz.

All components of the front-end chip have been tested. For the LO/SIS mixer structure, the current-voltage characteristic (I-V curve) of the LO, when a 7 mA current is applied through the control line, exhibited a pronounced flux-flow step at 0.75 mV. At the same time, the I-V curve of the SIS mixer irradiated by the LO, while its Josephson current is suppressed by current through control line and when LO is biased at flux-flow step, exhibits the photo-assisted tunneling step at hf_{RF}/e below the gap.

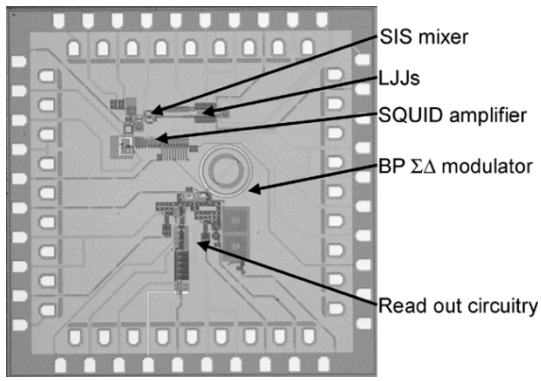

Fig. 2. The photo of front-end chip.

The main purpose for the SQUID amplifier on the front-end chip is to match low input impedance of bandpass modulator ($\mathrm{Z_{in}} \ll 1\ \Omega$) and high output impedance of SIS mixer ($\mathrm{Z_{out}} \approx 50\ \Omega$) with simultaneous filtering of all out of IF band signals. The realized amplifier consists of a front end and a power amplifier. The front-end is a simple two-junction voltage-mode SQUID to transform the input signal current into the stream of SFQ pulses. The pulses are amplified in power by passing over the Josephson transmission line (JTL) with exponentially increasing critical and bias currents of the Josephson junctions. The final stage of JTL and resistive-inductive network provide both the power gain and low-pass filtering in order to suppress the SQUID's Josephson oscillations and to refine the amplified signal.

The output signal is the current through a load inductor, which is inductively coupled to the modulator. The single Josephson junction connected in series with the load acts as the signal limiter.

The resonance frequency of mixer-amplifier tank circuit is measured to be 1.5 GHz. The SQUID amplifier has the following experimentally measured parameters: critical current and normal state resistance per junction of front end SQUID are $\mathrm{I_C} = 40\ \mu\mathrm{A}$ and $\mathrm{R_N} = 4\ \Omega$, SQUID inductance is 40 pH, mutual input inductance is 400 pH and input inductance is 5 nH providing the amplifier noise temperature $\mathrm{T_N} = 90\ \mathrm{K}$.

A first-order bandpass delta-sigma modulator with a center frequency of 1 GHz that used a lumped-element LC resonator is designed and fabricated on the front-end chip. The modulator uses implicit feedback—the switching of the clocked comparator automatically feeds $-\Phi_0$ back to the resonator—which is a fundamental advantage of superconductor delta-sigma modulators. In order to be able to verify performance of stand-alone front-end chip, the modulator is connected to read out digital circuitry, e.g., a high-speed output driver. The data from the modulator's output are converted to nonreturn-to-zero voltage-potential form, amplified and transferred to room temperature for additional amplification and processing.

Fig. 3 shows the measured spectrum of bandpass modulator when -20 dBm (-3 dB full scale) 1020 MHz input signal is sampled with 800 MHz clock. The undersampled spectrum clearly shows tone corresponding to 1020 MHz and expected noise shaping with dip of 15 dB in vicinity of 1 GHz.

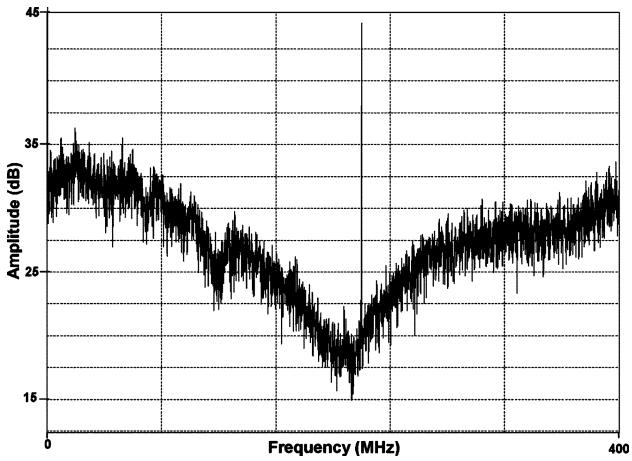

Fig. 3. Spectrum from bandpass delta-sigma modulator (1-bit digitizer) with clock signal at 800 MHz and input signal at 1020 MHz.

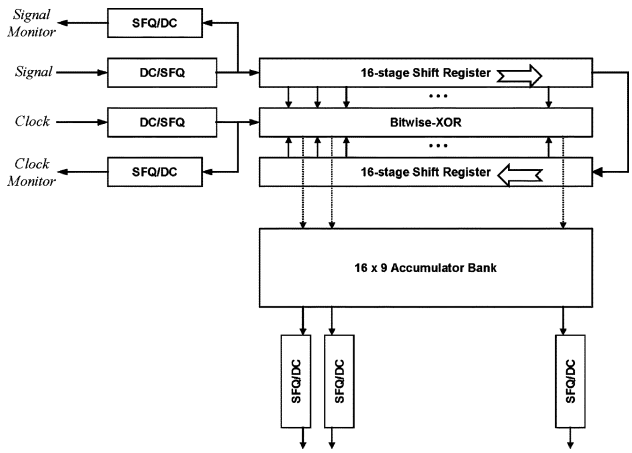

Fig. 4. The block diagram of 16-channel digital autocorrelator.

IV. Digital Signal Processing

We have selected the correlator circuit as the core component of our digital signal processor. One classic way to obtain the frequency spectrum of a time-domain signal $f(t)$ is to take the correlation between $f(t)$ and a time-delayed version of the same function $f(t-\tau)$. The autocorrelation function $R(\tau) = (1/T)\int f(t)f(t-\tau)dt$, will selectively strengthen coherent frequency components that are periodic with time τ; other components will exhibit a random walk. The power spectral density function $S(f)$ (or simply the spectrum of the signal) is then the Fourier transform of $R(\tau)$. If the signal is first digitized, then both the autocorrelation and the Fourier transform can be obtained in the discrete digital domain. The resolutions in the time and frequency domains are similar.

Our approach in design of 128-channel autocorrelator is to compose it from a 16-channel autocorrelator and 112-stage PRSR.

The shift register should have number of switches. By closing these switches data can be directed through or bypassing different digital delay lines, obtaining the data delay in increments of 16.

Fig. 4 shows the block diagram of 16-channel digital autocorrelator. The digital 16-channel autocorrelator forms a linear array with two main parts: digital delay lines with multipliers and an array of binary counters. The binary counters are composed of T flip-flop gates, outputting only the most significant bits. The individual components of the design—the circular shift register, XOR's and T flip-flop gates are well known and have been reported to have very wide operating margins in many studies. Straightforward integration of these gates into an operational subsystem is possible only for the T flip-flop counters, due to their asynchronous mode of operation and unusually wide parameter margins. Integration of the XOR gates into the circular shift register is a much less trivial task, mostly due to numerous timing requirements.

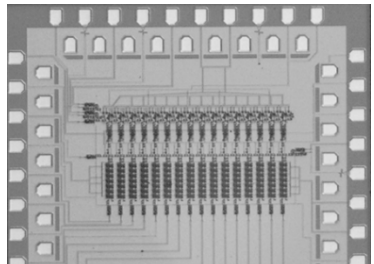

Fig. 5. The photo of 16-channel digital autocorrelator chip.

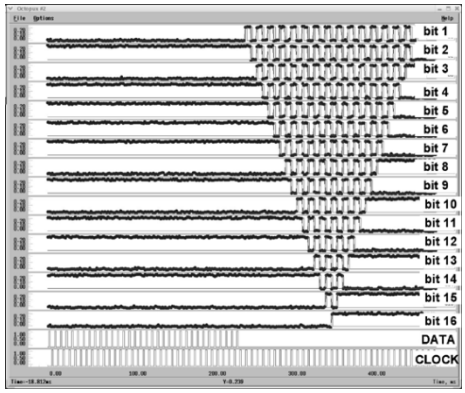

Fig. 6. Low-frequency testing of the 16 channel autocorrelator. For the data and clock inputs each rectangular pulse corresponds to an SFQ pulse.

The main part of the autocorrelator is the digital delay line, which is based on a circular shift register with XOR multipliers built into every stage. The digital test at low speed is performed to verify the correct operation of a 32-stage circular shift register. The total number of D flip-flops in the shift register is 34: 2 D flip-flops per each regular stage plus 2 in the "0-th" stage, where data makes a U-turn.

The 16-channel autocorrelator has been fabricated (the layout is shown in Fig. 5) and successfully tested using OCTOPUX test system [5] capable of performing exhaustive low speed (500 Hz) tests of large digital and analog circuits.

Fig. 6 shows the correct operation of the 16 channel autocorrelator without accumulator bank for the test sequence when a train of $2\times 16+2 = 34$ '1's (signal "DATA" in Fig. 6) is loaded into the circular shift register. High as digital '1' and low as digital '0' are interpreted. The correct operation of all 16 XOR gates (outputs O1-O16) for all possible combinations of inputs ("00",

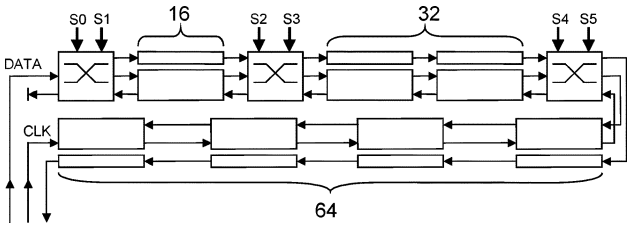

Fig. 7. The block diagram of programmable delay 112-stage shift register.

TABLE I
DC SWITCH SETTINGS FOR 112-bit PRSR

16-bit block		32-bit block		64-bit block		T_{clk}
S0	S1	S2	S3	S4	S5	(delay)
0	1	0	1	0	1	0
1	0	0	1	0	1	16
0	1	1	0	0	1	32
1	0	1	0	0	1	48
0	1	0	1	1	0	64
1	0	0	1	1	0	80
0	1	1	0	1	0	96
1	0	1	0	1	0	112

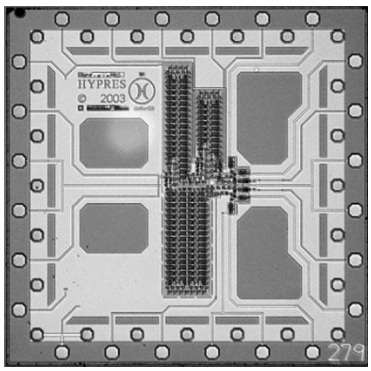

Fig. 8. The photo of 112-bit programmable shift register chip.

"10", "01", "11"), as well as correct operation of the circular shift register under full load is demonstrated.

Fig. 7 shows the block diagram 112-bit PRSR. This shift register includes 112 stages divided into three chunks of 16, 32 and 64 stages together with 6 switches S0-S5. It employs more robust counter-flow design [6], e.g. the stream of data and clock pulses flow in opposite directions. By applying DC current to different combination of the switches we are able to choose any delay from 0 to 112 in increments of 16 (see Table I). The 112-stage PRSR has been fabricated and a photo of the chip is presented in Fig. 8. The operation of the shift register has been successfully verified by using OCTOPUX. As an example, Fig. 9 presents test results for the 112-bit PRSR with correct operation of the shift register with switches S0, S3 and S5 closed while switches S1, S2 and S4 are opened, showing the delay of data at the output for 16 clock cycles (see Table I). Fig. 9 shows the following three groups of data traces: data and clock inputs—inputs that have been generated by OCTOPUX and sent to the chip, data and clock monitors—traces experimentally measured immediately after appropriate entrances to the chip, and clock and data outputs—traces measured after clock and data propagated through all 112 stages of shift register. The data output exhibits the correct 16-clock cycles delay.

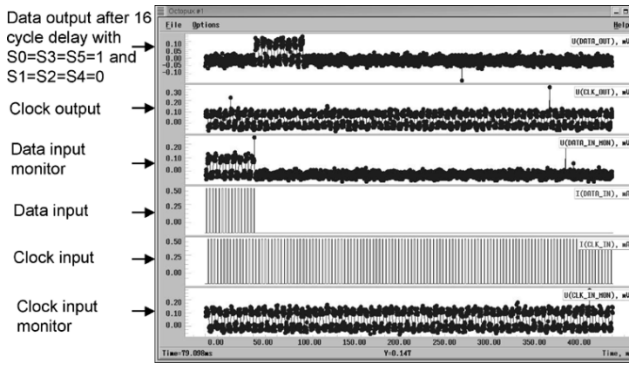

Fig. 9. Test results for the 112-bit PRSR with 16 clock cycles delay.

The correct performance of 16-lag autocorrelator and 112-lag PRSR has been verified. Their high-speed operation has been already realized before: autocorrelator at 11 GHz [3] and more complex shift register at 19 GHz [6]. After integration, our DSP circuit is expected to operate at slightly lower speed, still sufficient for intended applications—to acquire spectra of slow changing signals.

V. CONCLUSIONS

A compact superconducting mm/submm integrated digital spectrometer is being developed. This spectrometer may be used in radio-astronomical research, remote monitoring of the Earth atmosphere and environmental monitoring for hazardous materials of chemical and biological origin. Assembled on a multi-chip module the spectrometer offers integration of thin film analog components such as a mixer, superconducting local oscillator and an IF SQUID amplifier together with superconducting digital circuitry.

Correct performance of all integrated spectrometer analog and digital components, such as local oscillator/SIS mixer structure, IF SQUID amplifier, bandpass delta-sigma modulator, 16-lag autocorrelator and 112-bit programmable delay shift register have been successfully verified. The final assembling of these components on a multi-chip module is underway.

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