Superconducting High-Resolution Low-Pass Analog-to-Digital Converters

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***Abstract*—HYPRES has developed a high-resolution, dynamically programmable analog-to-digital converter (ADC) for radar and communications applications. The ADC uses the phase modulation-demodulation low-pass architecture and on-chip digital filtering. Detailed experimental results at 20 GHz clock frequency of the ADC chip fabricated with a 1 $\mathrm{kA/cm^2}$ Nb process are presented and discussed. In addition to the standard ADC configuration, different ADC modifications are described. In the multirate ADC, the modulator sampling frequency is the twice the clock frequency for the time-interleaved digital filter. In addition to the standard parallel-output ADC, a serial output ADC and its interface to room temperature electronics are developed. This serial ADC chip fabricated with the advanced HYPRES 4.5 $\mathrm{kA/cm^2}$ process operated up to 34 GHz clock. As a major step toward commercialization of superconducting electronics, an ADC chip was successfully packaged on a cryocooler where it showed reduced performance up to 11.52 GHz clock.**

***Index Terms*—Analog-to-digital converter, cryocooler, decimation filter, modulator, RSFQ, SFDR, SINAD, superconductor.**

I. Introduction

THE ANALOG-to-digital converter (ADC) is the critical element for progress in radar and communications, since it defines the architecture and the performance capabilities of an entire systems. High speed, low power, natural quantization, quantum accuracy, high sensitivity, and low noise make the superconductor ADC the prime candidate for direct digital conversion of analog signals right at the antennas for use in the next generation digital RF receivers [1]. Over the last decade, designs and results of evaluation of superconductor oversampling low-pass ADCs based on the phase modulation-demodulation (PMD) architecture [2] were reported. The complete test setup including room-temperature electronics for comprehensive ADC evaluation was assembled [3]. Both the ADC modulator and the decimation digital filter were re-optimized for operation at 20 GHz clock [4]. Initial test results at clock frequencies up to 19.6 GHz were described [5]. This paper presents detailed experimental data proving consistent ADC operation at a 20 GHz clock frequency. We also present results for the modified ADC chip based on the multirate approach allowing doubling the modulator sampling frequency, while the digital filter clock frequency stays the same. For the first time, such a complex circuit as our low-pass ADC has been successfully packaged on a commercial-off-the-shelf (COTS) cryocooler. In order to reduce number of output lines and therefore decrease cryocooler heat load, a serial interface between ADC and room temperature was developed. A serial ADC fabricated using the advanced 4.5 $\mathrm{kA/cm^2}$ HYPRES process operated up to 34 GHz clock.

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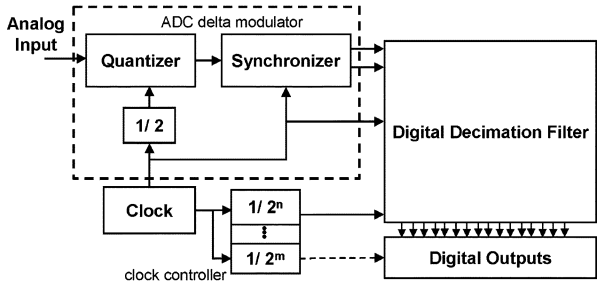

Fig. 1. Block diagram of the PMD ADC. Serialization of outputs may be used to reduce the number of lines.

II. Experimental Results

Fig. 1 shows the simplified block diagram for this PMD ADC [2]. In the delta ADC modulator, magnetic flux is continuously pumped into a quantizer at a constant rate of $\Phi_0/2$ per clock period, where it is modulated by a flux induced by the derivative (delta) of input RF signal. Then the flux leaves the quantizer in the form of the phase (or delay) modulated SFQ pulses via the only Josephson junction. This SFQ pulse train is passed to a two-channel synchronizer, which performs the phase demodulation and effectively increases the number of quantization levels to three. The subsequent Hogenauer-type digital decimation filter (DF) with a sinc (sinx/x) function frequency response integrates and averages the digitized signal, reducing the output bandwidth and increasing the signal-to-noise ratio. The filter operates at the same high clock rate as the ADC modulator. The filter output multi-bit data are read out at decimated clock rate, i.e. 2^{n} slower than input clock and amplified by output drivers to 1–2 mV level acceptable by room temperature electronics. Then these data are transferred to room temperature at a rate 2^{m} slower than the clock. In all our previous ADC work [3], a standard parallel interface was employed, i.e. data were transferred to room temperature with the filter output clock speed and $\mathrm{m} = \mathrm{n}$. In order to reduce the number of output lines between the ADC and room temperature, a serial interface with $2^{\mathrm{n}-\mathrm{m}} : 1$ (e.g., 8:1) serialization ratio was developed.

A. Parallel Output ADC

Here we report on the results of the evaluation of a 15-bit, low-pass ADC with 2-channel synchronizer, a 1:256 decimation ratio, parallel output, and operating at a 20 GHz clock. To increase the ADC chip robustness, the first integrator in the digital filter

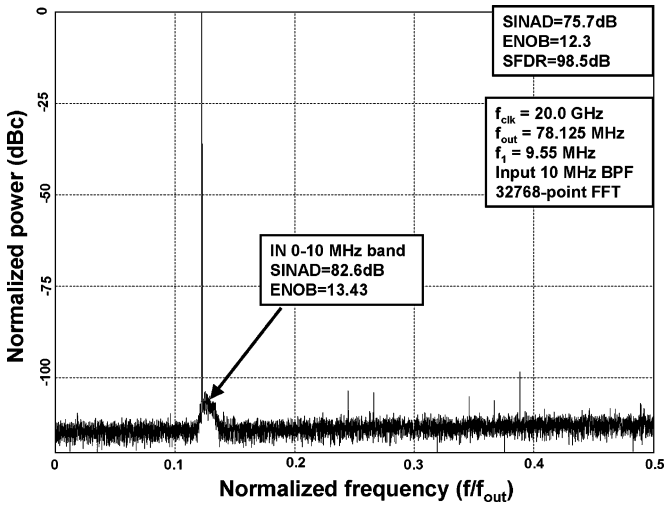

Fig. 2. FFT for a single 9.55 MHz, -7 dBm input sinewave measured at 20 GHz clock and acquired at 78.125 MS/s.

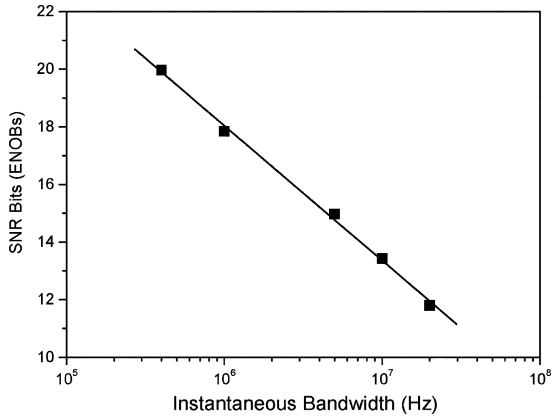

Fig. 3. ENOB vs. instantaneous bandwidth.

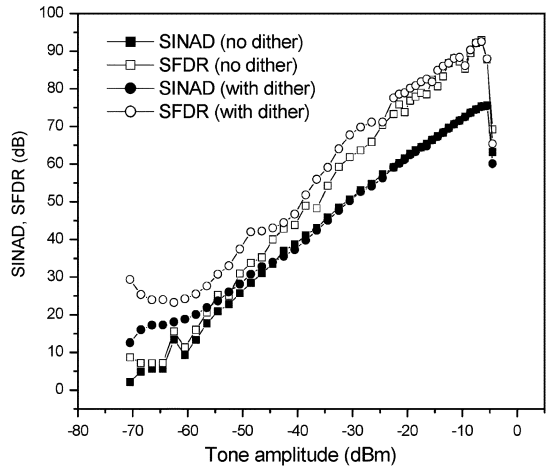

Fig. 4. SINAD and SFDR measured with a 10 MHz input sinewave for the ADC running at 20 GHz clock. Both with and without dither data were acquired at 78.125 MS/s.

which operates at a full clock speed was redesigned. In the previous versions, all toggle flip-flops with nondestructive readout included a half adder (HA). Now, this HA was removed from all but the first two slices. This modified ADC chip with about 5,000 Josephson junctions was fabricated using the standard HYPRES $1\,\mathrm{kA/cm^2}$ process [6] and tested in liquid helium. The complete test setup used for experimental evaluation is described elsewhere [3]. Fig. 2 shows a single 9.55 MHz tone 32768-point FFT taken at 20 GHz clock acquired at 78.125 MS/s. To reduce effects of harmonic distortion of an available test signal generator, a 10 MHz bandpass filter with $\sim$1 MHz bandwidth was used. This is evident in a characteristic noise cusp in vicinity of the tone (Fig. 2). The measurement was taken close to the slew rate limit of the ADC. In the Nyquist band, it shows 98.45 dB spurious-free dynamic range (SFDR) and 75.7 dB signal-to-noise-and-distortion ratio (SINAD) translating into 12.3 effective number of bits $(\mathrm{ENOB} = (\mathrm{SNR} - 1.76)/6.02)$. Since delta PMD ADC is slew-rate limited ADC, its performance degrades as the maximum input signal slew rate ($\Phi_0/2$ per clock period) is reached.

To take full advantage of oversampling in our ADC, additional post-process filtering in software was employed to effectively reduce the output sampling rate and remove higher frequency components. This averaging in the 0–9.7 MHz band gives SINAD of 82.6 dB or 13.43 ENOB.

The single tone measurements with 400 kHz, 1 MHz, 5 MHz and 20 MHz tones were performed with a variety of appropriate band pass or low pass filters depending on their availability. Similar post-processing averaging in the band from 0 to the tone frequency was performed. Fig. 3 shows the collection of these data, which closely follows ENOB versus bandwidth trade off curve at a rate of 1.5 bit (9 dB)/octave characteristic for ideal delta modulators [7]. Fig. 4 shows the SINAD and SFDR for a 10 MHz sinewave signal and 20 GHz clock. As expected [7], we observed a significant increase in spur content and SINAD drop after exceeding the slew rate limit. Two sets of data, both with and without dither are presented in Fig. 4. In order to improve ADC linearity, the dither signal was applied to the ADC input at the decimated clock frequency of 78.125 MHz. Indeed, data recorded with the dither source shows the SFDR improvement of up to 10 dB, especially for small signal amplitudes. In order not to introduce extra noise and excessively reduce SINAD, the dither with minimal possible power was applied.

This was controlled by observing smoothed out quantization steps on signal reconstruction for a low amplitude ($\sim$ -35 dBm), low frequency ($\sim$1 kHz) signal. To make quantization steps even more pronounced, a triangular input signal was applied. The dither was found especially useful in detection of single tone small amplitude signals, especially in the presence of big interferor tones, which is of an importance for many communication applications. As an example, Fig. 5 shows the FFT of the least detectable signal with dither present. The spectrum is taken for a single 9.8 MHz tone with amplitude -90 dB with respect to the ADC full scale. Moreover the input amplitude can be further reduced by at least an extra 10 dB, since the tone at -15 dB (see Fig. 5) is not a signal harmonic but rather some interference artifact of the test setup. The two-tone tests were done around a 10 MHz input signal frequency. Input signal powers were also varied in order to study the ADC performance both near and far from the slew rate limit. Fig. 6 shows a set of FFT results for $\mathrm{f_1} = 9.45\,\mathrm{MHz}$ and $\mathrm{f_2} = 10.45\,\mathrm{MHz}$ of the same input powers and equally spaced from the center of the bandpass filter. Our experimental results confirmed our expectation of low intermodulation products. The closest to the tones, 3rd order intermods $(2\mathrm{f_1} - \mathrm{f_2}, 2\mathrm{f_2} - \mathrm{f_1})$ did not show up prominently. Surprisingly, the highest was an intermodulation product of $5\mathrm{f_2} - 4\mathrm{f_1}$.

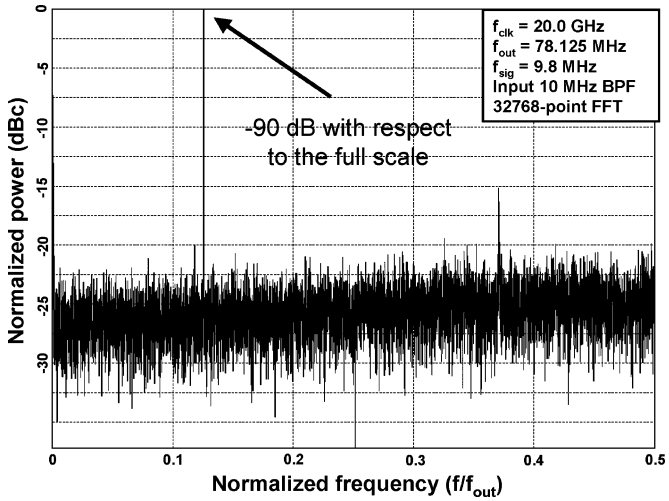

Fig. 5. FFT of 9.8 MHz tone with signal amplitude of -90 dB with respect to a full scale.

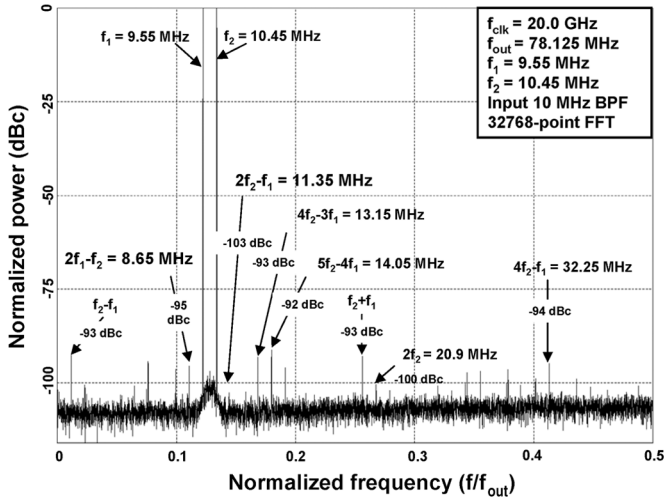

Fig. 6. FFT result for a two tone (9.55 and 10.45 MHz) recorded at 20 GHz clock and acquired at 78.125 MS/s. All intermodulation products are marked.

B. Serial ADC

An ADC with a new serial (8:1) interface between cryogenic and room temperature electronics has been developed. This interface employs two 8-bit parallel-to-serial converters [8] based on the B flip-flop cell [9] and two output drivers. The 8-fold increase of the output data rate due to serialization makes the on-chip output drivers and room-temperature amplifiers critically important. These drivers and interface amplifiers were modified enabling output rate to go over 1 GS/s. The read-out clock at speed 8 times faster than the digital filter output decimated clock was generated by taping appropriate place in clock controller circuit (Fig. 1). Two data streams together with decimated and read-out clocks were sent out to room temperature electronics to be amplified and deserialized before performing signal reconstruction.

This serial ADC chip was fabricated with a 4.5 $\mathrm{kA/cm^2}$ HYPRES process [6]. The design of all ADC components was essentially the same as for 1 $\mathrm{kA/cm^2}$ process with junction area proportionally decreased to keep critical current values while shunt resistors were adjusted to maintain junction Stewart-McCumber parameter β_c unchanged. We observed stable, error-free operation allowing performing long-FFT transforms up to

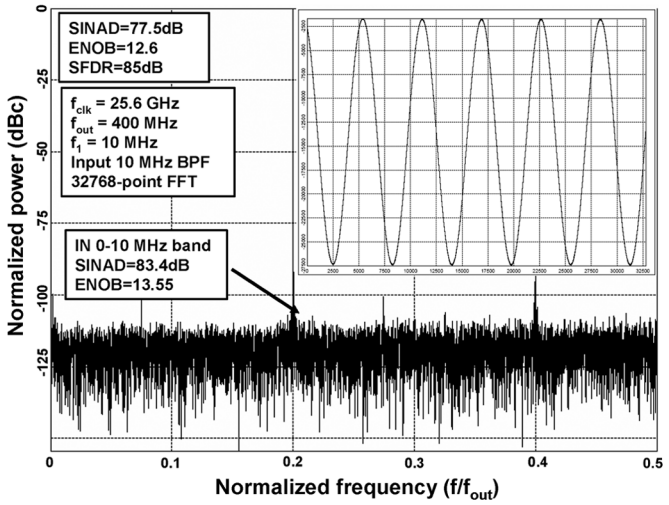

Fig. 7. FFT result for 4.5 $\mathrm{kA/cm^2}$ LP ADC for single 10 MHz tone (obscured by grid line) measured at 25.6 GHz clock and acquired at 400 MS/s through serial outputs. The inset shows the reconstructed waveform for 10 kHz input at 34 GHz clock.

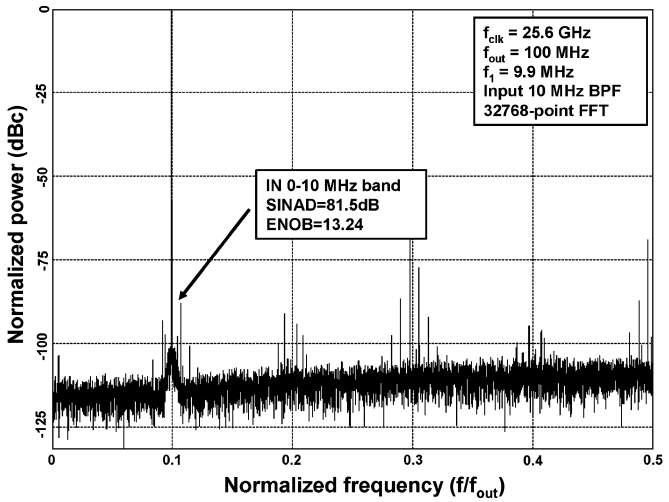

Fig. 8. FFT result for multirate ADC with 2-channel time interleaved DF for single 9.9 MHz tone at 25.6 GHz clock acquired at 100 MS/s.

TABLE I
ENOB PERFORMANCE FOR DIFFERENT LP ADCS

LP ADC type	Highest clock frequency (GHz)	ENOB for 10 MHz tone (in 0 - f_{sig} band)
Parallel (1 kA/cm^2)	20	13.43
Serial (4.5 kA/cm^2)	34	13.55 (at 25.6 GHz clock)
Parallel multirate (1 kA/cm^2)	25.6	13.24
Cryocooler mounted parallel (1 kA/cm^2)	11.52	11.96

25.6 GHz clock (Fig. 7). Somewhat less stable but still correct operation was observed up to 34 GHz clock (see inset to Fig. 7).

C. Multirate ADC

In a multirate ADC, different clock rates are used for sampling of the ADC modulator $(\mathrm{f_{MOD}})$ and clocking the digital filter $(\mathrm{f_{MOD}}/2)$. To provide a rate transition between different clocks, the ADC synchronizer output is demultiplexed into two data streams with the speed of each being half of the sampling frequency $\mathrm{f_{MOD}}$. An increase of the ADC clock frequency by factor

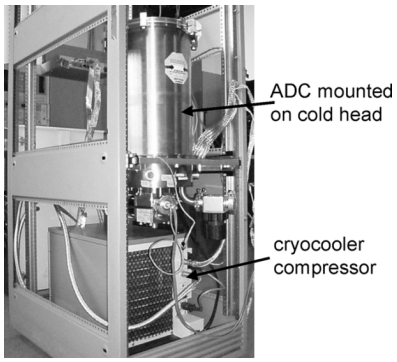

Fig. 9. An experimental setup with ADC packaged on Sumitomo cryocooler.

of 2, and therefore improved performance, may be achieved by implementing the 2-channel time-interleaving technique [10].

In the implemented multirate ADC chip, only one output of the synchronizer was used. This normally should cause the decrease in SINAD. However, this performance loss was outweighed by the increase of the modulator sampling frequency f_{MOD} in accordance to formula $ENOB \sim \log_2(k \cdot f_{MOD}^{3/2})$, where k is a number of channels in the synchronizer. The multirate ADC with a 2-channel interleaved digital filter was designed and fabricated with the HYPRES 1 kA/cm^2 process. The FFT result of a single 9.9 MHz tone measured at 25.6 GHz clock for this chip is presented in Fig. 8. The higher harmonic content seen in this spectrum was traced to the ADC input transformer. Its coil was twice narrower than for other ADC chips described here. This likely caused the nonlinear response to the input signal close to full scale when the coil critical current limit was approached (Table I).

III. Test in Cryocooler

As a major step toward commercialization of superconducting electronics, our low pass ADC chip with parallel output fabricated with 1 kA/cm^2 process was successfully cryopackaged on a COTS cryocooler [11], [12]. The Sumitomo SRDK-101D-A11 two-stage cryocooler was selected due to its relative compactness, adequate heat lift and air-cooled compressor. The cryocooler option with helium damper was chosen to reduce temperature oscillation and, therefore, improve circuit operational bias margins. Fig. 9 shows the cryocooler coldhead and compressor fitting in a standard 19″ rack. The cryopackaged ADC chip demonstrated stable and correct operation up to 11.52 GHz (Fig. 10). Its SINAD and SFDR were identical to that measured in liquid helium. However data acquisition at higher clock frequencies became corrupted by higher error rate caused by the crosstalk between output lines proportional to output data rate.

IV. Conclusion

A family of superconducting low pass ADCs were developed and investigated. Detailed results proving consistent operation of the 1 kA/cm^2 ADCs with parallel output at 20 GHz clock were presented. We also realized a multirate ADC allowing doubling of the modulator sampling frequency and a serial ADC to reduce the number of output lines. The serial ADC fabricated with an advanced 4.5 kA/cm^2 process operated up to 34 GHz clock. For the first time such a complex superconducting digital circuit

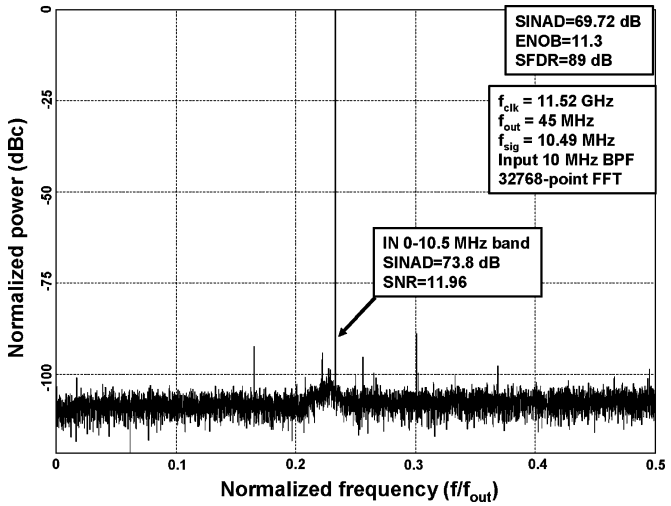

Fig. 10. Operation of the cryopackaged ADC chip mounted on Sumitomo cryocooler at 4 K. The FFT is for a 10.49 MHz input sinewave measured at 11.52 GHz clock and acquired at 45 MS/s.

as a 5,000 junction ADC was successfully tested on a COTS cryocooler. Table I summarizes our experimental results.

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