Progress in the Development of Cryocooled Digital Channelizing RF Receivers

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***Abstract*—HYPRES is developing a class of digital receivers featuring direct digitization at radio frequency. The complete system, consisting of a cryopackaged Nb superconductor All-Digital Receiver (ADR) chip followed by room-temperature interface electronics and a field-programmable gate array (FPGA) based post-processing module, has been developed. Depending on the targeted application the ADR chip comprised either a low-pass delta with phase modulation-demodulation architecture or X-band band-pass sigma-delta modulators together with digital in-phase and quadrature mixer and a pair of digital decimation filters. The chips were fabricated using a 4.5-$\mathrm{kA/cm^2}$ HYPRES process and were cryopackaged using a commercial-off-the-shelf cryocooler. Recently, with significant improvements in chip cryopackage, room-temperature electronics and FPGA programming we were able to achieve stable operation of a low-pass ADR at 28.16 GHz and X-band ADR at 30.72 GHz clock frequencies. Experimental results are presented and discussed.**

***Index Terms*—ADC, cryocooler, digital receiver, direct digitization, RSFQ.**

I. Introduction

THE AREA OF radio frequency (RF) communications, both commercial and military, represents one of the most promising applications for superconductor electronics. The future systems demand better utilization of the frequency spectrum, greater bandwidth and sensitivity, as well as moving towards higher input signal frequencies.

Performance of conventional analog RF systems is bound by frequency dependency, non-linearities, high insertion losses, and an extensive network of waveguide interconnects that ultimately limit the performance of the complete receiver system. These limitations are greatly multiplied when multiple frequencies and channel configurations are required.

These problems can be solved with the help of the software-defined radio concept [1], the digital-RF architecture and employing superconductor technologies by extension of digital processing to the traditionally analog RF domain. Superconductor Rapid Single Flux Quantum (RSFQ) electronics with ultrafast digital logic and high-linearity analog-to-digital converters (ADCs), allow direct digitization of RF signals and digital processing of the digitized RF signals. Such a direct-conversion system approach has been realized with Digital-RF architecture. This architecture enables digital signal distribution systems and can provide multiple band, frequency and channel operation within a single integrated system [2]. In addition, digital signal processing at RF eliminates all analog intermediate frequency (IF) and most analog RF processing and distribution.

Recently, we have developed the first generation of RSFQ digital-RF receivers, integrating RF signal digitizers and digital signal processing (DSP) modules into a single chip [3]. The digitizers are based on oversampling delta or delta-sigma modulators performing conversion of analog RF signals to digital. These are followed by digital channelizers that perform digital down-conversion and filtering, or more general correlation-based signal processors [4], [5]. We have assembled and successfully tested complete cryocooled All-Digital Receiver (ADR) system prototypes by integrating the digital receiver superconductor chips with commercial 4 K cryocoolers and room-temperature interface electronics. We demonstrated a cryocooled ADR system based on a low-pass (LP) ADC and operated at 24.32 GHz clock frequency [6]. This system performed direct digitization of RF signals over a wide frequency range in HF, VHF, UHF and L bands. Another cryocooled ADR system based on a delta-sigma band-pass ADC modulator directly digitizes the X-band RF signal using a 10.24 GHz clock in RF undersampling mode [7]. With the help of this ADR system we performed a successful live data and video reception with an XTAR satellite while the system was connected to a 3rd-party modem [7].

In what follows, we will describe the latest results in the development and demonstration of digital-RF receiver systems.

II. Superconductor Digital RF Receivers

We have evaluated several single-channel digital-RF receiver chips integrating an ADC modulator (low-pass or band-pass) with a single-channel digital channelizer. We use a delta modulator with a phase-modulation-demodulation (PMD) architecture [8] for the implementation of a low-pass ADC. Since the PMD ADC really measures the signal derivative, its maximum input is determined by a slew rate limit corresponding to a flux rate of $\Phi_0/2$ ($\Phi_0 = 2.07\,\mathrm{fWb}$) per clock period, of either sign. The signal to noise ratio (SNR) for this first-order oversampling ADC changes at a rate of 9 dB/octave. Therefore, by changing the decimation ratio, usually by factors of 2, one can trade-off bits of resolution (ENOB) for bandwidth at a rate of 1.5 bits/octave. The LP ADC performance was extensively evaluated for various input single-tone and two-tone sine waves [9].

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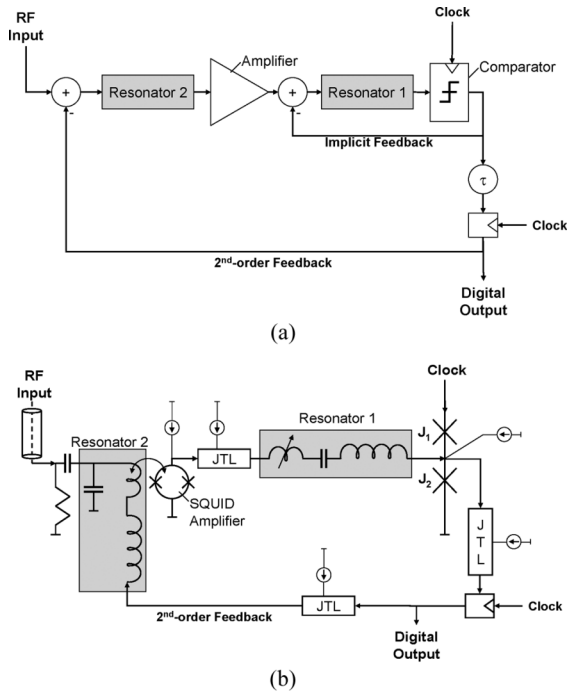

Fig. 1. Second-order band-pass delta-sigma ADC modulator. (a) Block diagram. (b) Schematics.

For direct band-pass sampling, the delta-sigma modulator is the best architecture, since it shapes the noise around a center frequency resulting in the maximum SNR. A band-pass delta-sigma ADC was chosen to minimize the quantization noise in the X-band (7.25–7.75 GHz). We developed this ADC modulator based on a continuous-time scheme [10] with two lumped LC resonators (Fig. 1(a)). One of the unique features of the superconductor delta-sigma ADC modulators is implicit feedback, i.e. when the bottom junction (J2) of the two-junction clocked comparator switches (Fig. 1(b)), it subtracts a single flux quantum Φ_0 from the input while producing a digital output SFQ pulse. Therefore, no explicit feedback loop is needed to construct a first-order ADC modulator. A second-order modulator improves SNR by further suppression of quantization noise. In this implementation of the band-pass ADC, the first and the second resonators were designed to be 7.4 GHz and 7.6 GHz respectively [7]. To achieve the second-order noise shaping, we introduced an explicit feedback loop using Josephson transmission lines (JTLs) as active delay elements in addition to a D flip-flop to control the phase of the feedback signal.

We have developed and demonstrated several single-channel digital-RF receiver chips [3] integrating an ADC modulator (low-pass or band-pass) with a digital in-phase (I) and quadrature (Q) digital mixer and two digital decimation filters (Fig. 2). The ultrafast oversampled digital data stream from the ADC modulators at the sampling clock rate of up to ~40 GHz using the 4.5 $\mathrm{kA/cm^2}$ HYPRES fabrication process [11] is down-converted by multiplying (mixing) with a digital local oscillator (LO). The subsequent Hogenauer-type digital decimation filter (DDF) with a sinc (sinx/x) function frequency response integrates and averages the digitized signal, reducing

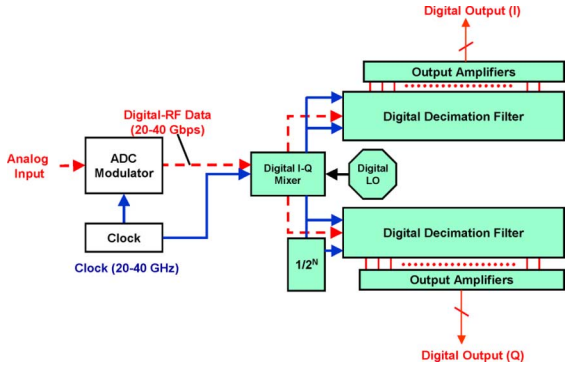

Fig. 2. Block diagram of a digital receiver chip comprising an ADC modulator, digital in-phase (I) and quadrature (Q) digital mixer and two digital decimation filters.

the output bandwidth and increasing the signal-to-noise ratio. The receiver produces two multi-bit digital words (I and Q) at the decimated clock rate $\mathrm{f_d} = \mathrm{f_{clk}}/2^{\mathrm{N}}$, where 2^N is decimation ratio.

We use a single-bit periodic waveform (square wave) as the local oscillator. In order to ensure exactly 90° relative phase difference, the in-phase (I) and quadrature (Q) local-oscillator $(\mathrm{f_{LO}})$ signals were derived by dividing a signal of frequency $4\mathrm{f_{LO}}$ with a binary tree of toggle (T) flip-flops [3]. Unfortunately, this design scheme brought in an intermittent phase loss, especially for high LO frequency for the X-band ADR, resulting in sporadic switching between I and Q channels. To solve this issue a new approach has been implemented. Its design details will be described elsewhere.

We designed [3] ADR chips and manufactured them using HYPRES fabrication process with 4.5 $\mathrm{kA/cm^2}$ critical current density [11]. Fig. 3 shows microphotographs of X-band (a) and LP (b) ADR chips comprising over 10000 Josephson junctions. The essential chip components such as modulator, common clock controller (CCC), digital down-converter (DDC) or mixer, DDFs and output drivers are marked on Fig. 3. A Typical ADR chip takes about 1.1 A of bias current delivered via multiple bias lines. To prevent negative effects of ground current distribution, large current leads are encased between two superconductor ground plane layers connected by multiple vias. The chip ground hole-and-moat patterns were optimized to maximize flux-trapping resistance and to preserve a symmetrical nature of the chip ground plane design. This allowed us to achieve complete independence from bias current distribution to such a degree that it was possible to completely operate either I or Q channel while the other one was completely unbiased.

III. System Integration

In order to make a superconductor digital RF receiver practical, it has to be integrated into the room temperature environment. Nb-based electronics must operate at a nominal 4 K, but cannot be realistically deployed in the field in an open boil-off LHe cryostat since small-scale low temperature superconducting systems justify neither the overhead of a large cryostat nor the logistics of cryogen supply. Therefore a critical part of the complete system is the cryocooled cryostat.

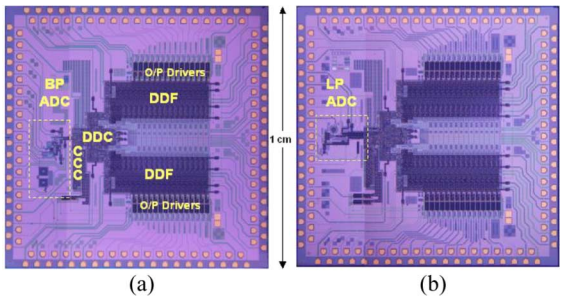

Fig. 3. Microphotographs of a single-channel superconductor digital-RF receiver chips: X-band ADR (a) and LP ADR (b).

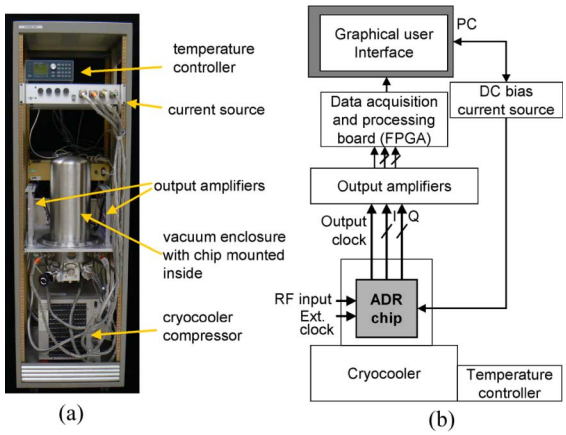

Fig. 4. Digital receiver system based on Sumitomo 4 K cryocooler with all components (PC is not shown) packaged in 19-inch rack (a). Block-diagram of ADR system (b).

Fig. 4(a) shows a 19-inch rack housing the ADR chip cryopackaged on a commercially available 2-stage cryocooler, an air-cooled He compressor for the selected Gifford-McMahon cryocooler, temperature controller, a computer controlled multichannel current source to bias the ADR chip, room-temperature interface amplifiers, and a FPGA-based post processing module. The complete block diagram of the system is in Fig. 4(b). Not shown in Fig. 4(a) are the PC that runs a custom-developed graphical user interface (GUI) to control the ADR chip current biasing and data acquisition as well as analysis, and a turbopump for initial pump-down of the cryostat vacuum space when system is warm. This pump-down is not needed during system operation since the sub-10 K surfaces self-pump adequately.

The system is built around a Sumitomo Heavy Industries (SHI) SRDK-101DP-11C two-stage cryocooler, which consumes a total of 1.3 kW wall power, giving a specified net refrigeration of 100 mW at 4.2 K and 5 W at 60 K. The cryocooler was selected due to its relative compactness, adequate heat lift and air-cooled compressor. It is equipped with a helium damper to reduce temperature oscillations that might be detrimental for system performance. An air-cooled He compressor for the selected Gifford-McMahon cryocooler is located at the bottom of the rack (Fig. 4(a)).

The ADR chip module including double mu-metal magnetic shielding attached to the second (4 K) stage of the cryocooler is shown in Fig. 5. The design of the chip module is based on the pressure-contact 80-line liquid He chip cryoprobe [12]. This

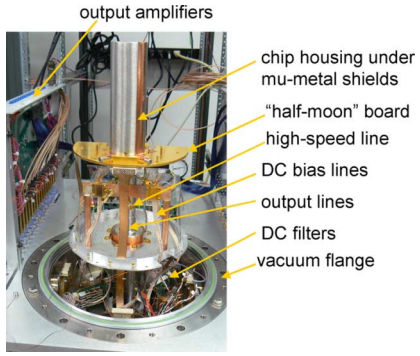

Fig. 5. View of open cryostat with ADR cryopackage mounted on cryocooler coldhead. Output amplifiers for I channel are visible on the left.

allowed a chip to be easily switched between cryocooler and liquid He probe during testing. We implemented here a modular approach for this ADR cryopackage, i.e. the whole module above the gold-plated "half-moon" board (see Fig. 5) can be easily disconnected and exchanged for a module designed for a different chip.

All the wiring between room temperature and the 4 K module is anchored on the 1st stage. The cryopackage requires three distinguished groups for input/output connection: input lines to supply DC bias currents (1 mA to 100 mA per bias line), intermediate speed output cables (up to 120 MHz) and coaxial lines for high-speed signals (input RF, external clock, etc.). Our earlier cryopackage [6], [7] contained twisted pairs for DC lines. For that cryopackage for output lines we used twisted pairs together with microstrip lines integrated into a 40 K radiation shield with multiple interconnects inside the vacuum space. In this work, in order to improve signal integrity and reliability of the entire system for the current cryopackage, we use three cable types: ribbons of beryllium-copper twisted pairs for dc bias currents, custom made flex cable for output digital signals, and UT-47 stainless steel coaxial lines for high-speed signals. All DC lines were heavily filtered by banks of LCL low-pass filters with a cut-off frequency of 300 kHz placed inside the cryostat at room temperature (see Fig. 5). New custom-made RF lines for intermediate speed data outputs were designed and implemented. Three layer flex boards formed these output lines with Kapton as a dielectric and BeCu as a conductor. This choice of metals represents a tradeoff between electric loss and low heat conductivity. In addition, the thermal and mechanical properties of new flex-lines allowed us to run them directly from the 4 K module all the way to the room temperature feedthrough (see Fig. 5), thus eliminating most of the internal connectors. These improvements also allow us to replace a sophisticated multi-layered radiation shield with traditional polished one, which reduced the heat load and consequently the base temperature for both 40 K and 4 K stages.

Earlier calibration of the temperature of each stage as a function of heat applied allowed estimation of thermal loads to both stages: they were 5 W to the first stage at 45 K (mostly thermal radiation) and 150 mW onto the second stage at 3.85 K. The second stage loading was almost entirely from the wiring. Joule heating from the bias leads caused a 0.1 K rise corresponding

to an additional 20 mW, whereas on-chip heating, from resistors used to distribute the bias currents, contributed only about 2 mW.

One of the most important aspects of cryopackaging for superconductor electronics is magnetic shielding. We achieved a low magnetic field by three nested mu-metal shields, two at 4 K and one at room temperature. Additionally, the latter one also acts as the outside vacuum can shown in Fig. 4(a) mounted on vacuum flange (see Fig. 5). The resulting field has been measured at about 10^{-7} T, and was similar to fields used for routine testing in liquid He dewars.

Cryopackage upgrades described above cause the following significant improvements: lower cross-talk in output data lines, a much lower level of outgassing inside the vacuum space resulting in a lower temperature at both stages of the cryocooler, and, finally, the whole cryopackage became more user-friendly with greater reliability of the entire system operations.

For proper operation at the current stage of development, the superconducting ADR chip requires many independent dc currents, typically in the range from 1 mA to 100 mA per bias line. For this purpose, custom current-control hardware and software modules were designed and fabricated. The current-source hardware module is shown in Fig. 4(a), and is a box mounted in a standard 19-inch rack. This box uses less than 300 W of standard AC power and consists of 48 independently controlled sources, which are connected to the cryocooler in 4 bundles of 12 lines each, shown on the right side of the system rack in Fig. 4(a). These current sources are controlled by a computer using a standard USB-bus line and are under complete digital software control, but are additionally equipped with 4 multi-turn control knobs in the left portion of the front panel for those who prefer a more traditional rotary knob for adjusting currents. Each knob can be assigned to any of the 48 bias lines under software command from the graphical user interface (GUI). The current source box is equipped with a hardware "mute" function. This mode is used whenever the system is turned ON or OFF to prevent fast transients from being coupled to the superconducting chip. The mute switch was also hardwired to the temperature controller and all current sources were muted as soon as temperature of the second stage exceeded 5 K. This feature turned out to be a very practical way to prevent the superconducting chip from being overheated and subsequently damaged in a real test environment.

The digital output signals are generated and pre-amplified by the superconducting ADR chip up to about 1–2 mV. This is not sufficient to be accepted by the FPGA-based post-processing module. We developed a custom amplifier bank consisting of two sets (for each of the I and Q channels) of 16 broadband amplifiers, mounted on the sides of the system 19-inch rack as shown in Fig. 4(a). Each amplifier module consists of a linear stage with an amplitude gain of about 1000 to positive ECL level, followed by a pulse shaping stage that produces standard-level digital signals suitable for a commercial FPGA data processing board. For the ADR systems described in this paper not all of the 32 channels are being used: only 27 for LP ADR and 23 for X-band ADR, i.e. 13 for LP ADR (11 for X-band ADR) for each of the I and Q output signals and one output is used for the decimated clock. Improving the previously developed ADR receiver [6], we placed these two banks of amplifiers directly on a slide-in tray upon which the cryostat is mounted. One bank of amplifiers for the I channel is visible on the left of Fig. 5. This allows us to place these amplifiers as close as possible to the superconducting chip and to avoid the use of 3-foot-long SMA cables used to connect outputs from the chip to the amplifiers [6]. As the result, the signal fidelity from outputs was significantly improved.

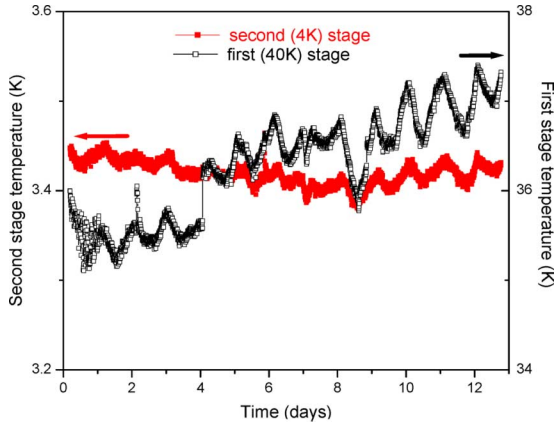

Fig. 6. The temperature dependence for cryocooler two stages with mounted LP ADR chip.

After amplification and pulse shaping output signals are sent to a FPGA board housed on the same slide-in tray behind the cryostat (therefore, not visible in Fig. 4(a)). A custom-made GUI to acquire and analyze experimental data coming from the superconducting receivers via the FPGA was developed. A computer using a standard USB-bus line controls this FPGA.

Advances in cryopackaging and room-temperature electronics allowed the X-band ADR system to perform up to a clock frequency of 30.72 GHz. The low-pass ADR system was operational with high reproducibility at clock frequencies up to 24.32 GHz with identical bias settings at temperatures from 3.4 K to 4.1 K measured at close proximity to the chip and with somewhat smaller margins of temperature up to 28.16 GHz clock.

IV. Performance of Digital RF-Receivers

The ADR chip design with special attention to magnetic shielding and uniformity of the bias current distribution together with an advanced cryopackage and custom-developed room temperature electronics made reliable and reproducible operation of both LP and X-band systems possible. A Lower level of outgassing inside the vacuum space allowed the system to perform continually without temperature degradation for a long period of time. Fig. 6 presents the temperature dependence over time of both stages under test with a mounted LP ADR chip. This dependence has been monitored over a period of 13 days and shows the first stage temperature rising from 35 K to 37 K whilst the second stage temperature stayed relatively stable at around 3.45 K. Temperature oscillations (Fig. 6), especially visible for first stage, are attributed to diurnal fluctuations

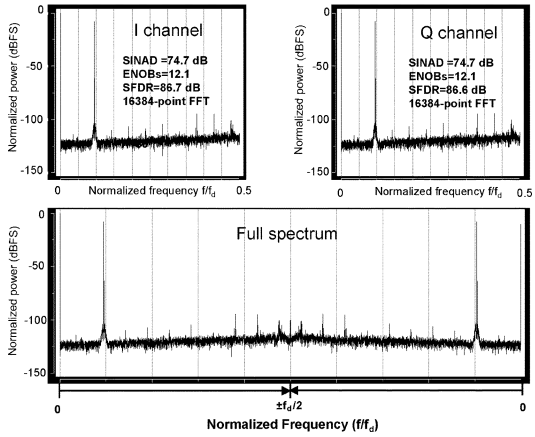

Fig. 7. The LP ADR system test. Measured spectrum of the digital I and Q data and complex FFT (I+jQ) for a single 9.9 MHz tone input sampled at 28.16 GHz clock, digitally filtered, and acquired by FPGA at 110 MS/s.

in ambient temperature and consequently the air-cooled He compressor but did not affect chip performance.

Turning both ADR systems on from a quiescent state $(\mathrm{T} < 4.1\ \mathrm{K})$ involved simply loading a file with preset bias values (using our GUI) and applying an external clock sine-wave at 28.16 GHz for low-pass or 30.72 GHz for X-band systems.

The first system we tested is based on the ADR chip with the low-pass ADC modulator shown in Fig. 3(a). It can digitize RF signals from very low frequencies all the way up to the cutoff frequency of about 1 GHz for the LP ADC input transformer. In practice, we tested this system from HF to L-band [6]. The system operated with high reproducibility at clock frequencies up to 28.16 GHz with identical bias settings at temperatures from 3.4 K to 4.1 K measured at close proximity to the chip. We performed a complete evaluation of the system both in ADC and ADR modes, i.e. with and without applying a local oscillator (LO) input. Fig. 7 shows the fast Fourier transform (FFT) for each I and Q channels and complex (I+jQ) FFT (16384 points) from the acquired I and Q data with a single 9.9 MHz input tone applied with a 10 MHz bandpass filter with ~1 MHz bandwidth. The full spectrum represents a bandwidth of $f_{\mathrm{d}} = \mathrm{f_{clk}}/256 = 110\ \mathrm{MHz}$. The measured SINAD of 74.7 dB over a bandwidth of 55 MHz compares well with 75.7 dB over a bandwidth of 39 MHz produced by our LP ADC [9] with 2-channel synchronizer.

In order to improve ADC linearity, a dither sine-wave signal was applied to the input at the decimated clock frequency of 110 MHz. Since the dither signal does degrade the SNR somewhat, its power was kept to a minimum. Indeed, data recorded with the dither applied show the improvement in spurious-free dynamic range (SFDR) of up to 10 dB, especially for small signal amplitudes [9]. As an example Fig. 8, shows the FFT of the least detectable signal with dither present. The spectrum is taken for a single 10.3 MHz tone with amplitude of −130 dBm. Moreover the input amplitude may be further reduced by at least an extra 5 dB, since the highest tone in Fig. 8 is not a signal harmonic but rather some interference artifact present in the test setup.

We tested the ADR with a variety of RF signals while the LO frequency was chosen to obtain a 10 MHz intermediate frequency (IF) response. Fig. 9 shows the FFT for I and Q channels and also the complex (I+jQ) FFT (16384 points) with a

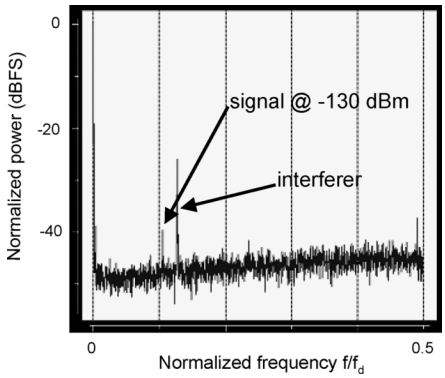

Fig. 8. The LP ADR system test. FFT of 10.3 MHz tone with signal amplitude of −130 dBm.

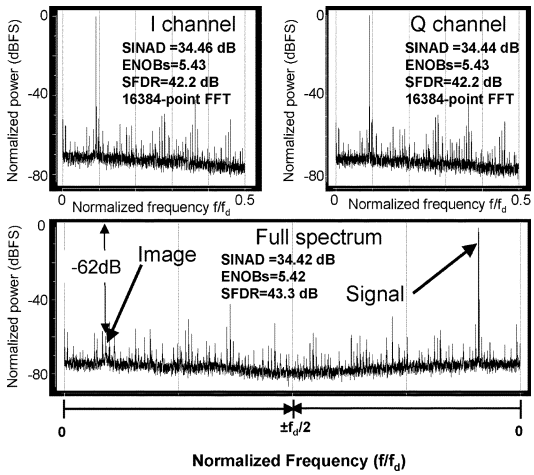

Fig. 9. The LP ADR system test. The 16384-point spectra of the I- and Q-channel outputs with the full spectrum (I+jQ) measured at 28.16 GHz clock and acquired at 110 Ms/s. The input tone frequency is 190 MHz and the LO is 180 MHz.

190 MHz sine-wave input. A local oscillator at 180 MHz was applied. The IF at 10 MHz is clearly visible for both I and Q channels. The image rejection was measured from the complex FFT to be 62 dB. With higher RF, the SNR is expectedly lower than for 10 MHz input (Fig. 7). This is due to the lower input RF amplitude necessary to stay within the delta ADC slew-rate limit—the maximum signal; for example, at 190 MHz is about 25.5 dB less than that at 10 MHz. Additionally, the SNR is reduced by the mixing of out-of-band quantization noise with the harmonics of the single-bit square-wave LO [3]. At higher input frequencies, the excess noise contribution due to mixing by the LO harmonics is lower since fewer of them contribute [6].

The second system we tested is based on the XADR chip with the X-band 2nd order delta-sigma band-pass ADC modulator shown in Fig. 3(b). It directly digitizes X-band RF signal using a 30.72 GHz clock.

In order to demonstrate a complete satellite receiver operation, we interfaced our cryocooled X-band digital-RF receiver with a digital modem (courtesy of L-3 Communications), which was specially modified to accept and demodulate digital I and Q digital data. The complete receiver system was tested with live satellite signals at HYPRES first, and then at the customer lab where it received signals from the XTAR satellite at the satellite

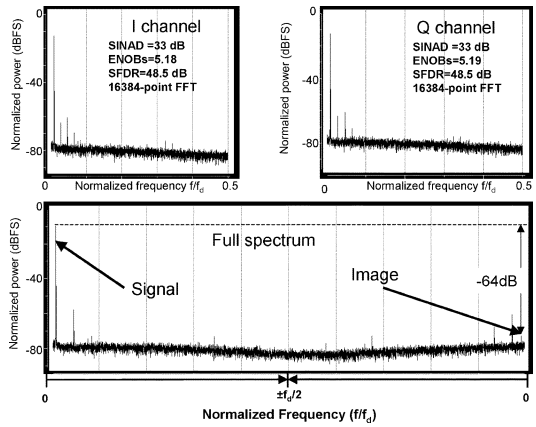

Fig. 10. The X-band ADR system test. The 16384-point spectra of the I- and Q-channel outputs with the full spectrum (I+jQ) measured at 30.72 GHz clock and acquired at 110 Ms/s. The input tone frequency is 7679 MHz and the LO is 7680 MHz.

communication terminal [7]. Previously, we tested X-band ADR system with single tone signals and different pseudo-random patterns as well as demonstrated this system with live transmission and reception of a video file [7]. These tests were performed with X-band ADR chip fabricated with 1 $\mathrm{kA/cm^2}$ HYPRES process [11] using a 10.24 GHz clock in RF undersampling mode.

The frequency of the local oscillator should be a submultiple of the clock frequency to prevent unwanted mixer artifacts, preferably by a factor divisible by 4 to ensure convenient generation of in-phase and quadrature components. Under these constraints, the clock frequency is given by $\mathrm{f_{clk}} - \mathrm{f_0} = \mathrm{f_{clk}}/4$, or $\mathrm{f_{clk}} = 4\mathrm{f_0}/3$, where $\mathrm{f_0}$ is the center of the band-of-interest. We designed two versions of the X-band ADR chip, for fabrication using HYPRES 1 $\mathrm{kA/cm^2}$ and 4.5 $\mathrm{kA/cm^2}$ processes [11], for target clock frequencies of 10 GHz and 30 GHz respectively.

With the help of the modular cryopackage described in the previous section, we upgraded the X-band ADR system at the Joint SATCOM Engineering Center (JSEC) by substituting the 1 $\mathrm{kA/cm^2}$ ADR with the 4.5 $\mathrm{kA/cm^2}$ version. We received signals from both the DSCS and the newly launched WGS satellites with the upgraded X-band ADR system, clocked at 30.72 GHz. For our chosen carrier, the input RF signal is $\mathrm{f_0} = 7680$ MHz. Cryocooled ADR chip sampled this 7.68 GHz RF input directly with an applied $\mathrm{f_{clk}} = 4\mathrm{f_0} = 30.72$ GHz, and digitally downconverted to baseband. The decimation ratio of digital filter is 256, and consequently, the output decimated clock rate was $\mathrm{f_d} = \mathrm{f_{clk}}/256 = 120$ MHz. The output digital I and Q data at 120 Ms/s are amplified, and passed through the FPGA data acquisition and processing board. We acquired the data from the data board and performed a FFT for display on our GUI. Fig. 10 shows the performance of the X-band ADR chip in terms of SNR and SFDR over the 60 MHz band with a single-tone 7679 MHz input signal. Here the measured SNR was 3 dB better than at the 10.24 GHz clock frequency [7] in a three-times larger bandwidth. Assuming a flat noise floor, further averaging to the same bandwidth brings an extra $10 \cdot \log 3 \approx 5$ dB of SNR.

V. Conclusion

We have successfully demonstrated a cryocooled All-Digital Receiver (ADR) system. The complete system consists of a superconducting chip containing more than 10,000 Josephson junctions packaged in a commercial off-the-shelf cryocooler followed by room-temperature interface electronics and a post-processing FPGA module.

Depending on the targeted application the superconducting chip comprises either a low-pass delta or X-band band-pass sigma-delta modulators together with a digital in-phase and quadrature mixer and a pair of digital decimation filters.

The low-pass system has been operating at 28.16 GHz and the X-band system has been operating at 30.72 GHz clock frequencies. To our knowledge these are the fastest digital receivers demonstrated to date.

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