Superconducting High-Resolution A/D Converter Based on Phase Modulation and Multichannel Timing Arbitration

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***Abstract*—We have developed a flux-quantizing A/D converter (ADC) based on RSFQ elements, employing a novel front end capable of generating high-linearity multibit differential code within a wide dynamic range (up to 16 bits). The front end operates as a phase modulator/demodulator and uses fractional-flux-quantum least significant bit (LSB). It runs at multi-GHz speed, enabling ADCs with large oversampling ratio and effective resolution in excess of 20 bits (after decimation filtering). We have designed, fabricated and tested several versions of a complete ADC using this new architecture and demonstrated its operation with dynamic range of 14 bits. We have also confirmed continuous phase modulation of the flux quantizer with a carrier frequency of 10 GHz.**

I. Introduction

The goal of this work is to present the results of a theoretical and experimental study of a novel flux-quantizing ADC using a voltage-biased single-junction interferometer as a front end device [1],[2]. This new architecture provides considerable advantages over traditional flux-quantizing ADCs using two-junction interferometers [3],[4], e.g. it completely eliminates conversion hysteresis [5] and enables fractional-flux-quantum hardware LSB. We will show that the operation principle of this new ADC can be interpreted as a process of phase modulation/demodulation and will derive from it the limitations on its performance. We will also discuss the ADC design, and report our first experimental results obtained with this architecture.

II. Overview of the ADC Architecture

Figure 1 shows the block diagram of the ADC using new single-junction flux quantizer [1],[2]. The ADC consists of a single-junction interferometer L_1, J_1 biased by frequency-stabilized dc voltage source V, a bank of time-interleaved race arbiters SYNC and a decoder unit DEC (which constitute together the differential-code ADC front end), and a decimation filter DSP which provides appropriate digital processing of the differential code. The ADC operates as follows: the dc voltage source V, stabilized by ADC clock frequency f_{clk}, continuously pumps magnetic flux into the interferometer loop L_1 at a rate of $\Phi_0/2$ per clock period, where Φ_0 is magnetic flux quantum. As a consequence, a pulse train with a frequency of $f_{clk}/2$ is generated by the interferometer Josephson junction J_1, and then amplified by

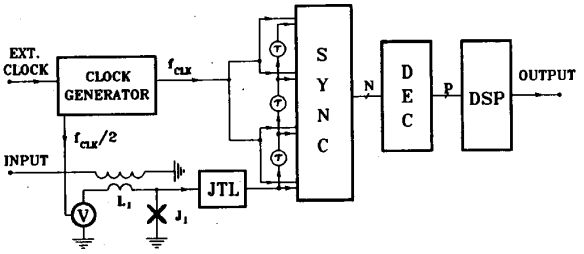

Fig. 1. Architecture of superconducting flux-quantizing ADC using a voltage-biased single-junction flux quantizer.

the Josephson transmission line JTL. As shown in [1],[2] the phase of this output pulse train is linearly and continuously dependent on the magnetic flux applied to the interferometer loop L_1 by the input current, and 2π of this phase corresponds to a single flux quantum in L_1. The next ADC stage performs demodulation of this phase-modulated pulse train by using N race arbitration channels SYNC, which perform synchronization of the train pulses with the ADC clock frequency f_{clk} [4]. These N channels are uniformly interleaved within one clock period by using delay elements $\tau = 1/Nf_{clk}$, so phase resolution of π/N is achieved. The same resolution (hardware LSB of the ADC) in flux units is $\Phi_0/2N$, while the ADC slew rate limit is $\pm N$ hardware LSBs per clock period [2]. The 1-bit outputs of the channels are summed together by the decoder unit DEC, yielding multibit differential code. Finally, the differential code is integrated, low-pass-filtered and decimated by the decimation filter DSP.

III. Analysis of ADC Operation

A. Phase Modulation.

Figure 2 shows a circuit diagram of the analog part of the ADC front end - phase modulator. Its left part is a dc voltage source which consists of an RSFQ T flip-flop, which generates a pulse train at half of the clock frequency, a Josephson transmission line (JTL) amplifier, which passes this pulse train to a large Josephson junction J_0, and a low-pass filter circuit L_0, R_0 which rejects the ac voltage components of the pulse train. The dc component of the voltage $V_0=\Phi_0 f_{clk}/2$ is then passed to a single-junction interferometer L_1, J_1, which performs phase modulation, as described in Section II.

The voltage generated by the junction J_0 is a periodic pulse train with a frequency $f_{clk}/2$, with pulses carrying single flux quanta Φ_0. Therefore, in order to support the flux

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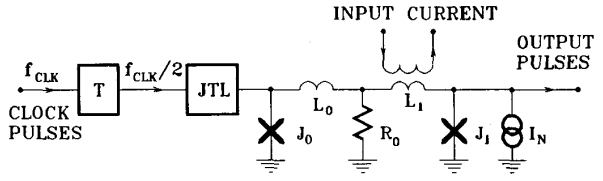

Fig. 2. Superconducting flux-quantizing phase modulator.

resolution of the demodulator (which is $\Phi_0/2N$) the L_0, R_0 circuit should attenuate all ac components by at least $1:2N$ ($L_0/R_0 > 2N/\pi f_{clk}$). At the same time the resistor R_0 should not overload J_0 at dc, i.e. $I_{c0}R_0$ product should be larger than V_0. These two conditions can be expressed as:

$$2N/\pi L_0 < f_{clk}/R_0 < 2I_{c0}/\Phi_0. \quad (1)$$

As we can see, the product $\pi I_{c0}L_0/N\Phi_0$ gives us the relative span of f_{clk} values, while R_0 can be used to adjust f_{clk} to any desired absolute value. For instance, assuming N=4, I_{c0}=1 mA and L_0=10 pH, the range of f_{clk} for R_0=0.1 Ohm is from 25 GHz to 100 GHz, while for R_0=0.01 Ohm it is from 2.5 GHz to 10 GHz.

The total loop inductance $L=L_0+L_1$ is limited also by the thermal noise, represented in Fig. 2 as a current source I_N in parallel with the junction J_1. The noise current I_N is typically several μA at 4.2 K [6]; it creates effective noise flux in the interferometer loop $\Phi_N=LI_N$. This flux should be less than one LSB ($\Phi_0/2N$); hence the upper limit on L is $\Phi_0/2NI_N$. For instance, N=4 and I_N=5 μA yield L < 50 pH.

B. Phase Demodulation

Figure 3 shows how the conversion of a phase-modulated pulse train to multibit differential code is realized with a 4-channel synchronizer. The top trace shows the ADC input signal (a step with large rise time); its flux amplitude is $\Phi_0/2$, while phase amplitude is π. As shown in Fig. 1, the phase-modulated pulse train is replicated in 4 copies having mutual time delay of $\tau = 1/4f_{clk}$, which are passed to 4 synchronizer channels (the next 4 traces in Fig. 3). For each channel the arrival (absence) of input pulse within a given clock period produces output of one (zero) respectively. The sum of four synchronizer outputs (calculated by the decoder DEC) varies from 0 to 4, corresponding to differential code from -4 to +4 LSBs, with each count equal to 2 LSBs (this linear transform is done within the decimation filter). The differential code, and its integral ("raw reconstruction") are plotted next in Fig. 3. As we can see, gradual increase of our input phase signal from 0 to π causes distinctive changes in the both waveforms occurring after each LSB increment (π/4), but deviations of the raw phase reconstruction from the actual phase can be as high as ±π/2, or ±2 LSBs. The main reason for these deviations is presence of the carrier frequency ($f_{clk}/2$) in our raw signal. If we remove this component (in Fig. 3 by simple 2-point averaging), we finally reveal the "true" LSB value of π/4.

For wide-bandwidth signals the carrier spectrum is also wide (due to the carrier frequency changing linearly with the signal slew rate), so it cannot be suppressed by simple 2-point averaging. However this wider carrier spectrum does not affect the ADC operation, as long as it stays out of signal band (since it will be removed by the decimation filter).

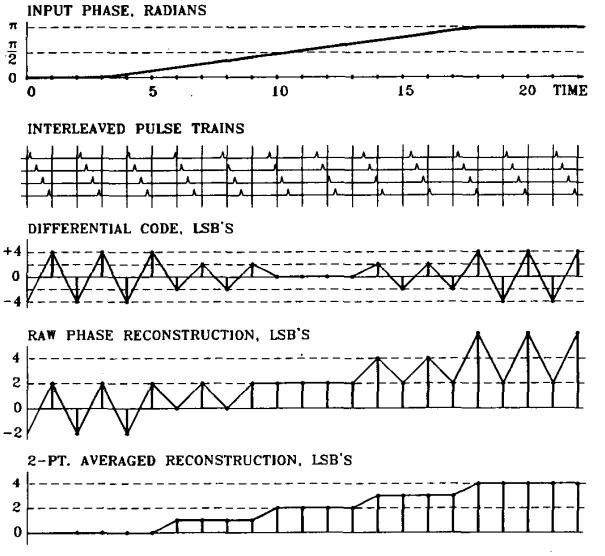

Fig. 3. Phase demodulation process for a system with 4-channel synchronizer.

C. ADC Performance

Dynamic performance of the ADC shown in Fig. 1, i.e. dependence of its effective resolution N_{eff} on signal bandwidth BW was analyzed in our previous work [2] and is given by the formula:

$$N_{eff} = \log_2(N f_{clk} / \pi BW) + \log_2(f_{clk} / 2BW)^{1/2}. \quad (2)$$

Its first term accounts for the slew rate limitation, while the second one - for oversampling gain. Table 1 lists the ADC dynamic performance (2) for two sets of parameters corresponding to the present-day and expected future level of superconducting technology.

TABLE I.
ADC DYNAMIC RESOLUTION IN EFFECTIVE BITS AS A FUNCTION OF BANDWIDTH BW AND SAMPLING RATE f_{out} ($BW=f_{out}/2$).

BW	f_{out}	N=4, f_{clk}=20 GHz	N=16, f_{clk}=100 GHz
5 GHz	10 GS/s	2.9	8.3
0.5 GHz	1 GS/s	7.9	13.3
50 MHz	100 MS/s	12.9	18.3
5 MHz	10 MS/s	17.9	23.3

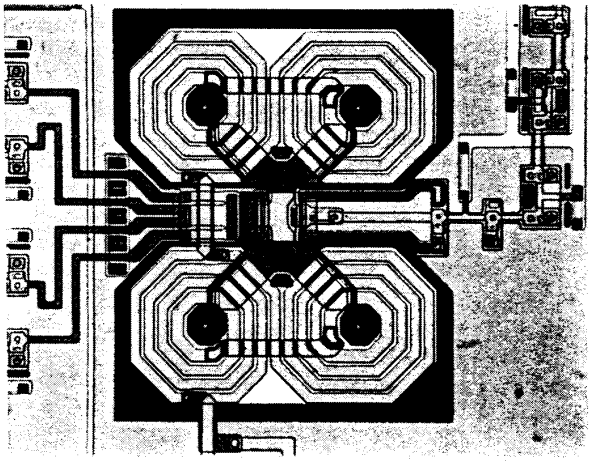

Fig. 4. Layout of the ADC single-junction flux quantizer: center - 16-turn flux quantizer transformer (250x300 μm^2) with single junction J_1 , left - 4-JJ dc voltage source with LR circuitry, right - JTL output amplifier. The flux quantizer parameters are: L_0 = 6 pH, I_{c0} = 1.6 mA, R_0 = 0.05 Ohm, L_1 = 14 pH, I_{c1} = 0.14 mA, M = 165 pH (12.6 μA per Φ_0).

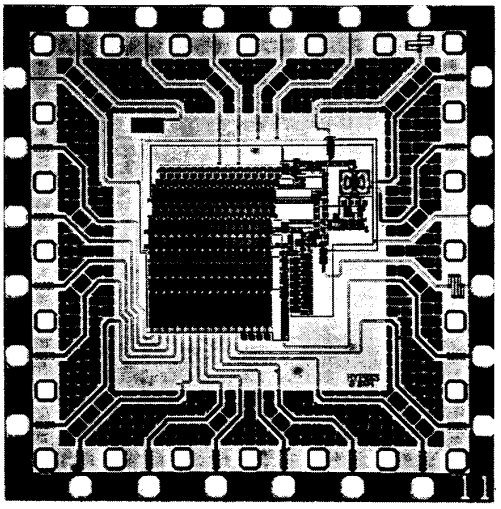

Fig. 5. Layout of 12-bit ADC using 16-bit decimation filter with 1:256 decimation ratio and high-voltage RSFQ output drivers. Chip size is 5x5 mm^2, active area is 2.1x2.4 mm^2.

IV. ADC Design and Fabrication

Figure 4 shows the layout of a single-junction flux quantizer, which uses the same multi-hole transformer as our earlier two-junction flux quantizers [5]. In order to simplify the dc voltage source layout, its single large junction J_0 was substituted with four smaller junctions (4x400 μA), each supplied with an individual LR low-pass filter (L = 24 pH, R = 0.2 Ohm). Using this flux quantizer, we have designed several ADC chips of different complexity. The ADCs were assembled directly from the cells of our dual-groundplane RSFQ library. All ADCs used a single-channel synchronizer and a simplified compact design of the decimation filter (80 μm per bit), so they fit on 5x5 mm^2 chips. Details of ADC implementation go beyond the scope of this report. All chips were fabricated using HYPRES standard 1 kA/cm^2 Niobium technology [7]. The microphotograph of our most complex ADC chip (2415 Josephson junctions) is shown in Fig. 5.

V. Test Results

Most of our test results to date have been obtained with the simplest of our ADC chips (about 400 JJs), which contained a flux quantizer, a clock generator with 1:4 decimation counter, 1-channel synchronizer, 2-point averager and a 4-bit NDRO accumulator with RS flip-flop output drivers. The chip was completely functional with low-speed margins of ±10 %.

Figure 6 demonstrates low-speed operation of the ADC front end (phase modulation principle). It is seen that the phase of the synchronizer output pulse train (viewed via T flip-flop driver) monotonically changes in π increments in response to increasing input signal, as expected. The high speed test of the front end (Fig. 7) was done with a different chip containing four time-interleaved channels (as shown in Fig.1). The test was based on mixing the phase-modulated pulse trains with non-modulated carrier train at 10 GHz. The mixing was performed by standard RSFQ confluence buffer elements. Two traces in Fig. 7 show the outputs of channels 1 and 3 as a function of input signal; the delay between these channels was adjusted (via changing the bias current of JTL delay lines) to provide their mutual phase difference of π.

The results of complete ADC test (conversion of input current to final digital output of the accumulator) are shown in Fig. 8, 9 and demonstrate the hysteresis-free operation

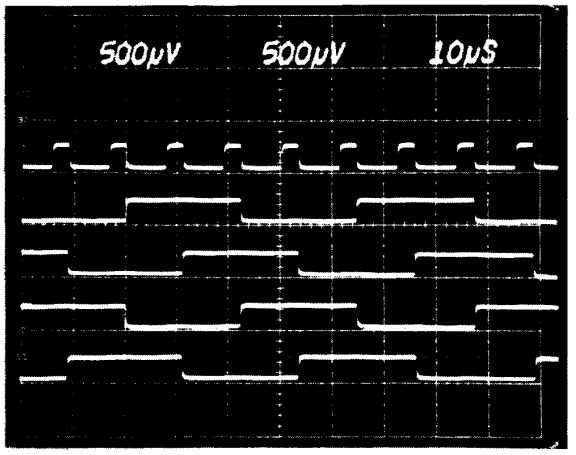

Fig. 6. Low-speed test of the ADC front end with a single synchronization channel. The top trace is ADC internal clock, the other ones are multiple exposures of the synchronizer output for input signal monotonically changing in single LSB increments (displayed via T flip-flop monitor), demonstrating correct phase modulation. LSB value is $\Phi_0/2$ in flux units, and π in phase units.

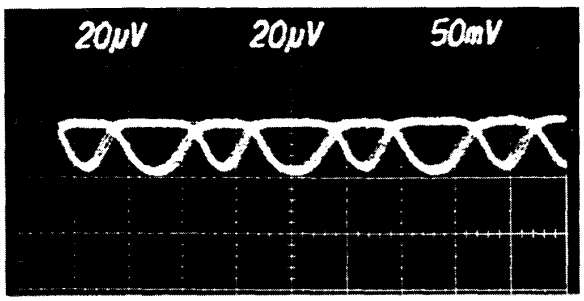

Fig. 7. High-speed test of the ADC analog front end (phase modulator) using 10 GHz carrier frequency. Two traces are outputs of the confluence buffer elements (20 μV/div) which mix two mutually delayed copies of the phase-modulated pulse train with non-modulated carrier train (the delay is adjusted to half of the carrier period). These traces are displayed as a function of the ADC input current (5 μA/div); dips in voltage correspond to coincidence of the trains, which happen 2π-periodically in respect to the train phase difference.

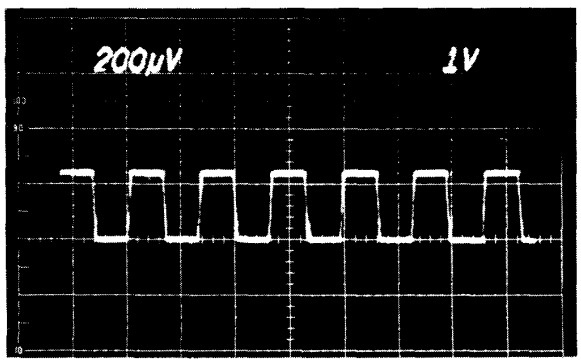

Fig. 8. Least significant bit (LSB) of the ADC displayed as a function of input current (10 μA/div). The photo demonstrates ADC hysteresis-free operation with LSB of $\Phi_0/2$ (6.3 μA) and threshold width below 1 μA. ADC clock frequency is 4 MHz., input frequency is 10 Hz, output amplitude is 250 μV.

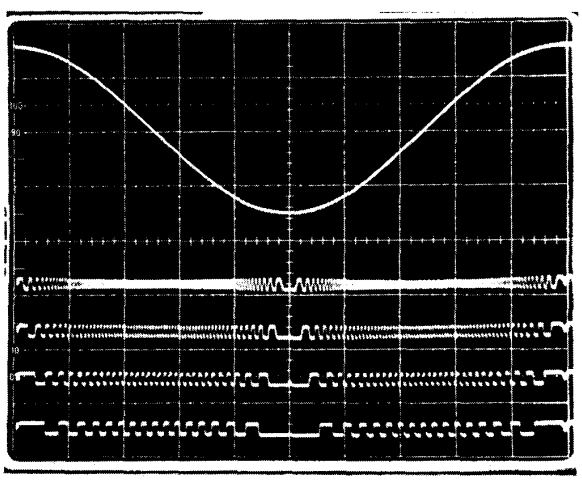

Fig. 9. Operation of the ADC with 8-bit sinusoidal input signal. Top trace - input signal, bottom traces - four ADC outputs (least significant bits). Note that the input minimum corresponds to output 0000, and the maximum - to output 1111, while bit 4 (MSB) goes through 16 periods between the minimum and the maximum. ADC clock frequency is 50 MHz, input frequency is 5 kHz.

with LSB of $\Phi_0/2$ (6.3 μA). The total threshold width (Fig. 8), is below 1 μA. This translates to an effective noise current I_N below ±8 μA (assuming 16-turn transformer), in good agreement with [6]. Figure 9 shows the ADC operation with the dynamic range of 8 bits. The maximum dynamic range of the ADC (for dc input signal) was measured to be ±60 mA (14 bits), which we believe is the highest dynamic range reported to date for a clocked flux-quantizing ADC.

VI. Conclusion

We have analyzed theoretically and demonstrated experimentally a new flux-quantizing ADC based on a single-junction voltage-biased front end. This front end architecture provides wide-dynamic-range hysteresis-free operation with fractional-flux-quantum LSB, and enables generation of high-linearity multibit differential code. We have determined the limitations on ADC parameters and have shown their consistency with the available superconducting technology. We have designed, fabricated and tested several versions of a complete ADC using this new architecture and achieved its low-speed operation with the dynamic range of 14 bits. We have also confirmed continuous phase modulation of the flux quantizer with a carrier frequency of 10 GHz.

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