A Niobium Nitride-Based Analog to Digital Converter using Rapid Single Flux Quantum Logic Operating at 9.5 K

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Abstract—**An analog to digital converter (ADC) using the rapid single flux quantum (RSFQ) logic family implemented in niobium nitride (NbN) technology is described. The circuit was originally developed and demonstrated in niobium technology. An identical circuit was then laid out, fabricated and demonstrated in NbN technology. The chips were fabricated using an eight-layer NbN-based process with Josephson junction critical current density of 500 A / cm^2. In this paper, we report on the measurement results for a 6-bit flux quantizing ADC which exhibited proper operation and good dc bias margins. We will also demonstrate results from an ADC chip operating up to 9.5 K.**

Introduction

THE RSFQ logic family [1] is an ideal technology for the emerging high T_c superconductor technology for several reasons. First, the logic family relies only on non-hysteretic Josephson junctions which seems to be the only type of Josephson junctions realizable in high T_c technology. Second, the RSFQ technology is a direct coupled logic and consequently does not require coupled inductors. In the case of logic families with coupled inductors, the coupling efficiency reduces significantly when kinetic inductances are large. NbN and high T_c superconductors possess high penetration depths and thus inductors based on these superconducting materials suffer from high kinetic inductance. High kinetic inductance makes designing circuits in such technologies rather difficult because of reduced coupling efficiency. Direct coupled logic also requires a less complex circuit process than technologies with magnetically coupled inductors. In addition, RSFQ also lends itself better to circuits operating with wider bath temperature. RSFQ logic families are based on SQUID gates with properties governed by the product of L and I_c of each gate, where L is the inductance associated with the gate and I_c is the critical current of the gate. Since with increasing bath temperature L increases and I_c decreases the product does not deviate very rapidly from its optimum value with changing bath temperature. Toward the goal of getting operational circuits with higher operating temperatures, we have designed and demonstrated an ADC based on NbN technology operating at estimated 9.5 K. Such ADCs are best suited for applications where sensitivity and high resolution are of importance. We report on the experimental design and demonstration of this flux quantizing ADC.

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Experimental Results

The NbN process used in fabrication of the flux quantizing ADCs has been described, rather extensively, elsewhere [2] and is summarized in Table I. This process is based on all-NbN process where tunnel junctions are fabricated using a thermally grown magnesium oxide film for better reproducibility, and is similar to a niobium process routinely being used for fabrication of Nb-based circuits. Thermally-oxidized magnesium barriers offer a higher degree of control over the tunnel barrier thickness, which results in a significant improvement over processes where the tunnel barrier is directly deposited from an MgO target. High quality tunnel junction devices have been achieved with good tunneling characteristics for devices as small as 3 μm^2 and energy gap voltages of more than 5.1 mV. Chips were fabricated with current density of 500 A/cm^2 and the minimum junction size of 3.5 $\times$ 3.5 μm^2. Fig. 1 exhibits typical results for this NbN tunnel junction process. Fig. 1a shows a string of 3.5 $\times$ 3.5 μm^2 junctions exhibiting energy gap of 5.15 mV at 4.2 K. Fig. 2(a)–(c) show NbN energy gap, Josephson junction critical current and penetration depth versus temperature for NbN films and tunnel junctions measured from a SQUID gate. These results indicate that it is not unreasonable to expect RSFQ-based circuit to operate up to and beyond 10 K, for circuits designed to be operated at 4.2 K. Any change in a gate inductance due to increased bath temperature is largely compensated by the reduction in the critical current of the Josephson junction.

The flux quantizing ADC that was developed using NbN technology is similar to the previously-demonstrated circuit in Nb technology [3]. Fig. 3 shows the circuit diagram for one bit of the flux quantizing ADC. A multi-bit flux quantizing ADC consists of a flux quantizing SQUID as the input stage followed by counter chains made of one-bit flip flops with the number of stages matched to the resolution desired.

The design of the flux quantizer requires it to operate with a high level of input current (I_c) and use relatively

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TABLE I

Layer	Material	Thickness (Å)	Function/Property
	NbN	3000	Penetration depth = 3000 Å
1	MgO	–	junction trilayer
	NbN	1000	
2	SiO_2	1000	Insulation
3	Mo	1000	1 Ω per □ Resistor
4	SiO_2	1000	Insulation
5	NbN	5000	Penetration depth = 3500 Å
6	SiO_2	6000	Insulation
7	NbN	7000	Penetration depth = 3500 Å
8	Au	6000	pad metallization

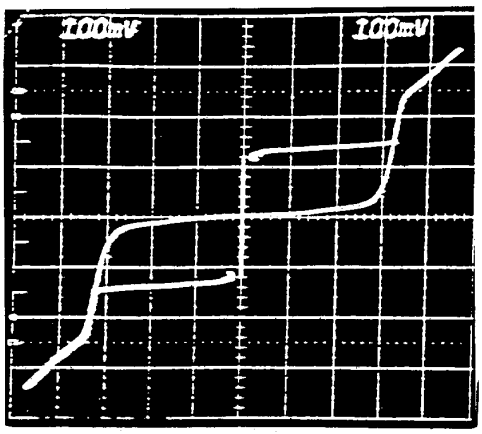

Fig. 1. Volt-ampere characteristics of 64 unshunted NbN-based SQUIDs operating at 4.2 K. Each junction is 3.5 × 3.5 μm^2. Horizontal scale = 100 mV. Vertical scale = 0.1 mA.

high critical current to drive digital circuitry. The transformer must have low output inductance (L) to keep $LI_c < \Phi_0$ and a high turns ratio to maintain good sensitivity. Fig. 4 shows the volt-ampere characteristic of a quantizer gate with 20 turn input coil. different curves correspond to characteristics due to various signal currents in the input coil. The input current ranges from −35 mA to +35 mA and Fig. 4 shows that the quantizer is free from parasitic $\sin(x)/x$ modulation of the junction critical current over this input current. The quantizer has a periodicity of 9.2 μA which results in a quantizer with more than 11 bit effective dynamic range. The mutual inductance between the input coil and the quantizer is estimated to be 225 pH.

Each bit of the ADC consists of a Josephson transmission line, a flip flop and an SFQ to dc converter to facilitate read out. The Josephson transmission line is used to provide current gain to SFQ pulses driving flip flops. Each flip flop consists of 4 shunted Josephson junctions where the stable states differ by the direction of the persistent current circulating in the bottom superconducting loop causing either the bottom-left or the bottom-right Josephson junction to emit SFQ pulse. The SFQ to dc converter is based on a two-junction dc SQUID with slightly hysteretic characteristics.

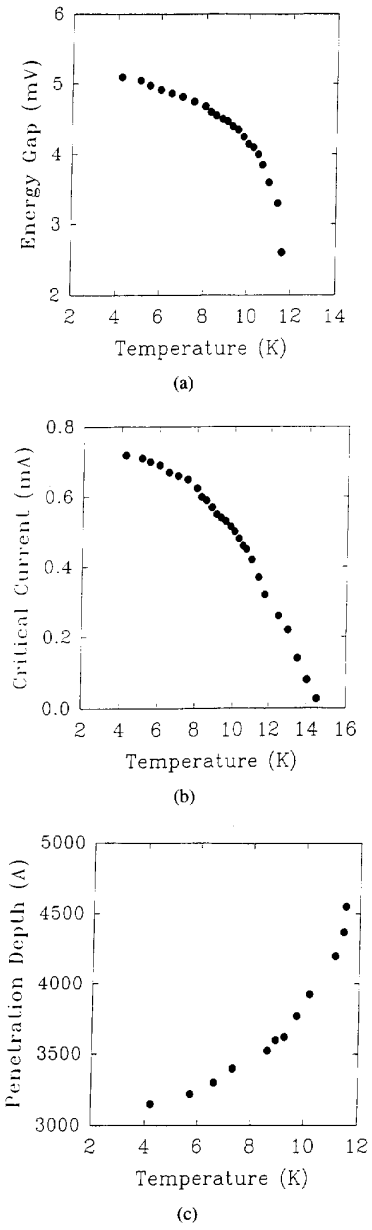

Fig. 2. (a) Energy gap and (b) critical current of Josephson tunnel junctions as a function of temperature (c) Penetration depth of NbN films as a function of temperature.

Fig. 5 shows the simulation results for a 4-bit flux quantizing analog to digital converter. The input signal (not shown) is linearly increasing current into the input coil. As the input analog signal is changing, pulses are generated by the SQUID quantizer. If the signal is increasing in amplitude, one pulse is emitted from the positive output (shown) for every crossing of a threshold boundary. If the signal is slewing in the negative direction, pulses are emitted from the negative output (not shown).

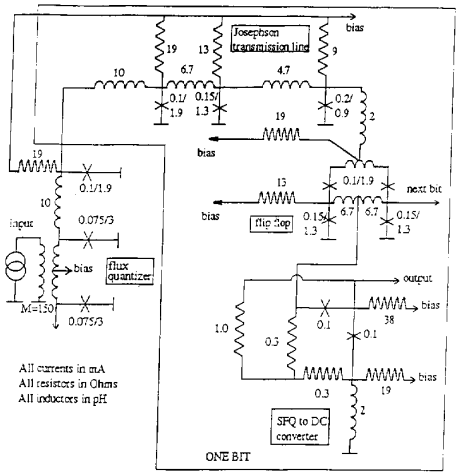

Fig. 3. Circuit diagram of one bit of the counter based on RSFQ logic family. Each bit consists of a flip flop circuit as well as a RSFQ to dc converter to facilitate read out. The numbers next to each Josephson junction are the *critical current/shunt resistance* of the corresponding device.

TABLE II

Inductor	Design Value (pH)	Measured Value (pH)
Transmission Line	6.7	5.5
Flip Flop	13.4	12.2
Transmission line/ flip flop	2	3.45

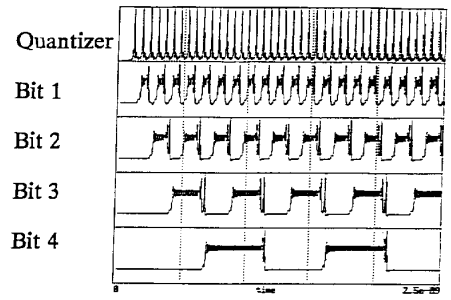

Fig. 5. Simulation results for a 4-bit ADC. The first trace is the output of the quantizer. The following four traces are the outputs of the four cascaded flip flop that correctly exhibit successive division by 2.

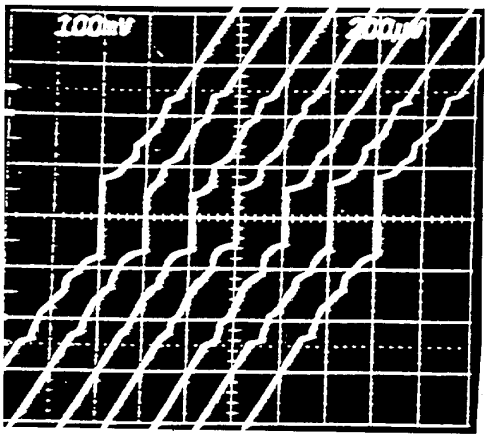

Fig. 4. Volt-ampere characteristics of an NbN-based flux quantizer for various input currents. The range of input current is ± 35 mA and the quantizer period is 9.2 μA. This results in a quantizer with more than 11 effective bits. Data is taken at 4.2 K. Horizontal scale = 0.2 mV. Vertical scale = 0.1 mA.

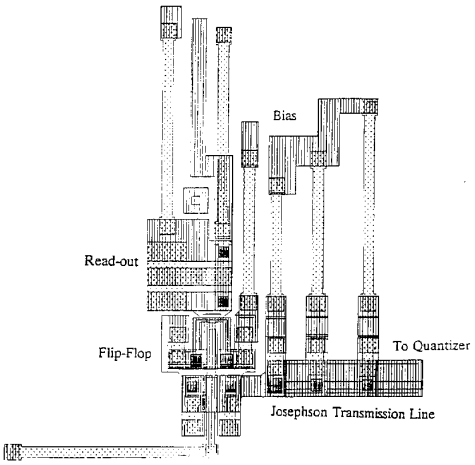

Fig. 6. Layout schematic of one-bit counting ADC for NbN technology.

When the signal is steady, no pulse occurs on either output. The simulation result for the 4-bit A/D converter, exhibited in Fig. 5, shows the desired operation of the binary counter part of the ADC at a speed of 15 GHz. The net difference in number of pulses registered by the counters attached to the separate outputs of the quantizer can be directly related to the net change in input signal amplitude.

We laid out, fabricated and tested a multi-bit ADC chip using NbN technology. It took only two design and fabrication iterations to demonstrate functioning circuits. The ADC design is based on well-proven circuits demonstrated previously in Nb technology where they were successfully transferred to NbN technology without any redesign. Fig. 6 shows the circuit layout for a one bit of the ADC. The layout for the NbN-based circuit process is considerably different from the Nb-based circuit because of the rather high penetration depth associated with NbN films. NbN films exhibit penetration depth of 3000–3500 Å, depending on the base material, compared with 800 Å for niobium films. Niobium nitride deposited on a thermally grown SiO_2 (such as base electrode of the junction trilayer) has a penetration depth of 3000 Å, while similar NbN films grown on deposited SiO_2 (such as wiring levels) have penetration depths close to 3500 Å. This difference is attributed to the different growth structure of NbN films. However, the difference is not so substantial to be taken into consideration for circuit design. Table II ex-

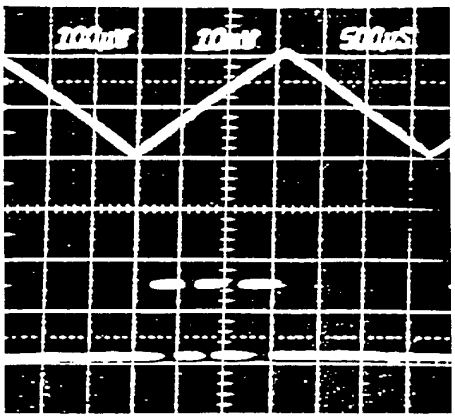

Fig. 7. Experimental results for an NbN-based ADC operating at 4.2 K. The bottom trace shows the output from the first bit of counter due to an input signal (top trace) applied to the quantizer. The positive slewing signal causes the quantizer to go through six transitions detected by the least significant bit of the counter. The output voltage of the SFQ to dc converter is approximately 140 μV. Horizontal scale is 0.5 msec.

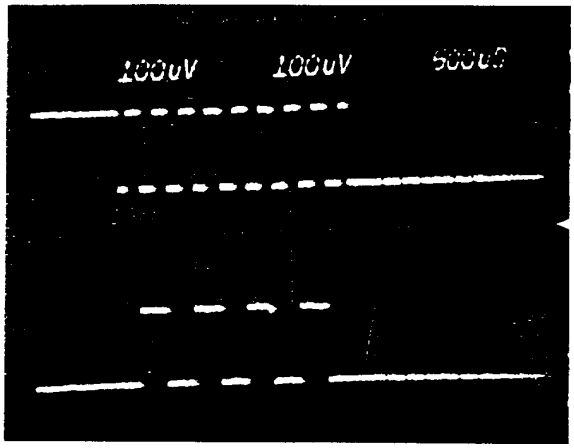

Fig. 8. The outputs of the fifth (top) and the sixth (bottom) bits of an NbN-based ADC operating at 4.2 K in response to an input signal. The output voltage of the SFQ to dc converter is approximately 140 μV. The horizontal scale is 0.5 msec.

hibits the measured values for the inductors and compares them with their design values implemented in the one bit counter shown in Fig. 4. Fig. 7 shows the experimental result for the first bit of the ADC coupled to the flux-quantizer at 4.2 K. The result shown in this figure is for the positive-slewing signal and clearly demonstrates that the quantizer goes through six phase transitions for the applied magnetic field to the quantizer. Fig. 8 shows the outputs for the fifth bit and the sixth bit of the counter. The experimental dc bias margins for all of the gates, with the exception of the flip flops, are approximately $\pm 8\%$ at 4.2 K. The flop flops exhibited almost no bias margins due to insufficiently damped Josephson junctions. Several of these chips have been tested and we, essentially, obtained similar results.

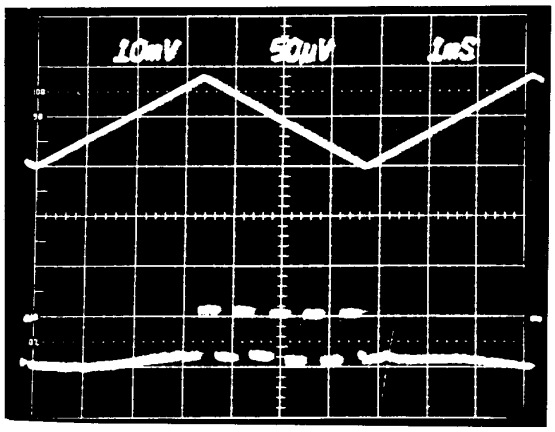

Fig. 9. Experimental results for the first bit of the counter operating at 9.5 K. The output voltage of the SFQ to dc converter is approximately 50 μV. Horizontal scale is 1 ms.

We also evaluated a chip at bath temperatures greater than 4.2 K. Fig. 9 shows the results for the quantizer and the first bit of the counter when operated at approximately 9.5 K. In this case, while adjusting DC bias currents for proper operation, the cryogenic probe containing the superconducting chip was pulled slowly out of the liquid helium reservoir. The circuit ceased operation at about 9.5 K, presumably due to low gate critical currents that was masked by noise. There was no indication that any Josephson junction or superconducting line switched to a normal state. The bath temperature was estimated from the reduction of the Josephson critical currents using the data exhibited in Fig. 2(a).

In conclusion, we have demonstrated an all NbN-based ADC functional at 9.5 K. This ADC is well suited for applications where linearity and high resolution, such as focal plane array and photon counting are necessary and operation close to 10 K is desirable.

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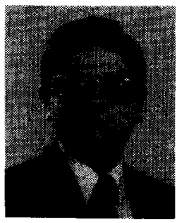

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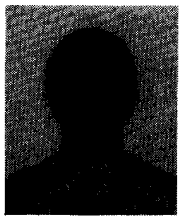

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