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INVITED PAPER *Special Section on Recent Progress in Superconductive Digital Electronics*

Superconductor Digital-RF Receiver Systems

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SUMMARY Digital superconductor electronics has been experiencing rapid maturation with the emergence of smaller-scale, lower-cost communications applications which became the major technology drivers. These applications are primarily in the area of wireless communications, radar, and surveillance as well as in imaging and sensor systems. In these areas, the fundamental advantages of superconductivity translate into system benefits through novel Digital-RF architectures with direct digitization of wide band, high frequency radio frequency (RF) signals. At the same time the availability of relatively small 4 K cryocoolers has lowered the foremost market barrier for cryogenically-cooled digital electronic systems. Recently, we have achieved a major breakthrough in the development, demonstration, and successful delivery of the cryocooled superconductor digital-RF receivers directly digitizing signals in a broad range from kilohertz to gigahertz. These essentially hybrid-technology systems combine a variety of superconductor and semiconductor technologies packaged with two-stage commercial cryocoolers: cryogenic Nb mixed-signal and digital circuits based on Rapid Single Flux Quantum (RSFQ) technology, room-temperature amplifiers, FPGA processing and control circuitry. The demonstrated cryocooled digital-RF systems are the world's first and fastest directly digitizing receivers operating with live satellite signals in X-band and performing signal acquisition in HF to L-band at ~30 GHz clock frequencies.

key words: *RSFQ, direct digitization, cryocooler, ADC, digital channelizer*

1. Introduction

Next generation radio frequency (RF), imaging, and sensor systems demand better utilization of the frequency spectrum, moving towards higher frequency, greater bandwidth and sensitivity, greater flexibility to accommodate diverse functions ranging from communicating voice, data, video to detection, surveillance, ranging, and electronic countermeasures. Conventional analog system implementations have many performance limitations that include frequency dependency, non-linearities, high insertion losses, circuit tuning requirements and expensive waveguide inter-connections that ultimately limit the performance of the complete receiver system. These limitations are greatly multiplied when operational scenarios require multiple frequency and channel configurations.

Solving these problems requires extension of digital processing to the traditionally analog RF domain. Superconductor Rapid Single Flux Quantum (RSFQ) electronics with ultrafast digital logic and high-linearity analog-to-digital converters, allows direct digitization of RF signals and digital processing of the digitized RF signals up to very high RF frequencies. Such direct-conversion system approach has been realized with Digital-RF architecture. This architecture enables digital signal distribution system and can provide multiple band, frequency and channel operation within a single integrated system. Digital signal processing and distribution effectively eliminates most analog RF and all analog IF processing and distribution.

Recently, we have developed first RSFQ digital-RF receivers, integrating RF signal digitizers and digital signal processing (DSP) modules into a single chip. The digitizers are based on oversampling delta or delta-sigma modulators performing analog-to-digital conversion. Digital signal processors are digital channelizers performing digital down-conversion and filtering. We have assembled and demonstrated complete cryocooled All-Digital Receiver (ADR) system prototypes using a hybrid-technology-hybrid-temperature system integration approach. We integrated the digital receiver superconductor chips with commercial 4 K cryocoolers and room-temperature interface electronics. In this paper, we will review the latest results in the development and demonstration of digital-RF receiver systems.

2. Digital-RF Architecture

Figure 1 explains the fundamental nature of our approach — Digital-RF architecture. It eliminates analog RF chains which are fundamentally responsible for overall system cost, size, weight, and power. The overall system performance is also set by these analog elements. Our approach is

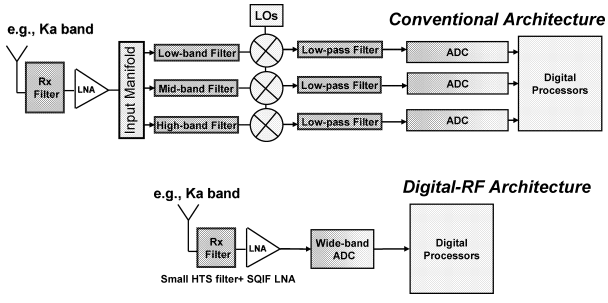

Fig. 1 Comparison of conventional and Digital-RF receiver architectures.

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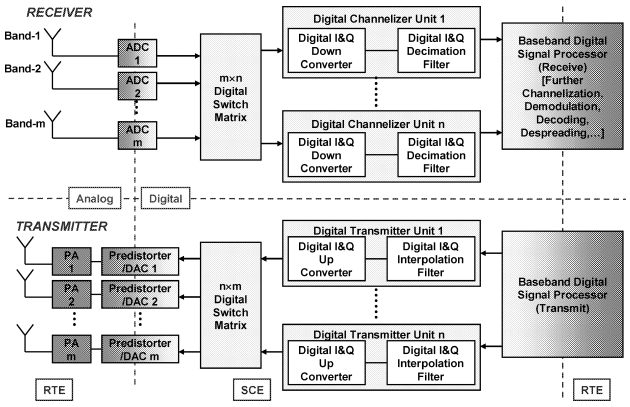


Fig. 2 Block diagram of a programmable multi-band, multi-channel Digital-RF Transceiver. It employs a combination of cryogenic superconductor electronics (SCE) and room-temperature electronics (RTE) elements located on different temperature stages of a cryocooler.

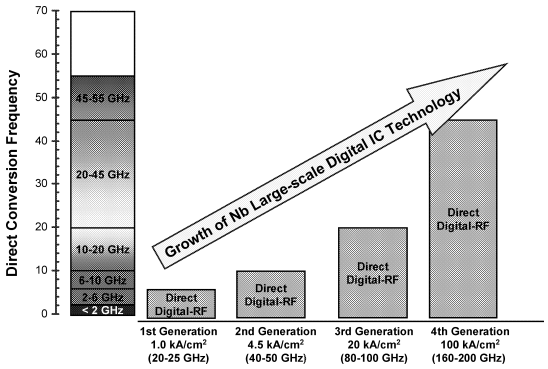


Fig. 3 Expected progress of directly digitizing Digital-RF systems with better fabrication process.

to move the Digitization Point (DP) — conversion between analog and digital — as close to antenna aperture as possible. Such a disruptive architecture change only can be implemented if analog/digital converters and digital logic are capable of delivering the required high-speed and high-fidelity operation. Superconductor technology including analog-to-digital converters (ADCs) and digital processing circuits have demonstrated their ability to meet these tasks.

This approach can also be extended to a transmitter to form an entire Digital-RF transceiver architecture (Fig. 2). In the multi-band, multi-channel architecture the multi-cast on-chip digital switch matrix provides programmable, rapidly configurable, high speed connectivity between frequency-dependent components (ADCs & DACs), which are matched to the bands of corresponding antennas and frequency independent high speed DSP modules. These DSP modules are replicated as necessary to provide the required number of independent channels.

3. RSFQ Circuits for Digital-RF Receivers

Digital-RF systems consist of front-end signal digitizers followed by digital signal processing circuits. The signal digitizers are based on various oversampling ADC modulators including low-pass and band-pass designs depending on band of interest [1]. Currently, we are able to digitize directly as high as ∼20 GHz (Ka band) RF signals. In order to digitize even higher frequency signals, some analog downconversion can be utilized. With progress in fabrication technology, we expect advancing direct digitization to higher RF frequencies as illustrated in Fig. 3.

Digital signal processors process high speed data produced by signal digitizers. These are single- or a few-bit wide data streams at high sampling clock. We have developed several DSP circuits to perform channelizing and filtering functions.

3.1 Signal Digitizers: Analog-to-Digital Converters

3.1.1 Low-Pass ADCs

We use delta modulators for the implementation of low-pass ADCs. We developed a phase-modulation-demodulation (PMD) ADC scheme which was extensively evaluated [1]. Since the PMD ADC really measures the signal derivative, its maximum input is determined by a slew rate limit corresponding to a flux rate of $\Phi_0/2$ (Φ_0 = 2.07 fWb) per clock period, of either sign. In this ADC, the signal to noise ratio (SNR) changes at 30 dB/decade or 9 dB/octave, corresponds to a first-order oversampling ADC. By changing the decimation ratio N, usually by factors of 2, one can trade-off bits of resolution (*ENOB*) vs. bandwidth at a rate of 1.5 bits/octave. The recent low-pass ADC performance was measured for various input single-tone and two-tone sine waves [2]. One can also use delta-sigma scheme for the implementation of low-pass ADCs [1], [3]–[5].

3.1.2 Band-Pass ADCs

The delta-sigma modulator is the best architecture for direct band-pass sampling, since it shapes the noise around a center frequency and produces the maximum SNR. For example, a band-pass ADC was chosen to minimize the quantization noise in X-band (7.25–7.75 GHz). We developed delta-sigma ADC modulator based on a continuous-time scheme [6] with two lumped LC resonators (Fig. 4(a)). One of the unique features of the superconductor delta-sigma ADC modulators is implicit feedback: when the bottom junction (J2) of the two-junction clocked comparator switches (Fig. 4(b)), it subtracts a single flux quantum Φ_0 from the input while producing a digital output SFQ pulse. Therefore, no explicit feedback loop is needed to construct a first-order ADC modulator. A second-order modulator improves SNR by further suppression of quantization noise. To achieve the second-order noise shaping, an explicit feedback loop is introduced using Josephson transmission lines (JTLs) as active delay elements in addition to a D flip-flop to control the phase of the feedback signal.

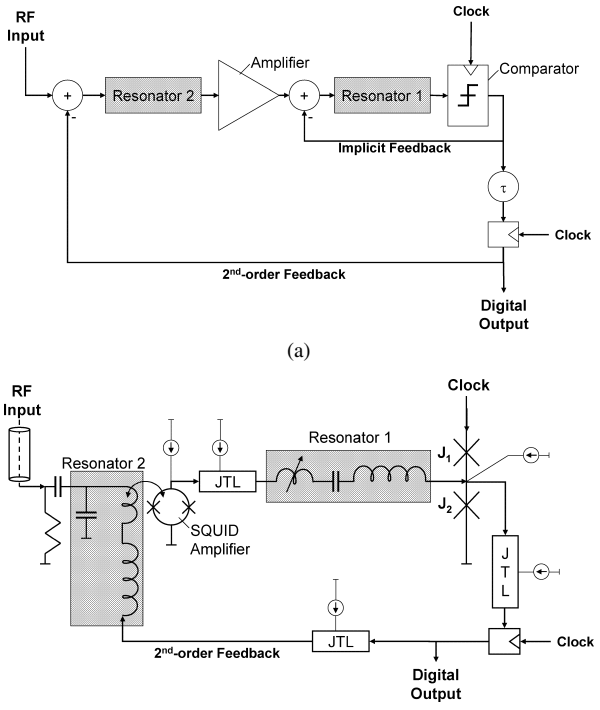


Fig. 4 Second-order bandpass ΔΣ ADC modulator. (a) Block diagram. (b) Schematics.

We have implemented and tested several second-order ADCs centered around various RF frequencies: 4 GHz, 5 GHz, 7.5 GHz, and 20 GHz. For 1 GHz ADC, only a first-order ADC was demonstrated.

Typically, the clock frequency for a bandpass ΔΣ ADC is chosen to be $f_{clk} = 4f_0$, where f_0 is the center of the band-of-interest. For X-band, this desired clock frequency is about 30 GHz. One can also use a lower clock frequency with some performance penalty. In this scheme, called RF undersampling, we take advantage of the sampling process that replicates the input analog frequency band, centered at f_0, translated by multiples of the sampling frequency (f_{clk}). In general, the sampled spectrum consists of an infinite number of band replicas at $\pm f_0 \pm nf_{clk}$, where $n = 0, 1, 2, \ldots$, but we are primarily interested in the first Nyquist zone $0 < f < f_{clk}/2$. For $f_{clk} > f_0$, the band center is shifted from f_0 to $f_{clk} - f_0$. We will need to apply a digital local oscillator at that frequency ($f_{LO} = f_{clk} - f_0$) to mix it down to baseband. Furthermore, the local oscillator should be a submultiple of the clock frequency to prevent unwanted mixer artifacts, preferably by a factor divisible by 4 to ensure convenient generation of in-phase and quadrature components. The highest clock frequency under these constraints is given by $f_{clk} - f_0 = f_{clk}/4$, or $f_{clk} = 4f_0/3$, which for X-band is about 10 GHz. This band-pass ADC design was extended to Ka-band digitization. The ADC with a 20.362 GHz center frequency was tested in the RF undersampling mode using 27.136 GHz clock.

We also demonstrated X-band ADC in oversampling mode. Figure 5 shows the spectrum of a 7.653 GHz RF input

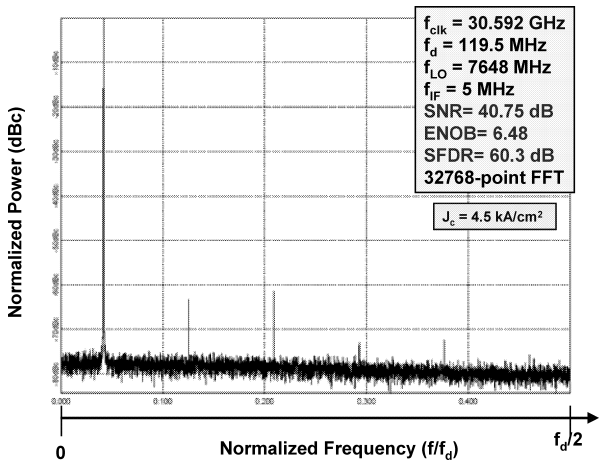


Fig. 5 Spectrum of the digitized output from an X-band ADC chip clocked above 30 GHz. The chip consisting of a band-pass ADC modulator, digital mixer and digital filter. The applied analog input signal is 7.653 GHz.

signal that has been digitized at $f_{clk} = 4f_{LO} = 30.592$ GHz and digitally down-converted to 5 MHz. The decimation ratio is 256 and the output sampling rate is 119.5 MHz. Compared to the results obtained with 10 GHz clock, both SNR and spur free dynamic range (SFDR) are higher over a larger bandwidth.

3.1.3 Digitizer with Analog Downconversion Stage

For input frequencies significantly above 20 GHz, it is impossible to perform direct digitization using available state-of-the-art fabrication process (e.g., 4.5 kA/cm^2). In this case, an analog downconversion has to be used. Figure 6 show a block diagram and chip microphotograph of a signal digitizer developed for mm/submm input signals [7]. This receiver expands the original work described in [8]. It consists of a local oscillator together with the superconductor-insulator-superconductor (SIS) mixer and impedance matching structure for better power delivery and to tune out the SIS junction capacitance, a first order band-pass ADC modulator centered for 1 GHz. This ADC digitizes the IF analog output and generates a one-bit digital data stream at a clock rate of the order of 20 GHz or greater. In order to improve noise temperature of this signal digitizer circuit, a SQUID-based IF amplifier is used.

3.2 Digital Signal Processors

The largest part in terms of area and junction count of our Digital-RF digital receiver is a digital signal processor. We have developed and integrated into a Digital-RF receiver a digital channelizer. We also developed and tested separately a digital autocorrelator, which will plan to integrate with the mm/submm wave receiver to form a spectrometer [7].

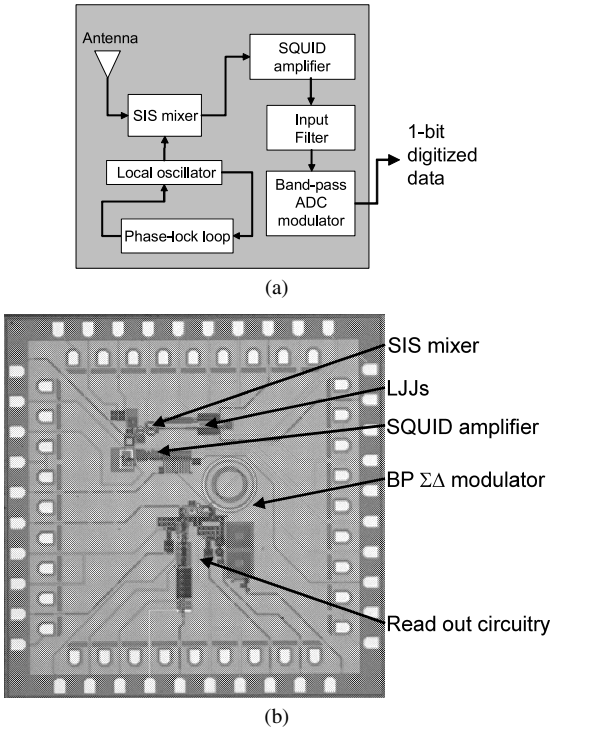


Fig. 6 A mm/submm signal digitizer designed for 350 GHz input signal. (a) block diagram. (b) a microphotograph of the mm/submm digitizer test chip ($5 \times 5\,\mathrm{mm}^2$).

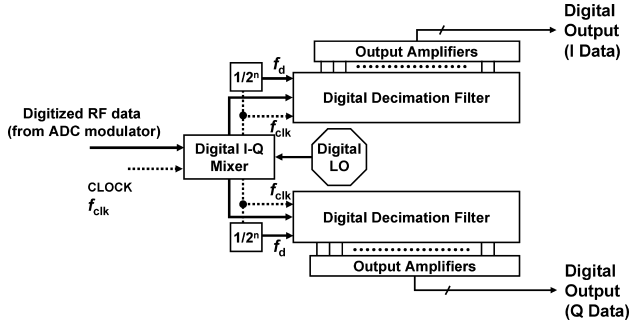


Fig. 7 Block diagram of a single channel of digital channelizer comprising a digital in-phase (I) and quadrature (Q) digital mixer and two digital decimation filters.

3.2.1 Digital Channelizer

We developed and demonstrated several versions of digital channelizers [9]. As shown in Fig. 7, the channelizer receives ultrafast oversampled digital data from the ADC modulators in form of a single-bit (or a few bit) data stream at the sampling clock rate (up to ~40 GHz with $4.5\,\mathrm{kA/cm}^2$ fabrication process). The channelizer produces two (I and Q) multi-bit digital words at the decimated clock rate $f_d = f_{clk}/2^n$, n is decimation ratio.

In our channelizer, the digitized RF data is down-converted by multiplying (mixing) with a digital local oscillator (LO). We use a single-bit periodic waveform (square wave) as the local oscillator. To ensure exactly 90° relative phase difference, the in-phase (I) and quadrature (Q) local-oscillator (f_{LO}) signals are derived by dividing a signal of frequency $4f_{LO}$ with a binary tree of toggle flip-flops (T). As described in [9], we developed and demonstrated two different versions of such a digital mixer.

As shown in Fig. 7, the digital mixer is connected to two second-order digital cascaded integrator comb (CIC) decimation filters (DDFs) [10]. Although these filters do not possess ideal pass-band characteristics and sharp cut-off, they are adequate for our application and easy to implement in RSFQ technology. The CIC filter does not require multipliers and is therefore the fastest. Since our ADCs are sampled at very high speed, the filter must also operate at the same high speed (20–40 GHz).

In our case, the oversampling ratio is very high and digital channelization is performed in two stages. The initial digital filter does not need to reduce the sample rate all the way down to the required Nyquist sample rate but only to a low enough rate (e.g., below 400 MHz for the current FPGA state-of-the-art) for the room-temperature electronics to perform the subsequent filtering function. This allows the first stage channelizer (e.g., an RSFQ channelizer) not to have an ideal pass-band and stop-band characteristics as long as subsequent stages can compensate by correcting the gain droop in the pass-band and defining sharp high-order cut-off on the narrower bandwidth.

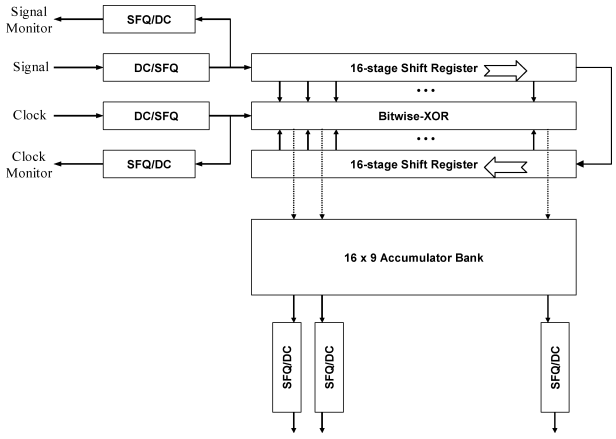
We also developed a multi-rate filter technique which allows the integrator and the differentiator of the comb filter to operate at different sample rates by introducing a down-sampler between them. This approach permits the lower-rate differentiators be implemented using slower room-temperature electronics.

To enable an interface to room-temperature electronics, the channelizer digital outputs are amplified to ~1 mV using high-speed voltage drivers designed to fit a 200-μm width, defined by that of a decimation filter bit slice [9]. The rise time of this device was measured to be 700 ps and the output amplitudes into a 50 Ohm load were 2.5 mV at 300 MHz and 1.3 mV at 1 GHz respectively for the $1\,\mathrm{kA/cm}^2$ process.

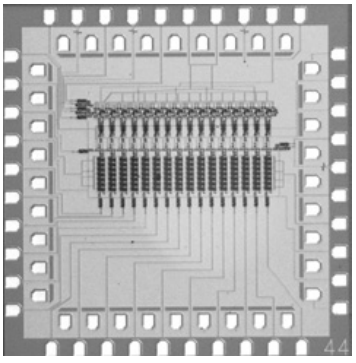
3.2.2 Digital Autocorrelator

For spectrometry applications, one can use the correlator circuit as a digital signal processor. One classic way to obtain the frequency spectrum of a time-domain signal $f(t)$ is to take the correlation between $f(t)$ and a time-delayed version of the same function $f(t-\tau)$. The autocorrelation function is then given by $R(\tau) = \frac{1}{T}\int f(t)f(t-\tau)dt$, where the integral is over a long time period T. That will selectively increase coherent frequency components that are periodic with time τ; other components will exhibit a random walk. For a rapidly changing signal, this correlation function must be computed in real-time, by using a large number of correlators and accumulators in parallel.

Figure 8 shows the block diagram of a 16-channel digital autocorrelator. The digital 16-channel autocorrelator



(a)



(b)

Fig. 8 A 16-lag digital autocorrelator. (a) Block diagram. (b) Microphotograph of chip.

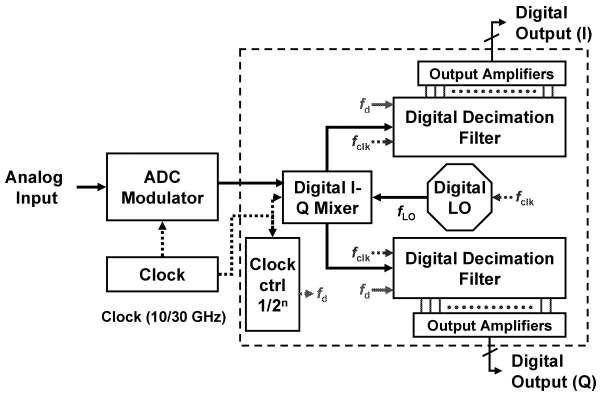


Fig. 9 Block diagram of digital-RF receiver chip (ADR chip) integrating ADC modulator and digital channelizer on a single chip.

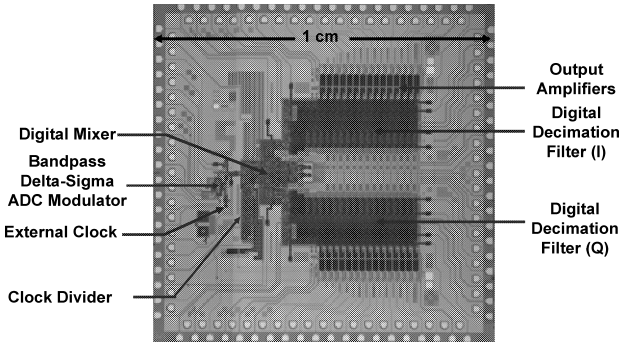


Fig. 10 Microphotograph of a single-channel superconductor X-band Digital-RF receiver chip (XADR). This $10 \times 10\,\mathrm{mm}^2$ chip is fabricated using HYPRES $4.5\,\mathrm{kA/cm}^2$ process and comprises about 11,000 Josephson junctions.

forms a linear array with two main parts: digital delay lines (shift registers) with multipliers (XOR elements) and an array of binary counters. The binary counters form an Accumulator Bank and comprised of T flip-flop gates, outputting only the most significant bits. The individual components of the design — the circular shift register, XORs and T flip-flop gates are well known and have been reported to have very wide operating margins in many studies. Recently, we have demonstrated a ∼20 GHz operation of the RSFQ autocorrelator [11].

4. Superconductor Digital RF Receivers

To date, we have developed and demonstrated several single-channel digital-RF receiver (or All-Digital Receiver (ADR)) chips integrating an ADC modulator (low-pass or band-pass) with a single-channel digital channelizer (Fig. 9). In order to integrate a multi-channel digital-RF receiver (as shown in Fig. 2), multi-chip module (MCM) integration is required. Similarly, the MCM integration is required for the mm/submm spectrometer with more than 32 lags. In this review, we only describe our single-chip digital-RF receivers. Their designs and results of characterization in liquid He testing are described in [9]. We implemented ADR chip designs using HYPRES fabrication processes with $1\,\mathrm{kA/cm}^2$ and $4.5\,\mathrm{kA/cm}^2$ critical current densities. The maximum clock frequency achieved was ∼14 GHz for a $1\,\mathrm{kA/cm}^2$ ADR and ∼31 GHz for $4.5\,\mathrm{kA/cm}^2$ ADR chips. Figure 10 shows a microphotograph a typical ADR chip comprising about 11,000 Josephson junction. The chip takes about 1.1 A of bias current delivered via multiple bias lines. In order to prevent negative effects of ground current distribution [12], large current leads are encased between two superconductor ground plane layers connected via multiple vias. The chip ground hole and moat patterns were optimized to maximize flux trapping resistance and to preserve a symmetrical nature of the chip ground plane design. This allowed us to achieve complete independence from bias current distribution.

It is possible to integrate a multi-band but single-channel digital-RF receiver on a single $10 \times 10\,\mathrm{mm}^2$ chip by integration of multiple ADC modulators to a single channelizer. We designed a chip integrating four ADC modulators (one low-pass delta and three bandpass delta-sigma ADC modulators) with a single-phase digital mixer and a decimation filter as a test circuit (Fig. 11). This receiver test chip allows the operation of only one ADC modulator at a time. The chip was fabricated with the $1\,\mathrm{kA/cm}^2$ process and tested at $f_{clk} > 20$ GHz.

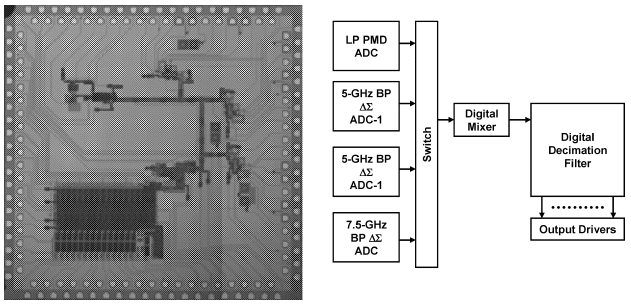


Fig. 11 Multi-band Digital-RF receiver test chip. Microphotograph of a $10 \times 10\,\mathrm{mm}^2$ (left) and block diagram (right) of a circuit with four different ADC modulators connected to a single mixer and filter.

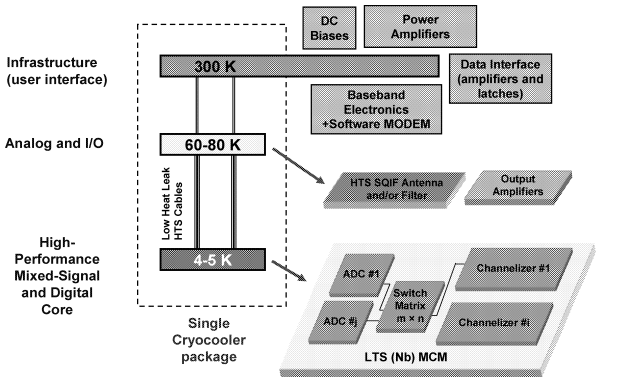


Fig. 12 Hybrid Temperature Hybrid Technology (ht^2) system integration approach.

5. Hybrid Technology Hybrid Temperature (ht^2) System Integration

In order to make superconductor electronics practical, it has to be integrated into room temperature environment. We introduce the Hybrid Technology Hybrid Temperature (ht^2) system integration concept that allows an effective combination of different technologies co-located at different temperature stages of a cryocooler (Fig. 12). It takes advantage of availability of different temperature stages of any 4 K cryocooler. For example, Sumitomo SRDK-101DP-11C cryocooler has two stages (4 K and 60 K). With active temperature control, the 60 K stage can be set for a particular temperature within 60–80 K. The low-temperature superconductor (LTS) digital and mixed signal module is located at a 4 K stage. The warmer temperature stage can host high-temperature superconductor (HTS) circuits such as analog filters, semiconductor (e.g., SiGe) or HTS low-noise amplifiers (LNAs) [13], [14]. This stage is also important for I/O cable heat intercept — the cable thermalization [15]. The room-temperature stage can house various support electronics including baseband digital signal processing, user system interface, bias current source, etc. The choice of circuit technology and operating temperature is driven by system-level performance maximization while minimizing system cost, size, weight and power.

We generally followed the ht^2 approach to integrate our Digital-RF receiver system prototype [16], [17]. Figure 13 shows a 19-inch rack housing the ADR chip cryopackaged on a commercially available 2-stage cryocooler (Sumitomo SRDK-101D-A11), a computer controlled multi-channel current source to bias the ADR chip, room-temperature interface amplifiers, and a PCI FPGA-based post processing module.

The cryocooler was selected due to its relative compactness, adequate heat lift and air-cooled compressor. It equipped with a helium damper to reduce temperature oscillations which might be detrimental for accurate sampling of RF signals. The cryocooler consumes a total wall power of 1.3 kW providing heat lift of 100 mW at 4.2 K and 5 W at 60 K. A single gold-plated radiation shield (without multi-layered insulation for convenience of assembly) is attached

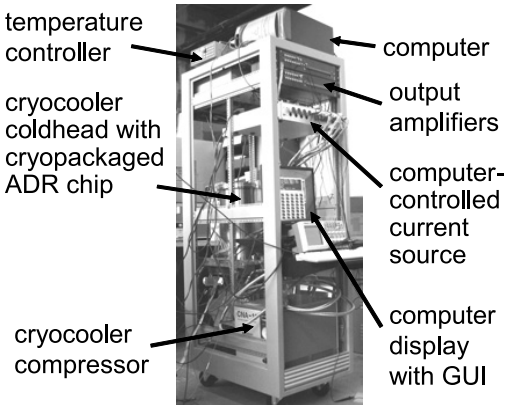


Fig. 13 Fully equipped 19-inch rack with all components of digital receiver system based on Sumitomo 4 K cryocooler.

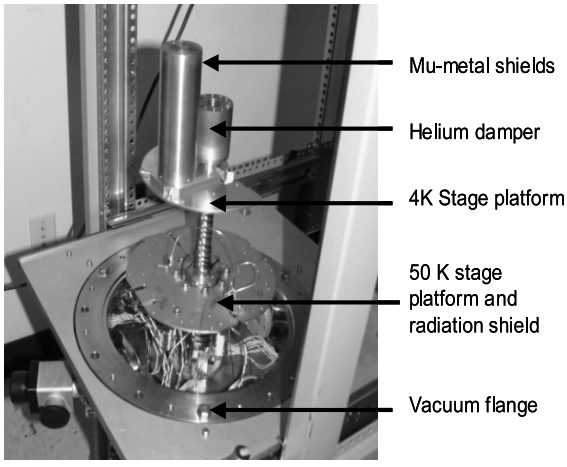


Fig. 14 View of open cryostat with ADR cryopackage mounted on cryocooler coldhead.

to the first stage. The ADR chip module including double mu-metal magnetic shielding attached to the second (4 K) stage (Fig. 14). The design chip module is based upon the pressure-contact 80-line LHe chip cryoprobe design described earlier [18]. This allowed a chip easily be switched between cryocooler and liquid He probe during initial test-

ing.

All the wiring between room temperature and the 4 K module is anchored on the 1st stage 60 K. We use three cable types: copper twisted pairs for dc bias currents (1 mA to 100 mA per bias line), microstrip flex cable for output digital signals, and UT-47 stainless steel coaxial lines for high-speed signals (input RF, external clock, etc.). Earlier calibration of the temperature of each stage as a function of heat applied allowed estimation of thermal loads to both stages: they were 5 W to the first stage at 45 K (mostly thermal radiation) and 150 mW onto the second stage at 3.85 K. The second stage loading was almost entirely from the wiring. Joule heating from the bias leads caused a 0.1 K rise corresponding to an additional 20 mW, whereas on-chip heating, from resistors used to distribute the bias currents, contributed only 2 mW.

One of the most important aspects of cryopackaging for superconductor electronics is magnetic shielding. We achieved low magnetic field by three nested mu-metal shields, two at 4 K and one at room temperature. The resulting field has been measured at about 10^{-7} T, and was similar to fields used for routine testing in liquid He dewars.

For ADR chip current biasing, we built a 48-channel, computer controlled dc bias current source box (Fig. 13). This box operates using less than 300 W of standard AC power [16]. For amplification of ADR output digital signals, we developed a custom amplifier bank consisting of two sets of 16 broadband amplifiers, mounted in the system 19-inch rack (Fig. 13). Each amplifier module consists of a linear stage with an amplitude gain of about 1000 to positive ECL level, followed by a pulse shaping stage that produces standard-level digital signals (LVDS) that are sent to a commercial FPGA data processing board housed in the internal PCI slot of the computer or as a stand-alone module.

6. Digital-RF Receiver Demonstrations

Here we describe test results of two cryocooled digital receiver systems, the X-band ADR system and the HF/L-band ADR system. They were fully integrated onto Sumitomo cryocoolers, equipped with room-temperature interfaces, support electronics, and controlled using GUI. Both systems were first tested at HYPRES laboratory and then delivered and demonstrated at customer facilities.

6.1 HF-to-L-Band ADR System Demonstration

This system is based on the ADR chip with the low-pass ADC modulator and a single-channel digital channelizer. It can digitize RF signals from very low frequencies all the way up to the cutoff frequency of the low-pass ADC input transformer. In practice, we tested this system from HF to L-band. The complete receiver system demonstrator was tested at HYPRES first, and then at the customer facility in Dayton, OH, where has been operated by customers.

The system operated with high reproducibility at clock frequencies up to 24.32 GHz with identical bias settings at

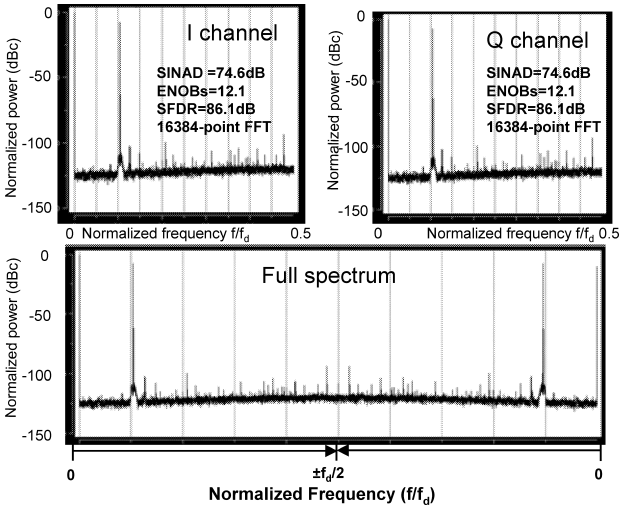


Fig. 15 The HF/L-band ADR system test. Measured spectrum of the digital I and Q data and complex I+jQ FFT for a single 10 MHz tone input sampled at 24.32 GHz clock, digitally filtered, and acquired to FPGA at 95 MS/s.

temperatures from 4.03 K to 4.38 K measured at close proximity to the chip. We performed complete evaluation of the system both with and without applying a local oscillator (LO) input. Figure 15 shows the fast Fourie transform (FFT) for each I and Q channels and complex (I+jQ) FFT (16384 points) from the acquired I and Q data with a single 10 MHz input tone applied with a 10 MHz bandpass filter with ∼1 MHz bandwidth. The full spectrum represents a bandwidth of $f_d = f_{clk}/256 = 95$ MHz. The measured SINAD of 74.6 dB over a bandwidth of 47.5 MHz compares well with 75.7 dB over a bandwidth of 39 MHz produced by our low-pass (LP) ADC [2] with 2-channel synchronizer.

The single tone measurements with 2, 5, 20, and 50 MHz tones were performed with a variety of appropriate band-pass or low-pass filters depending on their availability. To take full advantage of oversampling in our ADR, additional filtering in software was performed. In calculating signal-to-noise ratio (SNR), only noise in the band from 0 to the tone frequency has been integrated. As an example, for a 10 MHz tone at $f_{clk} = 24.32$ GHz with $f_d = 95$ MHz, this additional filtering produced additional 7.15 dB of SNR as compared to the result shown in Fig. 15. This improvement was achieved due to the band reduction ($10 \cdot \log(f_d/2 \cdot 10\,\text{MHz}) = 6.77$ dB) and also due to the elimination of out of band harmonics.

In order to improve ADC linearity, a dither sinewave signal was applied to the input at the decimated clock frequency of 95 MHz. Indeed, data recorded with the dither applied shows the SFDR improvement up to 10 dB, especially for small signal amplitudes. Since the dither signal does degrade SNR somewhat, its power was kept at a minimum. The dither was particularly useful in detection of single tone small amplitude signals.

We test the ADR with variety of RF signals from HF, VHF, UHF, and L bands while the LO frequency was chosen

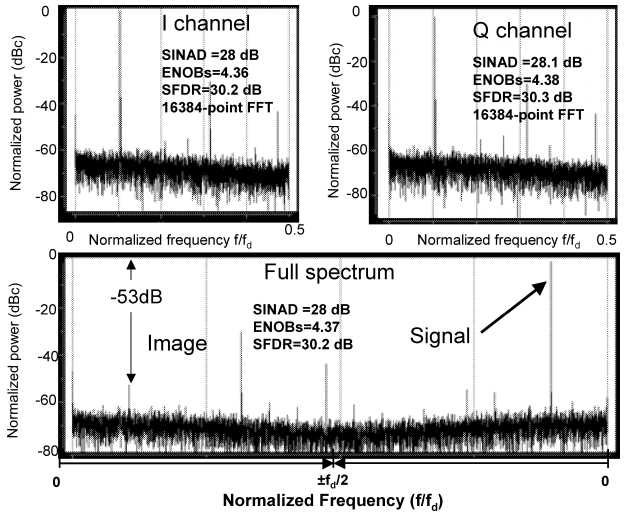


Fig. 16 The HF/L-band ADR system test. The spectra of the I-channel output (top left), the Q-channel output (top right) along with the full 32768-point spectrum (I+Q, bottom) acquired at 24.32 GHz. The input tone frequency is 1.5 GHz and the LO is 1.49 GHz. The output bandwidth ($f_d = f_{clk}/256$) is 95 MHz.

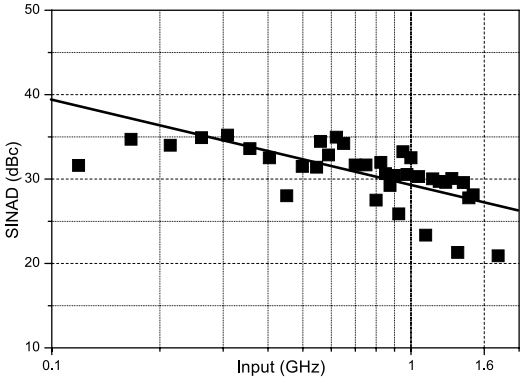


Fig. 17 The HF/L-band ADR system test. SINAD vs. input signal frequency. Line with the slope of 3 dB/octave is also shown.

to obtain a 10 MHz intermediate frequency (IF) response. Figure 16 shows the FFT for I and Q channels and also the complex (I+jQ) FFT (16384 points) with a 1500 MHz sinewave input. A local oscillator at 1490 MHz was applied. The IF at 10 MHz is clearly visible for both I and Q channels. The image rejection was measured from the complex FFT to be 53 dB. With higher RF, the SNR is expectedly lower than for 10 MHz input (Fig. 15). This is due to the lower input RF amplitude necessary to stay within the LP delta ADC slew-rate limit — the maximum signal, for example, at 1.5 GHz is about 43.5 dB less than that at 10 MHz. Additionally, the SNR is reduced by the mixing of out-of-band quantization noise with the harmonics of the single-bit square-wave LO [9]. At lower input frequencies, the excess noise contribution due to mixing by the LO harmonics is greater since more of them contribute [16].

Figure 17 shows the collection of measured data with the input RF signals in VHF, UHF, and L bands. The

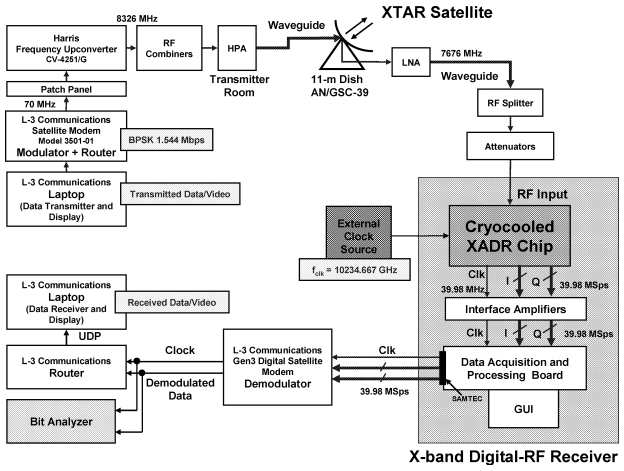


Fig. 18 Block diagram of X-band ADR system demonstration with live XTAR satellite.

corresponding LO signals were applied in order to obtain a 10 MHz IF response. The line with the slope of a 3 dB/octave is also shown for comparison. This line shows the expected performance taking into account a 6 dB/octave loss due to the slew-rate limit and a 3 dB/octave gain of due to decrease of number of LO harmonics within 0–$f_{clk}/2$ band.

6.2 X-Band ADR System Demonstration

This system is based on the XADR chip with the X-band 2nd order delta-sigma band-pass ADC modulator and a single-channel digital channelizer. It directly digitizes X-band RF signal using a 10 GHz clock in RF undersampling mode.

In order to demonstrate a complete satellite receiver operation, we interfaced our cryocooled X-band digital-RF receiver with a digital modem (courtesy of L-3 Communications), which was specially modified to accept and demodulate digital I and Q digital data. The complete receiver system demonstrator was tested with live satellite signals at HYPRES first, and then at the customer lab in Fort Monmouth, NJ, where it received signals from the XTAR satellite at the satellite communication terminal.

The block diagram of the test setup is shown in Fig. 18. First, we generate a data enriched RF stream, originating from a typical user data stream from a computer feeding into a modulator through a typical router. We use an uncoded binary phase shift keying (BPSK) modulation onto a 70-MHz intermediate frequency (IF) carrier at a modulation rate of 1544 kbps (T1). Then, the signal is injected into a two-stage (630 MHz and tunable 7.2 GHz to 7.7 GHz) frequency up-converter. The first stage heterodyne mixer produced 700 MHz RF, while the second stage produced tunable X-band RF (from 7.9 GHz to 8.4 GHz). For our test, we selected the center frequency to be 8.326 GHz.

The modulated X-band RF signal is amplified and radiated towards a satellite with a circular polarization and ef-

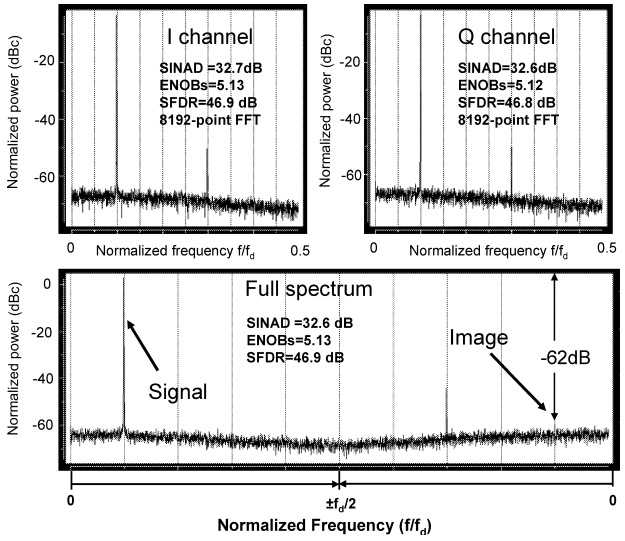


Fig. 19 The X-band ADR system test. The spectra of the I-channel output (top left), the Q-channel output (top right) along with the full 8192-point spectrum (I+jQ, bottom) acquired at 10.24 GHz. The input tone frequency is 7676 MHz. The LO is 2560 MHz to mix with signal alias at 2564 MHz (IF is 4 MHz). The output bandwidth ($f_d = f_{clk}/256$) is 40 MHz.

fective antenna gain of 57 dB. The loss to the satellite, approximately 22,380 miles away, is 202 dB. On the satellite, the signal is amplified, frequency shifted down by 650 MHz (7.25 to 7.75 GHz), circular polarized, and amplified again for a transmission back to earth. After another 202 dB of loss, the RF signal is collected by the 57 dB gain aperture similar to that it was transmitted except its lower frequency and opposite polarization. Upon arrival, the signal is amplified by a 73 dB LNA integrated behind the dish. The signal then traversed more waveguide to a bank of RF splitters and a set of fixed and variable attenuators before being applied to the X-band digital-RF receiver. For our chosen carrier, the input RF signal is $f_0 = 7676$ MHz.

Our cryocooled XADR chip sampled this 7.676 GHz RF input directly with an applied $f_{clk} = 4f_0/3 = 10.234667$ GHz, and digitally down converted down to baseband. The decimation ratio of digital filter is 256, and consequently, the output decimated clock rate was $f_d = f_{clk}/256 = 39.98$ MHz. The output digital I and Q data at 39.98 Msample/s are amplified, passed through the FPGA data acquisition board, and sent to the L-3 digital modem. Upon demodulation, the signal was passed through the router in its packet form to be acquired and displayed by a computer. We also acquired the data from the data acquisition and processing board and performed FFT for display on our graphical user interface (GUI). Figure 19 shows the performance of the XADR chip in terms of SNR and SFDR over the 40 MHz band with a single-tone RF input signal.

In addition to testing with pseudo-random patterns, we demonstrated the XADR system with live transmission and reception of a video file (Fig. 20). The spectrum shows the digitally down-converted signal-of-interest on either side of $f = 0$. During this demonstration, there were other com-

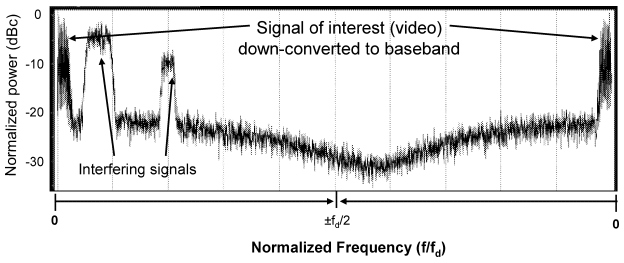


Fig. 20 The X-band ADR system operation. The measured spectrum of the received satellite signal-of-interest with input 7676 MHz signal modulated at 1.544 Mbps with a packetized video file. Our wideband XADR receiver also captured other signals in the same transmitted band, at 7679 MHz and 7684 MHz. The clock frequency is ∼10.235 GHz.

munication signals present in the same band. The closest in frequency was a transmission centered at 7679 MHz with 10 dB more power than our signal-of-interest. These signals were also digitized by the XADR chip, and could be extracted from the same digitized data using a set of second-level channelizers [2]. In other words, our Digital-RF receiver permits extraction of multiple sub-bands from a broad digitized band.

It is worth noting that the level of noise received from the antenna was significantly higher (by about 20 dB) than the ADC quantization noise floor. We estimated the total losses between the receiver LNA and the RF input port of the cryopackage unit to be 70–72 dB. Therefore, we expect that this XADR system could be placed directly behind the antenna, eliminating the need for amplification.

7. Conclusions

We have developed and demonstrated complete digital receiver prototype systems, implementing Digital-RF architecture capable of directly digitizing wide-band RF signals from kHz to GHz. The heart of these systems is a low temperature superconductor integrated circuit chip (ADR), consisting of either low-pass or band-pass ADC modulator and digital channelizer processors. These ADR systems have been assembled following the hybrid-technology-hybrid-temperature (ht^2) system integration approach. We integrated digital receiver LTS chips with commercial 4 K cryocoolers and equipped them with room-temperature interface electronics controlled by GUI.

The HF/L-band ADR has been operating above 24 GHz both in HYPRES and customer facilities by HYPRES and customers. The X-band ADR has demonstrated live operation with XTAR satellite while integrated with a 3rd-party equipment (modem) and successfully passing data and video. This demonstrates a relative maturity of superconductor Digital-RF technology.

These Digital-RF receiver demonstrations are just initial steps toward an All-Digital-RF Transceiver (ADT) for future communications systems. The overall goal of the ADT is a true software-defined radio [19]–[21], which will provide direct RF digitization of the whole bandwidth for all

incoming signal carriers from the antenna and consolidate all digital-RF distributions from the antenna into a single all-digital software-defined platform from RF to baseband. In terms of increased capability, this will allow us to have programmable and flexible multi-band multi-mode communications across multiple RF sources simultaneously. In terms of increased performance, this will allows us to have greater gain over noise temperature improvement on the receive-side and greater power efficiency on the transmit side, due to the intrinsic low noise temperature and direct digital-RF processing using superconducting digital circuits. In terms of acquisition and logistics cost, this will eliminate significant amount of legacy equipment, such as, IF cablings, analog RF switch panels, analog IF up/down converters, and analog IF modems.

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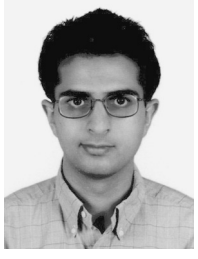

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