RAPID SINGLE FLUX QUANTUM (RSFQ) SHIFT REGISTER FAMILY

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Abstract--This paper presents the design and test results for a novel, buffered RSFQ shift register. The shift register is relatively insensitive to clock/data skew. The test results of buffered and of two-junction cell shift registers with different lengths (from 4 to 256 bits) and configurations indicate proper operation with wide margins (up to ±30% for a 32-b register) and high speed (up to 60 GHz for a 4-b register).[+]

I. INTRODUCTION

Impressive results have previously been achieved with superconductive shift registers (SR) based on latching edge-triggered logic [1] as well as non-latching quantum flux parametron (QFP) logic [2]. However, higher speed operation for shift registers of practical length is limited in these two approaches by problems associated with delivering and distributing external clock power on a superconducting chip.

The RSFQ logic family uses, for the clock, single flux quantum (SFQ) pulses easily generated on-chip. These pulses are distributed and processed by a Josephson junction network similar to the digital circuit being clocked.

The first RSFQ shift registers were proposed in 1987 [3] as an array of reset-set flip-flops (RS f-f). A separate Josephson transmission line (JTL) carries clock SFQ pulses in a direction opposite to the data stream. This design was extended with an additional clock JTL to build a reversible shift register. The merging of a clock distributing JTL and of RS flip-flops into one circuit has allowed a junction-efficient shift register design - with only two junctions per bit (2-JJ design) [4].

Both of these designs require a constraint on the delay of a traveling clock pulse t_c and on the delay of a data shift t_s. The clock delay t_c must be negative (i.e. clock and data travel in opposite directions), and longer than t_s: $-t_c > t_s$. Otherwise racing problems can appear.

In some applications, such as the circular shift register discussed later, both clock and data must have the same directions as well [5].

The purpose of this paper is to present: a) a new design of a buffered RSFQ shift register suitable for circular applications; b) the results of the experimental implementation of buffered and of 2-JJ shift registers.

II. DESIGN AND LAYOUT

A. Buffered Shift Register Cell Design

Three register cells are shown in Fig.1. The first one is the data input cell; the others are regular cells. Each cell consists of storage and buffer interferometers (e.g. JM2, LR2, JR2 and JR1, LM2, JM2, respectively). A clock distributing network, separate from the shift register, consists of an array of SFQ pulse splitters (JC1, LB1, LC2, JC2, LC3,...). Note that a merged clock network is also possible by eliminating junctions JC1 - JC3. The pair of junctions with critical currents JR2 > JB2 serves as a threshold detector. When a clock pulse comes, JR2 or JB2 will respectively undergo a 2-π phase leap in the presence (JR2) or absence (JB2) of a data SFQ in the storage loop. As a result, a data SFQ is released to a buffer stage of the next cell. If the next storage loop is empty, a data SFQ will enter the loop causing a 2-π phase leap across JM3. If it is not empty, a persistent current circulating in the storage loop will decrease the bias current of JM3 by superimposing a dc current from source IB4. In that case, a data SFQ will be trapped in the buffer stage until the next storage is empty and the circulating current has completely vanished.

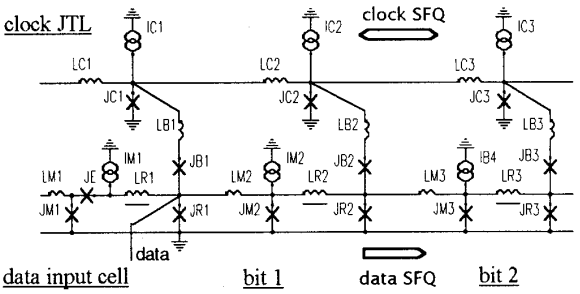

Fig.1 Schematic of a buffered shift register design. Total number of junctions per bit - 4. Underlined inductor designates a storage interferometer.

The introduction of a buffer stage allows us to virtually eliminate any constraint on t_s and t_c in the case of opposite data/clock direction. Furthermore, t_c can be positive, i.e. clock and data can travel in the same directions. In this case, we have to fulfill the condition $t_c < t_s$ which is relatively easy to achieve since a buffer stage delay contributes to t_s.

Fig.1 shows also the data input cell capable of accepting both external data - similar to a timed dc/SFQ converter [6] -

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and SFQ data from another RSFQ cell (e.g., from the last shift register cell). The non-reciprocal buffer (JE, JM1) prevents the propagation of data in the opposite direction.

Extensive simulations and optimization have been conducted to achieve margins of critical currents at least ±28% and margin of dc bias current of approximately ±31%. A margin of a parameter is defined as the range over which it yields proper circuit operation when all the other parameters are set at the midpoint of their margin range.

B. Shift Register Design and Layout

Unidirectional shift register circuits (Fig.2a) with both types of cells (2-JJ and buffered) have been designed. A modified version of a standard dc/SFQ converter (see e.g. [6]) generates SFQ clock pulses by an external trigger signal. Alternatively, when the applied dc input current exceeds a critical value, a pulse train is generated. In the triggered regime, the dc/SFQ converter is capable of generating one or two SFQ pulses per clock trigger period depending on its offset and amplitude. For the data input cell, a simple timed dc/SFQ converter is used. An output data SFQ goes through a short JTL to a standard toggle flip-flop (T f-f) with a SFQ/dc converter (see e.g. [6]) to provide direct observation of the output data. In some cases the T f-f with SFQ/dc converter or just the SFQ/dc converter are attached to the intermediate bits to control shift operation.

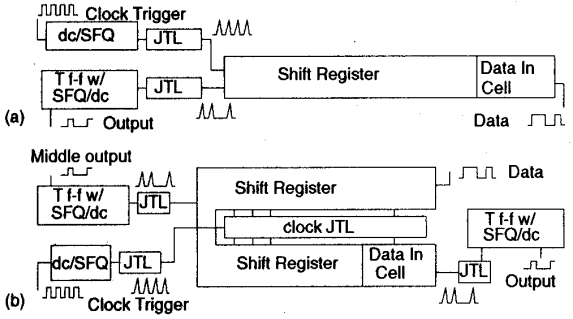

Fig.2 Block diagrams of experimental shift register circuits. (a) unidirectional. (b) open circular.

Fig. 2b shows a block diagram of an open circular shift register circuit. It consists of two connected buffered shift registers surrounding one clock JTL - an array of pulse splitters feeding both upper and bottom shift registers. Each clock SFQ pulse traveling from left to right causes a shift by one bit in both shift registers: in an opposite direction in the upper register and in the same direction in the bottom one. Such design eliminates the problem of data/clock skew in the case of closed circular registers [5]. For the data input cell, a timed dc/SFQ converter with the buffer is used (see Fig. 1).

The shift registers have been implemented using a standard HYPRES 10-level all-niobium process with 3.75 x 3.75 μm^2 minimum junction size, j_c = 1.0 and 1.3 kA/cm^2.

A typical layout of a 2-JJ shift register is shown in Fig. 3a. The design of a 2-JJ cell (see Fig. 5a [4]) is improved by adding a shunt resistor to the upper inductor. The cell occupies an area of 29 x 75 μm^2 without dc bias resistors. The power dissipation is ~ 1 μW/bit. To make the shift register layout more compact, a left and a right corner cell have been laid out with circuit parameters identical to a regular cell (Fig. 3a). Initially, the dc biases of all the odd bits and of all the even bits are wired separately to simplify testing. In later iterations, all dc biases are wired together and one resistor per two bits is used to conserve area.

A fragment of a circular shift register layout is shown in Fig. 3b. The area of a 2-bit cell consisting of two single bit cells of bottom and upper registers with clock JTL stages is 61 x 177 μm^2. The power dissipation is ~ 3 μW/bit. A clock JTL occupies the center. The dc biases for the clock JTL and for both shift registers are independent to simplify testing.

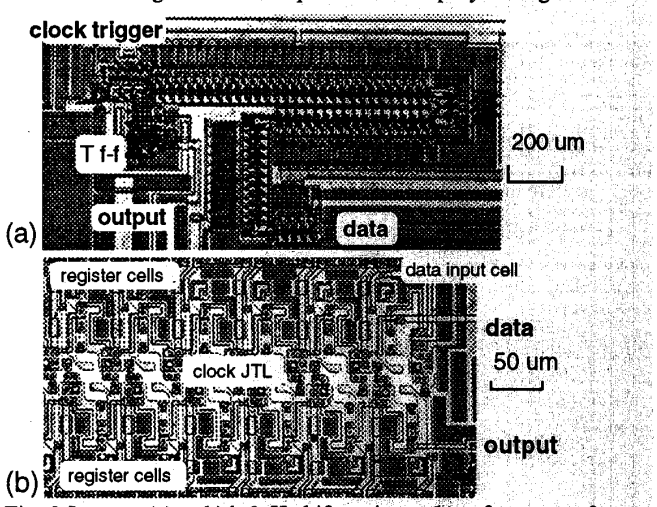

Fig. 3 Layout. (a) a 64-b 2-JJ shift register. (b) a fragment of circular buffered shift register.

All shift registers are implemented within a standard 24-pad chip. The data and the clock trigger signals are introduced through a 40 Ω resistor and a 10 Ω microstrip line (MSL) with a 10 Ω termination, or with a 3:1 resistive attenuator, respectively. The output line is a 22 Ω MSL with a 40 Ω shunt resistor to match a 50 Ω output cable. The dc biases of each functional block are separate to allow independent measurement of their margins. The clock generator and the output of the shift register have wires to monitor the dc voltages. The dense ground plane hole design is used to protect the circuit from flux trapping.

III. LOW-SPEED TESTING

Starting with a very low (~50 kHz) frequency for the external clock trigger, we verify the operation of the designed shift registers by observing the intermediate or/and the last bit outputs shifted by a number of clock periods corresponding to the register length. As an example, proper operation of a 256-bit 2-JJ shift register is shown in Fig. 4 with the responses of both types of output devices mentioned above. The 32-nd bit has the SFQ/dc converter attached directly to its storage loop while the 256-th bit is connected to the T f-f with its SFQ/dc

converter. Fig. 5 shows the test results of an open circular 64-bit (32 x 2) buffered shift register. The responses of the T f-f's connected with the 32-nd and 64-th bits confirms, in one measurement, proper shift operation for data and clock SFQ pulses going in: 1) opposite directions (upper 32-b SR); 2) the same direction (bottom 32-b SR).

Table 1 presents the results of the margin measurements at a clock frequency ~50 GHz in the terms mentioned above and determined by a relatively low error rate. The output T f-f with dc/SFQ converter is ideally suited for the detection of single errors since it changes its state with every SFQ pulse.

Table 1. Measured margins for shift registers

Circuit	Parameter	Margin	Comments
2-JJ Cell	*dc biases of*		
32-bit	odd bits	±49%	j_c=1kA/cm^2
	even bits	±68%	
64-bit	odd bits	±30%	j_c=1kA/cm^2
	even bits	±31%	
256-bit	odd+even bits	±6%	j_c=1kA/cm^2
Buffered	*dc biases of*		
64-bit	clock JTL	±30%	
(2x32)	bottom SR	±21%	j_c=1kA/cm^2
circular	upper SR	±15%	
32-bit	clock JTL	±19%	j_c=1.3
opposite	cell array	±18%	kA/cm^2
I/O block			
dc/SFQ	dc bias	±24%	
converter	clock trigger	±65%	single clock
	amplitude	±12%	double clock
T f-f w/ SFQ/dc	dc bias	±17%	V_{out}=80 to 350 μV
data input cell	input current	±27%	w/o buffer
		±51%	w/ buffer

The error rate is considered low if we cannot visually detect any errors in a reasonable amount of time at the margin midpoint. At the margin limits, the error rate can be roughly estimated as ~10^{-5} error/clock period (one error per second at 50 kHz). Except for obvious length dependence, the margin measurements have shown a significant variation with the conditions of the dc bias filtering, the flux trapping, and the particular fabrication run. The particular design of the circuit environment (e.g., the ground plane holes) also contributes to the margin width.

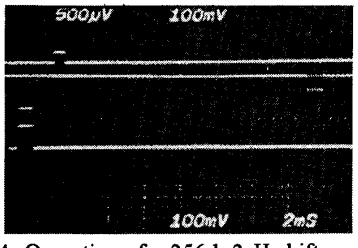

Fig. 4 Operation of a 256-b 2-JJ shift register. Two levels of the data represents an input margin.

Approaching a ~ 2 GHz clock trigger frequency - the limit of the synchronous regime of our test set-up - we verify the operation of the shift registers using the capability of our dc/SFQ converter to double the clock frequency in comparison with the trigger clock frequency (Fig. 6). The time shift between the output envelopes at the single and the double speed should correspond to half of the shift register delay at the given clock trigger frequency.

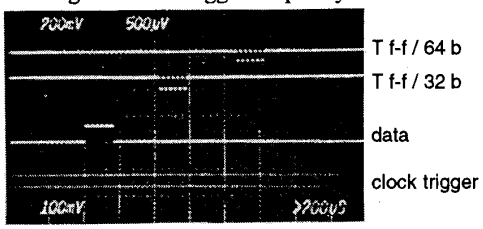

Fig. 5 Operation of a 64-b (32 x 2) open circular buffered shift register.

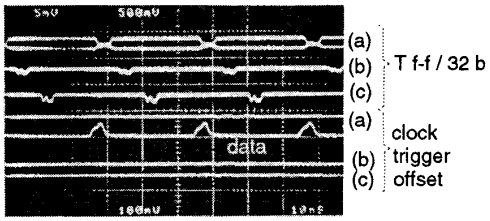

Fig. 6 Operation of a 32-b 2-JJ shift register at clock trigger frequency 2.113 GHz with the offset of clock trigger. (a) 6.9 mA (clock pulse train generation). (b) 1.5 mA (a double clock - 4.226 GHz). (c) 0 mA (single clock - 2.113 GHz). The data is 11110011.

IV. HIGH-SPEED TESTING

A. Triggered Clock.

Starting with ~ 2 GHz for the external clock trigger, we conduct testing in an asynchronous mode within the data signal bandwidth of 2 GHz. In this mode, the output T f-f is in two possible states when no data arrive from the shift register - the double traces in Fig. 7. While the data pulses are switching the T f-f, these traces merge together into a single trace located at the average voltage. Because the test is asynchronous, we cannot detect error rates below ~ $5 \cdot 10^{-2}$.

Our test procedure utilizes the clock doubling feature of the dc/SFQ converter described above. Fig. 7 shows the test results of the 256-b 2-JJ shift register at the 6.18 GHz of the clock trigger. Gradually increasing the clock trigger offset up to a certain value (~ 1.9 mA), we observe a distinct leap of the output envelope to a new position by half of the shift register delay: 6.18 GHz^{-1}· 1/2 · (256 bits) = 20.7 ns, corresponding to an operation at the double frequency 12.36 GHz. The next trace corresponds a leap to the position when the dc/SFQ converter generates the clock pulse train. Similar testing for a 2-JJ 32-b shift register results in proper operation at a 31.8 GHz of the clock frequency (a double clock trigger frequency).

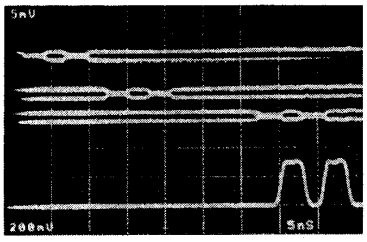

Fig. 7. Triggered clock test of a 256-b shift register with the clock trigger offset. (a) >2.4 mA (clock pulse train generation). (b). 2.0 - 2.1 mA (12.36 GHz). (c) 0-1.9 mA (6.18 GHz). Data pattern is 11100111 at 885 MHz.

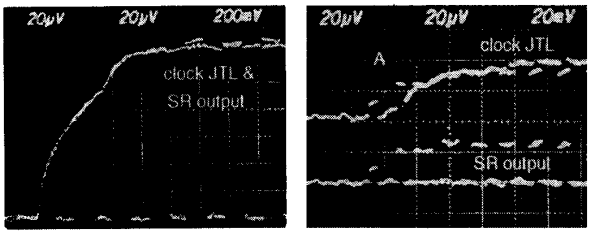

Fig. 8. Non-triggered clock test. Vertical scale 9.7 GHz/div. (frequency = voltage/(h/2e)). Horiz. scale: (a) a 4-b SR, 50 μA/div. (b) a 256-b SR, 20 μA/div.

B. Non-Triggered Clock.

Applying a ~ 1-200 Hz triangle wave (sweep) current to the input of the dc/SFQ converter - the generator of the clock pulse train, we monitor the dc voltages on the clock JTL and on the output of the shift register. The data signal frequency is adjusted to observe few data envelopes in a sweep period. All dc biases and the data signal are within their ranges known from low-speed testing. Fig. 8a shows the test results of a 4-b buffered shift register. In the range of proper operation, the output voltage is the same as the voltage on the clock JTL when the data is "1". The output voltage is zero when the data is "0". Beyond ~ 124 μV (or ~ 60 GHz according the voltage-to-frequency ratio), the output voltage cannot follow the clock voltage. Similar tests have been conducted for other shift registers excluding the case of the buffered shift registers with the clock and data traveling in the same direction. The highest operating frequencies within an accuracy of ±5% are: a 2-JJ cell design (j_c=1 kA/cm^2): 30 GHz (32-b), 22 GHz (64-b), 12 GHz (256-b); a buffered design (j_c=1.3 kA/cm^2): 60 GHz (4-b), 44 GHz (32-b); a buffered design (j_c=1 kA/cm^2): 17 GHz (64-b). An accuracy of the error rate detection being inferred from the voltage measurement accuracy is ~ 10^{-1}. These experimental speeds are lower than the simulated frequency margin of 75 GHz. This can be due to: 1) the upper frequency of the dc/SFQ converter (~ 65 GHz), 2) the underbias of the shift register due to the small margins of some cells, 3) the resonance of the dc bias lines.

The observation of the voltage on the clock JTL, while the ac data signal is applied allows us to distinguish between the proper shift operation and its action similar to a transmission line. In that case, the data SFQ pulses traveling along the shift register feed back the clock JTL by the extra pulses and inevitably change its measured voltage in contrast with the voltage when the data applied is zero. Fig. 8b shows a detection of such a regime (region A) for a 256-b shift register when the data signal is twice as large as its upper margin limit. This technique is not applicable for the buffered shift registers with the data and clock traveling in the same direction.

V. CONCLUSION

A proposed novel buffered register design allows us to build a circular 64-b shift register which is insensitive to the clock pulse direction within the experimentally measured dc bias margin of ±15%. The implementation of a large variety of unidirectional shift registers using either a buffered or a 2-JJ cell design confirms an expected wide dc bias margin ±30% (for 32-b) and high speed up to 60 GHz (for a 4-b). Among these circuits, is a 256-b shift register. To our knowledge, this is the largest RSFQ circuit (533 junctions) reported to date. This shift register was tested to have a dc bias margin of ±6% and proper high speed operation up to 12 GHz.

The problem of the relatively fast margin narrowing with increasing complexity has still to be solved. A more adequate high speed test providing a more accurate estimation of the error rate needs to be used. Such a test could be the fast acquisition of a known high speed signal into a unidirectional shift register or the circulation of a certain pattern in a circular shift register with low-speed read-out.

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