Josephson Output Interfaces for RSFQ Circuits

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Abstract—**We have developed and demonstrated high bandwidth Josephson circuits to interface the output of RSFQ circuits to room temperature electronics. Asynchronous dc powered voltage driver circuits have been designed to amplify RSFQ signal levels to voltage outputs in the 2-4 mV range, in a wide bandwidth. These driver circuits have been characterized and tested for data rates up to 8 Gb/s. The bit error rate for one of these drivers has been measured up to 7 Gb/s for a (2^{31} -1) bit long pseudo-random bit sequence (PRBS). In order to match the data rate of Josephson circuits to slower room temperature electronics, we have developed clock-controlled shift registers which allow shift-in and shift-out of data at different frequencies. Complete functionality of these circuits integrated with the drivers has been demonstrated at low speed. Shift registers integrated with the voltage driver circuits have been tested at high-speed for data rates up to 6 Gb/s.**

I. INTRODUCTION

As the Internet expands and bandwidth requirements of local area networks increase, fiber optic communication standards continue to be pushed to higher frequencies [1], [2]. Josephson RSFQ electronics can best utilize the available bandwidth of fiber-optic communications. Although RSFQ circuits are capable of internal operation at tens of gigahertz their application is limited by the output drive capability. For data communication applications which require high-speed outputs such as switches and transmitters, the usable bandwidth of the RSFQ circuit is limited by the output interface. The RSFQ signal must be amplified on chip at low temperature to a large enough level to be sensed by a low-noise wideband semiconductor amplifier with a low error rate. Once amplified, the signal can be used, for example, to drive a laser diode or optical modulator for fiber-optic communication links.

Large communication switches and network systems need high-throughput serial buffers to handle data overflow. Josephson clock-controlled shift register circuits can offer flexible and efficient ways of dealing with high-speed data overflow. For example, a two-speed shift register enables shift in of overflow data at high speed, temporary storage, and shift out at lower speed to a slower large memory where the data can wait for retransmission. For the retransmission process, the data is uploaded into the shift register at low speed and shifted out at high speed. For processing applications, these clock-controlled shift registers can be similarly used as a buffer interface between a fast superconducting processor and a slower room temperature computer or memory.

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II. DESIGN OF ASYNCHRONOUS VOLTAGE DRIVERS

There have been a number of driver circuits used and proposed for high-speed and high-voltage output interfaces of RSFQ circuits. An ac-driven SFQ-to-latch converter capable of operating at 3 GHz was proposed in [3]. However, the integration of dc-driven RSFQ circuits and ac-driven output drivers is prone to the problems associated with the ac-current-induced crosstalks and a ground ripple. In contrast, the dc-driven HUFFLEs are free of these crosstalk problems. However, they are limited to operation below 4 GHz [4] and are prone to entering parasitic "hang-up" mode, which cannot be reset without switching the dc power off.

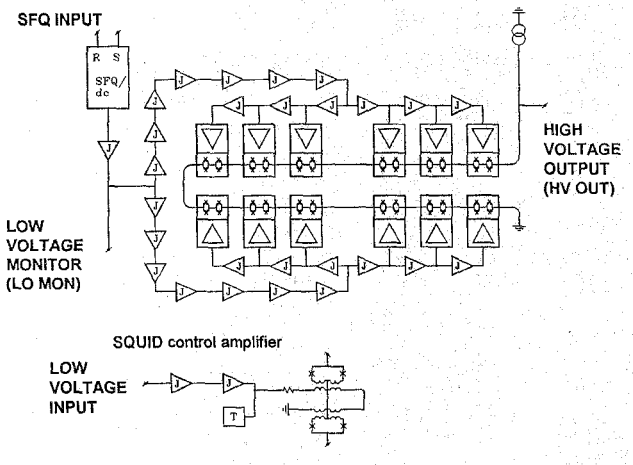


Fig. 1. Block diagram of the dc-driven, high-speed, high-voltage RSFQ driver. Small amplifier sections marked "J" are two-junction JTL stages. A box marked "T" is an underbiased two-junction JTL stage used for termination purposes.

The driver developed here is a high-speed modification of a dc-driven high-voltage driver described in [5]. It consists of a low-voltage, low output impedance SFQ/dc converter, a Josephson transmission line (JTL) current amplifier, and a stack of dc SQUIDs. The design of the JTL amplifier was fine-tuned for maximum speed, while other elements of the driver were adopted from the driver described in [5]. Fig. 1 shows the driver block diagram. The low-voltage, low-impedance SFQ/DC converter with set (S)

and reset (R) SFQ inputs generates low-voltage output signal applied to 12 SQUID control amplifiers. Each amplifier channel controls two symmetric two-junction SQUIDs. All 24 output SQUIDs are connected in series and biased with dc current.

The circuits are implemented using HYPRES' standard 10 level Nb process with critical current densities of 1 kA/cm^2 and 2.5 kA/cm^2 [6]. Fig. 2 shows the driver layout. Most of the area of the driver is consumed by the JTL amplifier having 12 independent current outputs. The parallel control scheme allows a dramatic increase in speed compared to the serial control used in [5] at the expense of increased area.

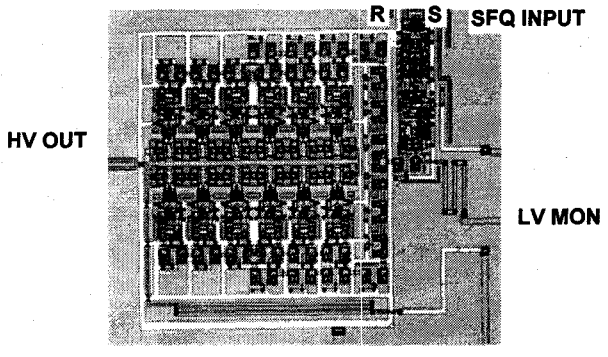
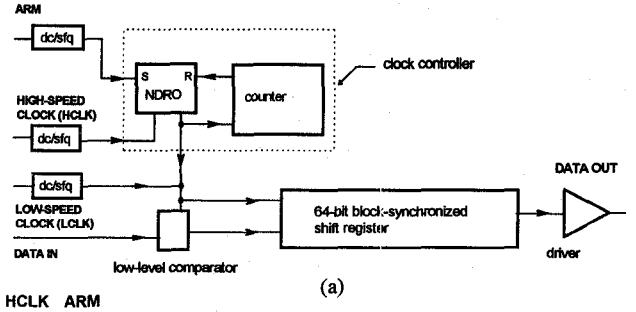
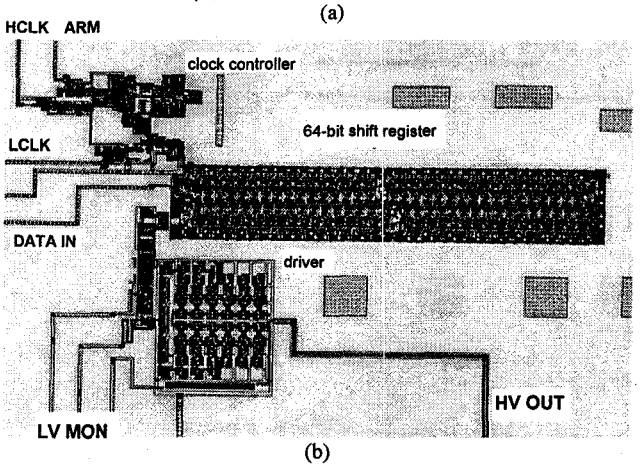


Fig. 2. Layout of 2.5 kA/cm^2 dc-powered high-speed high-voltage RSFQ driver. The circuit contains 184 Josephson junctions and occupies 0.6x0.65 mm^2. The low-voltage, low-impedance SFQ/DC converter with RS flip-flop is located at the top right. The circuit has low-voltage monitor and high-voltage output (LV MON and HV OUT, respectively).



(a)



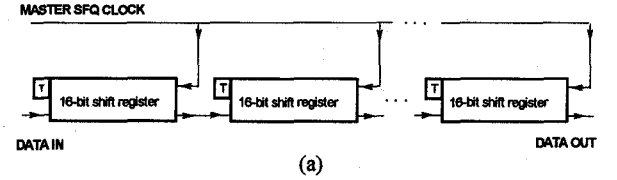
(b)

Fig. 3. High throughput serial buffer based on a clock-controlled, block-synchronized shift register integrated with a high voltage output driver. (a) Block diagram. (b) Layout.

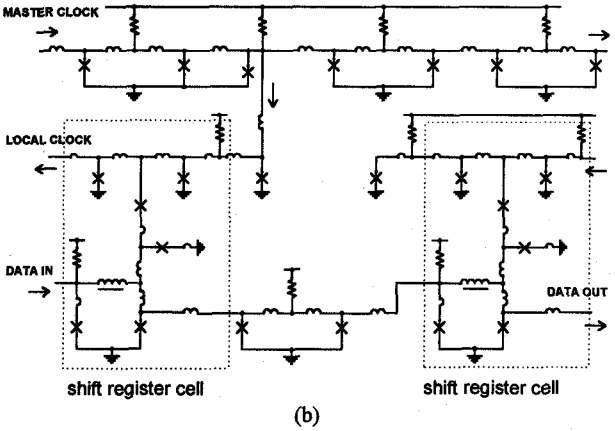
III. DESIGN OF CLOCK-CONTROLLED SHIFT REGISTERS

The RSFQ shift registers have been already used for the implementation of high throughput serial buffers (acquisition memories) [7]. Although these acquisition shift registers successfully demonstrated required operation, a fast shift-in up to 18 GHz and a slow shift-out, their dual timing was implemented using a quite cumbersome external test setup which is not practical in real systems. We have developed a new high throughput serial buffer based on a novel on-chip clock controller and a new block-synchronized design of RSFQ shift registers.

Fig. 3 shows block diagram and layout of our experimental circuit of a high throughput 64-bit buffer. Asynchronous input data are picked up by a low-level receiving latch, then converted into an SFQ form, and applied to the shift register input. Output SFQ data is unloaded to the output high-voltage driver to be converted into voltage mode and amplified. The dc/SFQ converters are used to generate switchable low- and high-speed SFQ clocks. The low-speed clock is set by an external generator providing exactly 64 clock cycles. The high-speed clock is a continuous sinewave converted on chip into an SFQ pulse train. After initialization by the trigger signal (ARM), the clock controller selects 64 high speed clock pulses for timing of the shift register.



(a)



(b)

Fig. 4. Block-synchronized shift register. (a) Block diagram. The design is a combination of two clocking schemes: a concurrent flow for an entire shift register and a counter flow for each 16-bit block. A box marked "T" is an underbiased JTL stage used for termination purposes. (b) Schematics of interblock section of a block-synchronized shift register.

A. Block-Synchronized Shift Registers

For many applications, it is preferable to use concurrent-flow timing when clock and data propagate in the same direction along a digital circuit [8]. However, RSFQ shift registers were found to exhibit larger margins when they

employ a counter-flow timing scheme [9]. In order to maintain a high margin, we have developed a new shift register with block synchronization using an approach similar to that used in [10]. Fig. 4a shows the block diagram of this shift register. Concurrent flow timing is used for an entire shift register which is subdivided onto a number of 16-bit shift register blocks. Each block uses a counter-flow timing scheme. A master SFQ clock is distributed along the shift register with a JTL and SFQ splitters to broadcast SFQ clock pulses to each block.

Fig. 4b shows schematics of the interblock section of the circuit. The design of the shift register is based on the new six-junction cell design for counter-flow clocking. Its simulated margins exceed ±40% for dc bias and ±30% for critical current density. The 48-bit circuits made of these cells demonstrated wide measured margins exceeding ±30% and substantial endurance to operate under moderate flux trapping levels [11].

B. Clock Controller

The high speed SFQ clock is generated by a continuous sinewave. The function of a clock controller is to control the flow of high-speed clock SFQ pulses. The circuit is based on an RSFQ RS flip-flop with a non-destructive readout (NDRO switch). The ARM pulse writes "1" into the RS flip-flop. The CARRY pulse from the counter resets the flip-flop. The high-speed clock is applied to NDRO input. It reads out "1" when the RS flip-flip is set, and "0" when it is reset. The NDRO output is connected to the clock input of the shift register.

The function of the counter is to keep the NDRO switch open for 64 clock pulses. A carry from the last bit resets NDRO switch to OFF. We use both latched and non-latched designs of a counter. The latched design (in Fig. 5) is employed in order to eliminate a carry propagation delay. The CARRY output is generated with the regular one-stage delay of the last latch. An extra initial 6-cycle set up delay will be observed, then the required 64-cycle delay will be established. This circuit is similar to one described in [12], [13].

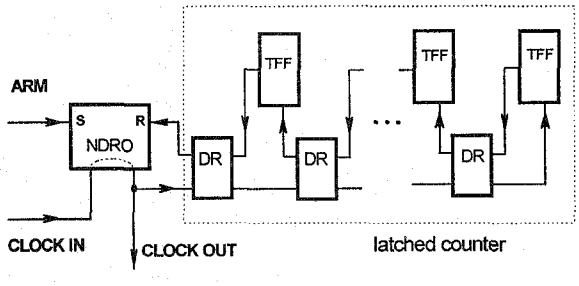


Fig. 5. Clock controller based on latched counter. A carry of each counter bit is synchronized using a latch DR.

IV. TESTING OF ASYNCHRONOUS VOLTAGE DRIVERS

The measurements reported here are of an optimized driver circuit with 24 SQUIDs in the output array coupled to 12 branches of the JTL current amplifier. The test circuit consisted of a two phase dc/SFQ converter at the input, connected to an RS flip-flop which was integrated with the driver. Thus the circuit could be used to amplify NRZ signals, which is desirable for PRBS measurements. Driver circuits with current densities of 1 kA/cm^2 and 2.5 kA/cm^2 were tested.

A. Low Speed Test

For data rate of 50 Mb/s, the 1 kA/cm^2 driver circuit operated with output voltage amplitude of 3 mV into a 50 Ω load. The dc bias margins for the 1kA/cm^2 circuit were ±14% for the JTL amplifier bias and ± 15% for the output array bias, for output amplitude greater than 2 mV. The main dc bias is the current required for the JTL amplifier, which is about 40 mA. The output array requires only 300 μA. The 2.5 kA/cm^2 driver circuit demonstrated a 4 mV output amplitude into a 50 Ω load. The dc bias margins for the 2.5 kA/cm^2 circuit were ± 18% for the JTL amplifier bias and ± 15% for the output array bias, for output amplitude greater than 3 mV. A maximum output of 4.8 mV was obtained for a test circuit of an analog amplifier, without the RS flip-flop (Fig. 6). We believe, this is the highest 50 Ω output achieved with a dc-powered Josephson device to date.

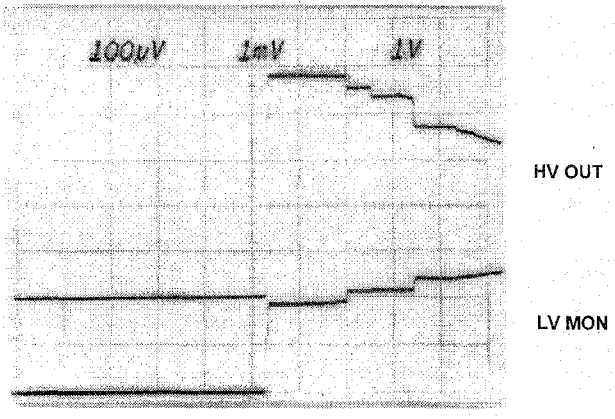


Fig. 6. Operation of the analog amplifier part of a high-voltage driver at 2.5 kA/cm^2. Low-voltage (100 μV/div) and high-voltage (1 mV/div) outputs of the amplifier are plotted as a function of its input current (1 mA/div). The high-voltage output is displayed at 50 Ω load. Note that an increase of the low-voltage signal beyond 200 μV leads to a decrease of the high-voltage output due to the periodic response of a SQUID to its control current.

B. High Speed Test

The high speed measurements were done using an HP 80000 data generator and a 10 Gb/s 4:1 multiplexer to obtain data patterns up to 10 Gb/s. The outputs were measured on a 50 GHz sampling oscilloscope. For PRBS measurement, which do not allow averaging, a low-noise wideband Anritsu amplifier A3HB3102 was used. The amplifier has a bandwidth of 30 kHz - 10 GHz, gain of 25 dB, noise figure of 4 dB, and gain variation less than ± 1.5 dB. A high-performance amplifier is necessary for doing high-speed PRBS measurements.

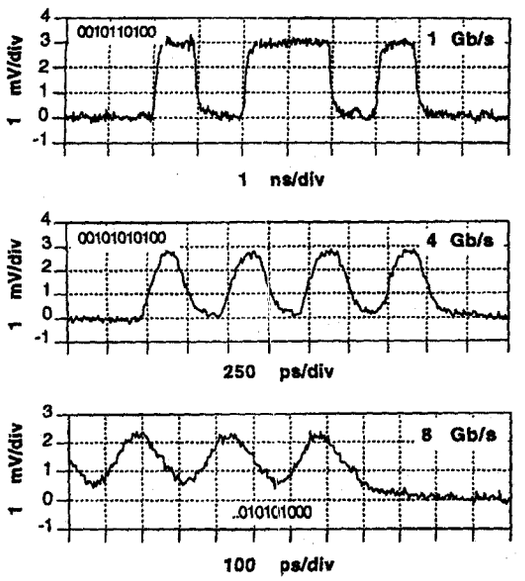


Fig. 7. Output of 2.5 kA/cm^2 asynchronous voltage driver circuit for 1 Gb/s, 4 Gb/s and 8 Gb/s input patterns. Traces include 16 averages of sampling oscilloscope.

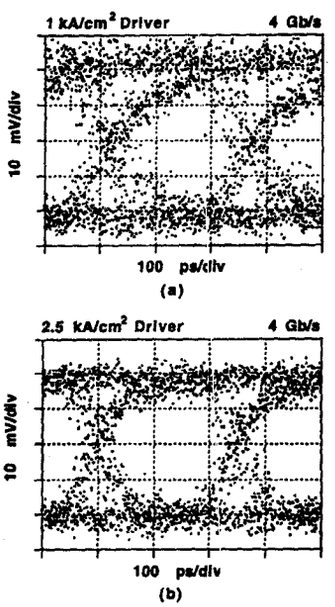


Fig. 8. Output eye diagram of (a) 1 kA/cm^2 and (b) 2.5 kA/cm^2 driver circuits for 4 Gb/s PRBS input, with 25 dB Anritsu amplifier and 3 sec. persistence time on HP54120B sampling oscilloscope.

The 2.5 kA/cm^2 driver circuit operated at high-speed up to 8 Gb/s, with rise and fall times of about 100 ps. The outputs of the 2.5 kA/cm^2 driver circuit for input pulse patterns at 1Gb/s, 4 Gb/s and 8 Gb/s are shown in Fig. 7. Since no following amplifier was used for this measurement, some averaging was necessary to obtain clean signals, as the input noise of the sampling oscilloscope is about 1 mV. Each trace in Fig. 7 includes 16 averages. Note that the 3 mV output amplitude at 1 Gb/s is less than the 4 mV amplitude measured at low speed, and it continues to decrease with increasing frequency. A large part of the decreased output amplitude at higher frequency is due to increasing loss in the measurement probe. The probe attenuation increases by 1.7 dB between 0.1 GHz and 5 GHz.

Measurements without averaging were done using the Anritsu wideband amplifier. The output eye diagrams for a 4 Gb/s PRBS pattern input are shown in Fig. 8 for the 1 kA/cm^2 and the 2.5 kA/cm^2 driver circuits. The eye diagram is a persistence plot of a random bit sequence on a sampling oscilloscope. The performance of the circuit is gauged by the size of the eye opening, which will improve with larger SNR, smaller phase noise, and smaller rise and fall times. The eye opening represents the region, in voltage and time, of error-free operation. As seen in Fig. 4, the 2.5 kA/cm^2 circuit has a larger eye opening primarily due to faster rise and fall times, which are about 50% of the 1 kA/cm^2 circuit. The phase and voltage noise are also reduced for the 2.5 kA/cm^2 circuit.

C. Bit-Error Measurements at High-Speed

The bit-error-ratio (BER) measurements were done using the Hewlett Packard 12 Gb/s error detector and pattern generator test set HP71612A. Two of the Anritsu amplifiers described above were used between the driver output and the error detector input. The BER for these amplifiers was less than 10^{-12} for a 3 mV input at 10 Gb/s. The BER of the American Cryoprobe high-speed probe used for these measurements was less than 10^{-12} for a 100 mV input signal with no amplifiers at 10 Gb/s, measured through a 50 Ω superconducting transmission line on chip.

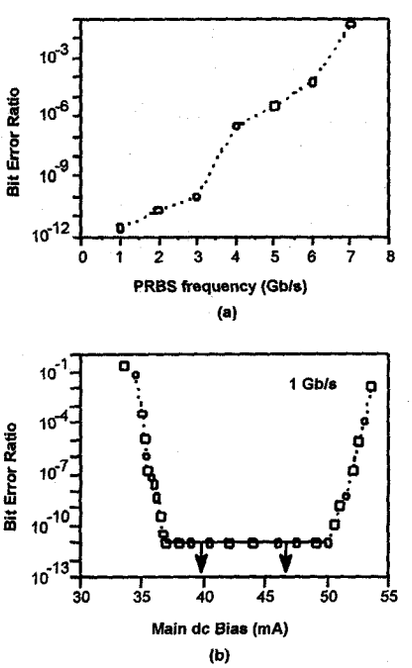


Fig. 9. BER measurement of 1 kA/cm^2 asynchronous voltage driver as a function of (a) PRBS frequency, and (b) main dc bias at 1 Gb/s. The 10^{-11} limit in (b) is due to limited measurement time.

The BER for the 1 kA/cm^2 driver circuit as a function of the PRBS frequency is plotted in Fig. 9a. The length of the PRBS pattern was $(2^{31} - 1)$ bits, and the test time for each data point was at least 100 seconds. The BER increases as a function of frequency from about 10^{-12} at 1 Gb/s to 10^{-2} at 7Gb/s. For 1 Gb/s PRBS frequency, the BER was measured as a function of the main dc bias to determine high-speed bias margins, as shown in Fig. 9b. The 1 Gb/s bias margin for BER < 10^{-11} is ± 15 %, which is the same as the low-speed bias margin.

The measured BER for the 2.5 kA/cm^2 driver was slightly worse than the 1 kA/cm^2 driver. We believe this is due to the very small bias margin for the RS flip-flop input circuit in this chip. This low margin is due to the lower fabrication yield for the 2.5 kA/cm^2 circuits. Higher current density circuits with good margins can be expected to have a better BER at high frequency than the 1 kA/cm^2 circuits.

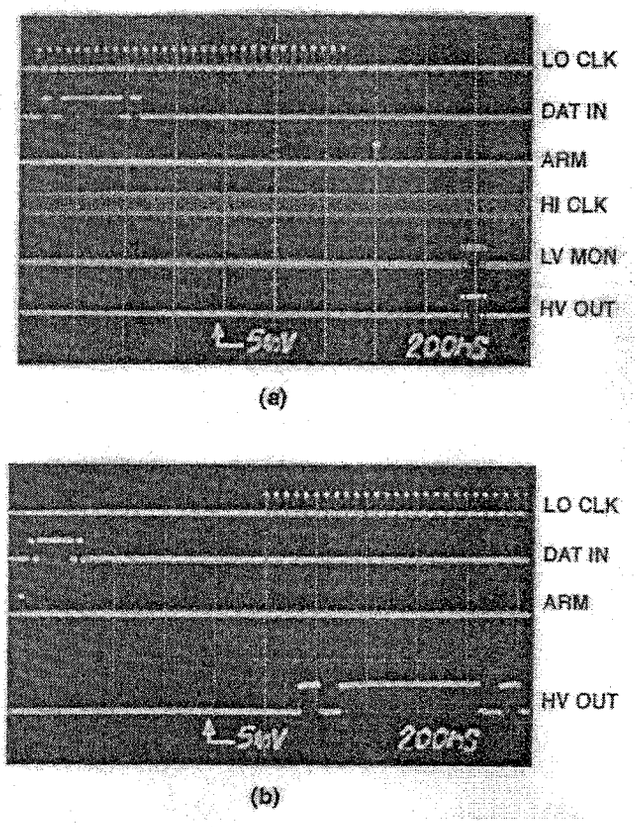


Fig. 10. Operation of a 1 kA/cm^2 clock-controlled shift register circuit integrated with the voltage driver, for (a) 25 MHz shift-in and 100 MHz shift-out and (b) 100 MHz shift-in and 25 MHz shift-out. Circuit contains a 64-bit shift register and a 6-bit clock controller. LV MON is a low-voltage monitor with a 25 dB external amplifier, and HV OUT is the direct high-voltage output of the driver.

V. TESTING OF CLOCK-CONTROLLED SHIFT REGISTERS

The circuits tested consist of a 32-bit or 64-bit shift register integrated with the clock controller circuit, and the asynchronous voltage driver. The clock controller circuit consists of a 5 or 6 bit unlatched counter coupled to an NDRO switch. When activated the n-bit clock controller will produce 2^n HI CLK pulses.

A. Low Speed Test

For the low speed tests a 25 MHz signal was used for the LO CLK and a 100 MHz signal was used for the HI CLK. Operation of a circuit with a 64-bit shift register and a 6-bit clock controller is shown in Fig. 10. For the measurement in Fig. 10a, a 1011111101 data pattern is shifted in at 25 MHz and shifted out at 100 MHz. A continuous sinusoidal signal is used for the HI CLK input. A single ARM pulse activates the clock-controller which sends 64 high frequency SFQ pulses to the shift register. For the second measurement, in Fig. 10b, the pattern is shifted in at the higher clock frequency and shifted out at the lower clock frequency. The dc bias margins of the circuit were ± 18% for shift register bias, ± 19% for clock-controller bias, and ± 17% for the driver main bias. The input margins for the clock, data and ARM signals were ± 35% to ± 45%. Six out of seven of these circuit tested worked with comparable margins.

B. High-Speed BER Test

For these high speed tests the data were shifted through a 64-bit shift register and amplified by the asynchronous voltage driver, on a 1 kA/cm^2 chip. The clock-controller section of the circuit was not used, as the BER test set did not have the capability of testing the full functionality of the circuit with different clock rates. The LO CLK input of the circuit was used for the clock, which is independent of the clock-controller and has the same bandwidth as the HI CLK input. The eye diagrams of the output for a 1 Gb/s, 3 Gb/s, and 5 Gb/s PRBS input pattern are shown in Fig. 11. Note that the shape of the eye opening becomes triangular at higher frequency, unlike the stand-alone driver which had a symmetric eye diagram. This is due to the reset or clock pulse to the RS flip-flop arriving just before the set or data pulse, so that the flip-flop will always be reset to the '0' state for a very short period of time between the valid data. This effect will not be seen at low speed since this time is very short.

The measured bit-error ratio of this shift register and driver circuit as a function of PRBS frequency is plotted in Fig. 12. The BER is less than 10^{-11} up to 4 Gb/s, which is the best we can expect from a 1 kA/cm^2 circuit. Most commercial data communication applications require bit error ratios less than 10^{-10}. Note that this BER performance is better than that of the stand-alone 1 kA/cm^2 driver in Fig. 9. This is probably due a better chip with larger high-speed margins, and less fabrication parameter variations. The amplifier and shift register circuit include about 700 Josephson junctions. We believe this is the best high-speed bit error rate measured for a complex Josephson circuit using a commercial communications error detector.

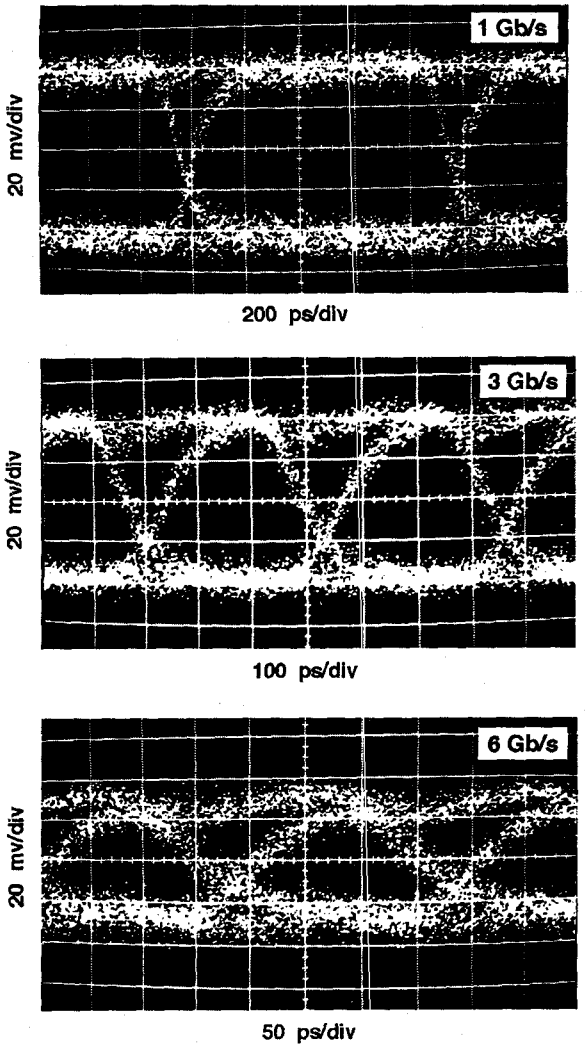


Fig. 11. Output eye diagram of 1 kA/cm^2 64-bit shift register integrated with voltage driver, for 1 Gb/s, 3 Gb/s, and 5 Gb/s PRBS at 3 sec. persistence time on HP54120B sampling oscilloscope.

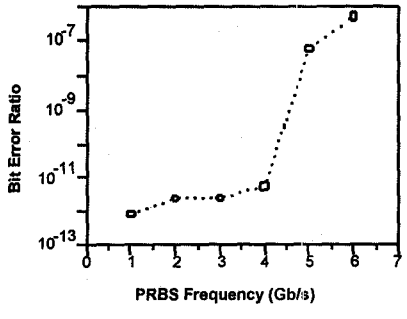


Fig. 12. Bit error ratio of 1 kA/cm^2 64-bit RSFQ shift register integrated with asynchronous voltage driver, as a function of PRBS frequency. Length of PRBS input pattern is (2^{31}-1) bits.

VI. Conclusion

The insertion of high-speed, low-power superconductive RSFQ circuits into high-performance communications systems requires the development of interface circuits capable of data inputs and outputs at GHz rates. We have developed a high-speed Josephson driver to amplify SFQ signals up to 2-4 mV at GHz rates. Our dc-driven driver design has been implemented and characterized up to 8 Gb/s. It demonstrated a 4.8 mV output into 50 Ω load at low speed and 2-3 mV at high speed. We believe, this is the highest 50 Ω output achieved with a dc-driven Josephson device to date.

To handle data overflow at the interfaces, we have developed high-throughput serial buffers based on clock-controlled RSFQ shift registers. They have been successfully characterized up to 6 Gb/s.

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