RSFQ Time Digitizing System

Alex F. Kirichenko, Saad Sarwana, Oleg A. Mukhanov, Igor V. Vernik,
Yongming Zhang, Joonhee Kang, and Johannes M. Vogt

Abstract—**We have developed a high-performance time digitizer system using a superconductor technology for high-energy and nuclear physics detector instrumentation, CMOS chip diagnostics, and military applications. The system consists of an 8-channel, RSFQ multi-hit Time-to-Digital Converter (TDC) integrated into a single system with a semiconductor VXI interface and control modules. The Digitizer operation and output digital data analysis are performed and fully controlled using custom PC-based LabVIEW™ software. This all-digital TDC contains eight 9-hit, 14-bit, 20-GHz TDC channels on a 1 cm x 1 cm chip. The TDC chip is capable of operation in Common Start and Common Stop modes. The VXI digitizer part comprises a 200 MS/s, 8-channel data receiver module, a TDC control module, and a commercial VXI-PCI link. The data receiver module converts data into ECL format. The TDC control module based on Xilinx CPLD technology sorts this data and also controls the superconductive RSFQ chip operation by producing all necessary control and readout signals. We present results of operation and experimental performance evaluation of this system**

Index Terms—**TDC, time-to-digital converter, Josephson junction, RSFQ, superconductor, VME/VXI.**

I. Introduction

THERE are a number of applications that require very high time resolution. Examples include time-of-flight (TOF) systems for nuclear and high-energy physics (HEP), ranging systems for military surveillance, and new emerging systems CMOS VLSI diagnostics. HEP instrumentation applications have so far been the most accepting to the necessity for cryocooling, including liquid He cooled systems. For now, our RSFQ time digitizing system is being developed primarily for such HEP TOF systems. This allows us to defer the cryocooling system aspect for now, and focus on the integration of the superconductor time-to-digital converter (TDC) chip with room-temperature electronics.

There are two key requirements for modern HEP systems. First, they require the absolute highest performance, in order to maximize the physics potential of their complex and costly experimental systems. Second, all interfacing and control functions have to be done using standard buses and computer control. Toward the first goal, we have been developing a high-resolution TDC capable of achieving a time resolution of a few ps, far beyond the capabilities of semiconductor electronics. In order to meet the second requirement, we have developed VXI-based interface and control modules with software control and data processing. In this paper, we describe the TDC chip design, the VXI interface and control modules, and the LabVIEW-based TDC control and processing of data. Results of initial system testing are presented.

Manuscript received September 19, 2000.

This work was supported in part by the U.S. Department of Energy under contracts DE-FG02-95ER81990 and DE-FG02-98ER82595.

J. M. Vogt was with HYPRES. He is now with Canadian Light Source, 107 North Road, Saskatoon, SKS7N5C6 Canada, e-mail: vogt@cls.usask.ca.

Y. M. Zhang is with Conductus, Inc., 969 W. Maude Ave., Sunnyvale, CA 94086, USA, e-mail: yongming@conductus.com.

All other authors are with HYPRES, Inc., 175 Clearbrook Rd., Elmsford, NY 10523, USA, e-mail: firstname.lastname@hypres.com.

II. Chip Design

A. Multi-Hit Digital 8-channel TDC

The basic design of our RSFQ time-to-digital converter is described in [1]. The design capitalizes on the ability of RSFQ binary counters to operate at very high clock frequencies. This allows us to perform a time digitization by the direct counting of high-speed clock pulses, making the TDC time resolution equal to one clock period.

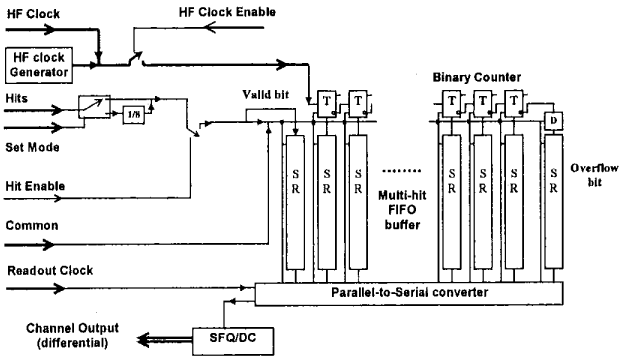

Fig. 1. Block diagram of a single channel of multi-hit TDC.

Fig. 1 shows a block diagram of a single channel the RSFQ multi-hit TDC. Each channel consists of a binary DRO counter, a first-in-first-out (FIFO) buffer, a parallel-to-serial converter (PSC), and a differential amplifier. Each TDC input (event) causes a destructive readout of the counter and a shift of the data stored in FIFO buffer by one word.

The novel design of the parallel-to-serial converter (see Fig. 2) allows the FIFO buffer to operate correctly, even in case of the data overflow. The PSC is based on B flip-flop cells [2]. When each parallel clock arrives, it resets the PSC prior to writing the data into the PSC register. Each cell of the PSC in Fig. 2c is connected to one shift-register of the FIFO buffer (Fig. 1). The shift register clock always precedes

the data to reset the content of the corresponding PSC cell before the data arrives at the "set" input.

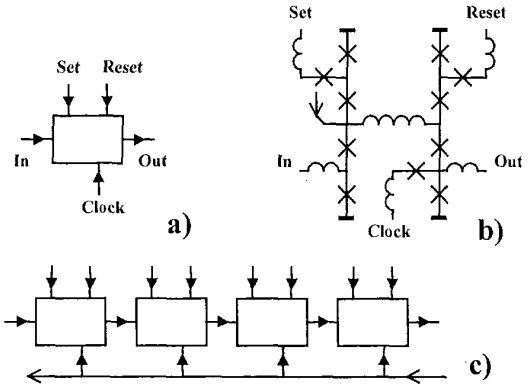

Fig. 2. Novel design of a parallel-to-serial converter: (a) notation of single cell; (b) schematic of single cell; (c) block diagram of a full parallel-to-serial converter.

The layout of the 8-channel multi-hit TDC is shown in Fig. 3. The 1 cm x 1 cm chip was fabricated in the 1 kA/cm^2 3-μm HYPRES fabrication process [3]. All common signals on the chip run on impedance-matched microstrip lines, which are magnetically connected to SFQ/dc converters on the appropriate input of each channel.

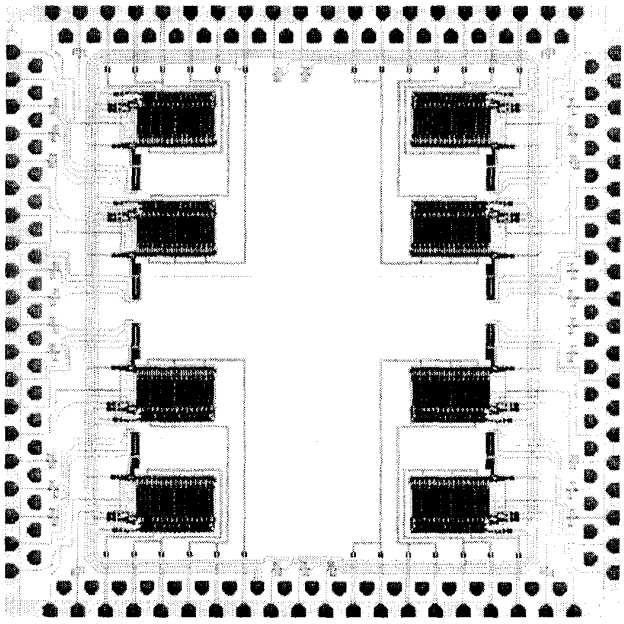

Fig. 3. Chip layout of the 8-channel TDC chip (1 cm x 1 cm).

B. *High-Resolution Multi-Hit TDC*

In order to increase time resolution, we have also designed a two-channel multi-hit high-resolution TDC. (See Fig. 4) Each of the two channels consists of a digital TDC (as described above) and an analog prescaler [4], [5] capable of digitizing fractions of the clock period.

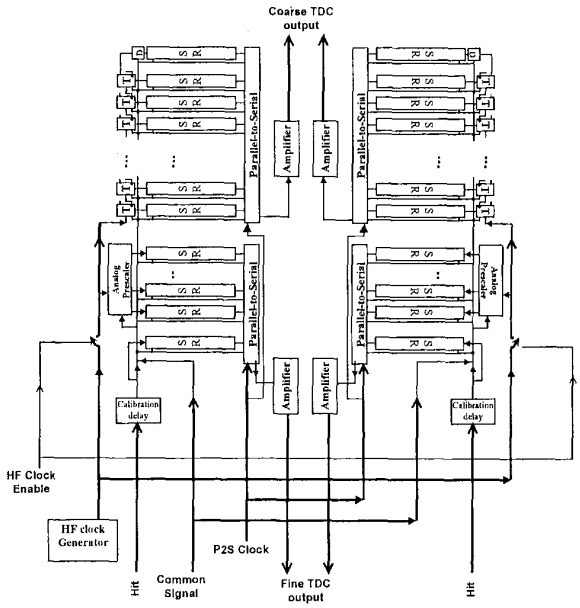

Fig. 4. Block diagram of a single High-Resolution TDC channel, consisting of a Fine TDC based on analog prescaler, and a Coarse TDC based on digital counters.

III. VXI Interface

A. *VXI based TDC Interface*

We have also developed a room-temperature interface using the VME Instrument Extension (VXI) standard. The VXI bus is widely accepted in physics laboratories.

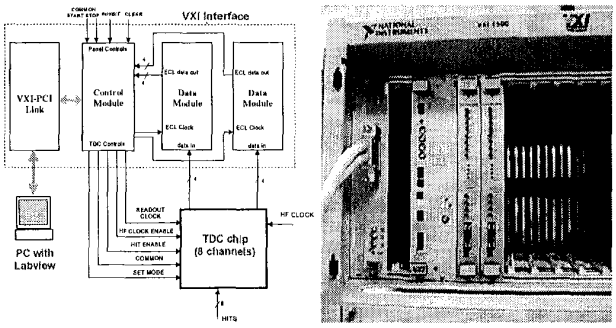

Fig. 5. A multi-channel, multi-hit time digitizer based on a superconductor TDC chip, a VXI-bus interface, and a PC running LabVIEW: (a) block diagram; (b) photo of the VXI interface (from left to right: commercial VXI-PCI link with cable to controlling PC, TDC Control Module (double slot module), and two 4-channel data receiver modules).

The interface generates all control signals necessary to operate the TDC chip, including both data acquisition and readout. Data from the chip is received and stored in local memory, than made available to the data acquisition controlling PC. This provides the functionality that users expect from a traditional (room temperature) TDC, but with a significant increase in performance, including the ability to switch between Common Start and Common Stop operation mode, and implementation of features such as a fast clear input, an inhibit input, and a software controlled test mode.

A block diagram and a photo of the TDC interface are shown in Fig. 5. The interface consists of a National Instruments VXI-PCI link to connect the VXI mainframe to the data acquisition PC, the Data receiver Modules, and the TDC Control Module. The complete interface, including data, TDC control, and VXI-PCI Link modules, was successfully tested using the acquisition program developed under LabVIEW.

B. *TDC Data Acquisition & Control Software*

The TDC data acquisition and control software is based on the LabVIEW platform. The data acquisition software system is designed with a polling routine to acquiring data from the VXI buffer memory, process and format them, and then store them to disk. Data processing subroutines do the actual data analysis, as well as bit checking, time interval extraction from the time stamps, and provide a Graphical User Interface (GUI) for data visualization. Fig. 6 shows a screen snapshot of the data acquisition part of the program.

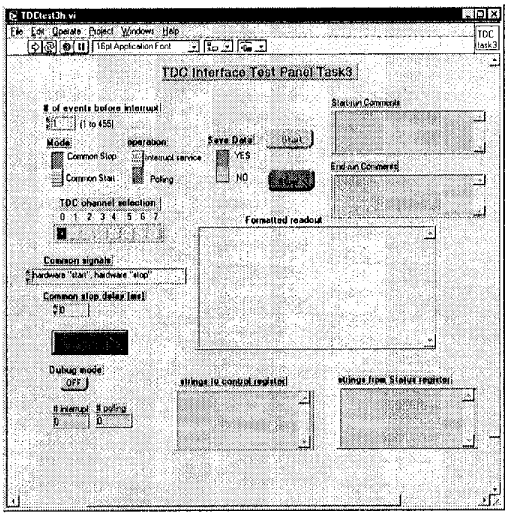

Fig. 6. TDC data acquisition program screen snapshot.

IV. TEST

A. *Low-speed Test of the TDC*

Because of the high complexity of the chip (more than 11,000 JJs), the fabrication yield has been low; however, we have successfully conducted tests at both low-speed and high-speed for the single channel of the TDC. To fully test the digital TDC at low speed, we used a computerized data acquisition setup [6]. This allowed us to directly verify the functionality of all bits of the counter and all words of the FIFO buffer before continuing with high-speed testing. Fig. 7 shows the results of this pattern verification. The test vector pattern checks all 9 words of the TDC using different numbers of CLOCK pulses for each of the 9 HIT signals. The dc bias current margins at low speed were up to 11%.

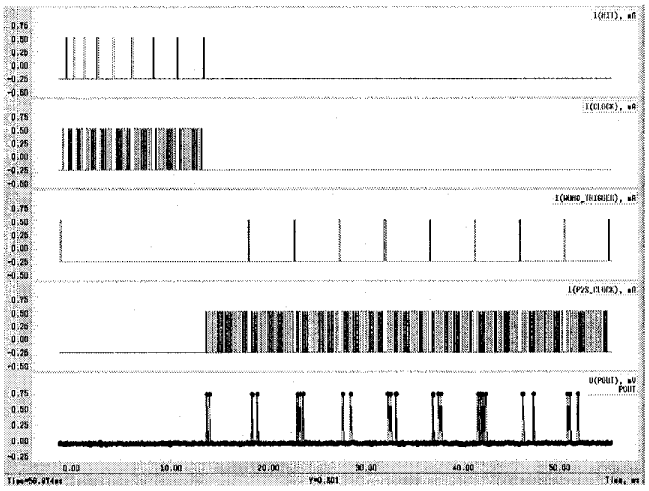

Fig. 7. Automated low-speed testing of the coarse digital TDC. In this case, the input sequence was {1-2-3-4-5-6-7-8-9}. The output (bottom trace) shows 9 numbers with a valid bit in front of each.

B. *High-speed Test of the TDC*

After passing the functional (low-speed) tests, the TDC chip underwent high-speed tests in order to determine its maximum working clock frequency. The results in Fig. 8 were taken at a 33 GHz clock frequency, which is the target frequency for the 6-bin prescaler architecture.

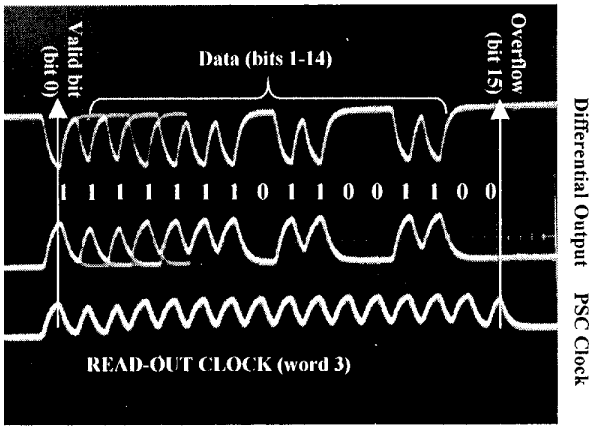

Fig. 8. High-speed testing of the digital (coarse) part of the TDC. The applied distance between the first and the second hits is 0.2 μs and the clock frequency is 33 GHz. The binary output number is {1100110111111}, which is 6591 in decimal. Thus, 6591 x (1/33 GHz) = 199.7 ns ≅ 0.2 μs.

One can see that the first four LSBs in Fig. 8 are unstable. This is due to the waveform jitter in the HP33120A signal generator used, which is (according to its manual) less than 25 ns. In fact, the fifth bit gives us $2^5 / (33\ GHz) \cong 1\ ns$ error.

C. Complete System Test with the VXI Interface

We have also successfully tested a single-channel TDC with our VXI module interface for functionality at low (100 MHz) frequencies. Fig. 9a shows the input sequence to the TDC chip, as monitored with an oscilloscope. Fig. 9b shows the correctly acquired and statistically processed TDC output. The TDC was operating in "Common Stop" mode. This means that all time intervals were counted until the COMMON STOP signal, which corresponds to 0 μs in Fig. 9b.

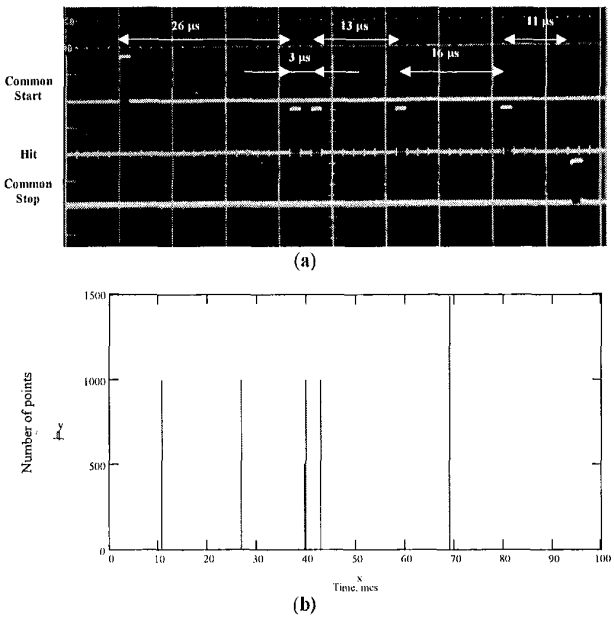

Fig. 9. Successful demonstration of a single channel of TDC with VXI interface. TDC input signals (a) and digitized output data (b). On the bar plot, Y-axis represents numbers of successfully detected signals (HITs) at the certain moment of time (X-axis). All HITs and COMMON START are counted from the COMMON STOP signal (which is at 0 on the time axis).

V. Conclusion

We have developed and demonstrated a complete Time Digitizing System. It consists of a superconductor RSFQ TDC chip, a custom built VXI interface, and a PC with controlling LabVIEW software.

The same VXI interface system with minor difference in software can serve both the 8-channel digital TDC and 2-channel High-Resolution TDC discussed.

We have demonstrated a single channel of the TDC working at 33 GHz clock frequency. The same channel has shown 11% of dc bias current margins at the low-speed test.

We have demostrated a successful operation of the VXI interface modules with the superconductor chip.

Next we plan to demonstrate a two-channel TDC with up to 6 ps time resolution. The device is going to be used in experiments at Fermi National Accelerator Laboratory (FNAL).

Acknowledgment

The authors would like to thank Alan Bross of the FNAL for useful discussions.

References

[1] A. F. Kirichenko, O. A. Mukhanov, and S. V. Rylov, "Superconductive time-to-digital converters", in: *Extended Abstracts of ISEC'97*, Berlin, Germany, vol. 1, pp. 34-37, Jun. 1997.

[2] L.S. Yu, C.J. Berry, R.E. Drake, K. Li, R.M. Patt, M. Radparvar, S.R. Whiteley, and S.M. Faris, "An all-niobium eight level process for small and medium scale applications," *IEEE Trans. Mag.*, vol 23, pp. 1476-1479, March 1987; see also HYPRES Nb Process Design Rules, http://www.hypres.com/.

[3] A. Kirichenko and O. Mukhanov, "A Superconductive High-Resolution Time-to-Digital Converter", *Extended Abstracts of ISEC'99*, Berkeley, USA, p. 353, Jun. 1999.

[4] S. Kaplan, A. Kirichenko, O. Mukhanov, and S. Sarwana "A Prescaler Circuit for a Superconductive Time-to-Digital Converter", *this conference*, poster # EI08.

[5] S. Polonsky et al., "Single Flux Quantum B flip-flop and its possible applications", *IEEE trans. on Appl. Supercond.*, vol.4, p .9 1994.

[6] D. Zinoviev and Y. Polyakov, "Octopux: An advanced automated setup for testing superconductor circuits," *IEEE Trans. Appl. Supercond.* vol. 7, pp. 3240-3243, Jun. 1997.