Microwave Receivers with Direct Digitization

Dmitri E. Kirichenko, Timur V. Filippov, and Deepnarayan Gupta

HYPRES, Elmsford, NY, 10532, U.S.A.

***Abstract* — Superconductor analog-to-digital converters (ADCs) and ultrafast digital circuitry enable processing of microwave signals entirely in the digital domain. We have designed and demonstrated a wide variety of continuous-time bandpass delta-sigma modulators using Josephson junction comparators. Featuring sampling frequencies up to 30 GHz, single-chip digital receivers have been demonstrated by connecting a rapid single flux quantum (RSFQ) digital circuitry with these ADCs. These receiver chips, cooled to 4 K by cryogen-free refrigerators, have been used with room-temperature digital processors to demonstrate reception of microwave signals for X-band satellite communications and Link-16 data links. To date, the highest frequency of direct digitization is 21 GHz for satellite communication. We report recent advances in ADC design to obtain higher dynamic range.**

***Index Terms* — Analog-to-digital converter, RSFQ, cryogenic, SATCOM.**

I. Introduction

The goal of modern radio frequency (RF) receiver systems is to operate simultaneously in multiple frequency bands and maximize spectrum utilization while supporting diverse modalities, e.g. voice, data, video, and particularly in case of military systems, detection and ranging, and electronic countermeasures. With the advent of software and cognitive radio concepts, there is a growing desire to bring the flexibility and fidelity of digital processing to the RF domain. This, however, requires direct digitization of the received RF signal. Radio frequency receivers at the higher end of the spectrum have always had one or more analog down-converters; until recently, no analog-to-digital converter (ADC) was capable of directly converting microwave signals. A digital-RF receiver, featuring direct digitization followed by subsequent digital processing, circumvents all the limitations of an analog RF receiver front-end, enables scalability, agility, rapid reconfigurability, and supports advanced waveforms, such as those with fast frequency hopping.

One of the primary advantages of digital processing lies in the ability to produce multiple copies without loss of power or fidelity. In a digital-RF receiver, multiple, independent chains of digital signal processing elements, performing a variety of functions such as down-conversion, filtering, and demodulation, follow a fast ADC. Our multi-band digital-RF architecture uniquely incorporates RF switching and distribution in the digital domain, providing programmable connectivity between a set of ADCs and a set of digital processors [1]. Although this digital-RF architecture and all its elements are technology-independent, superconductor integrated circuit (IC) technology with Niobium (Nb) Josephson junctions (JJs), currently offer the best solution. Superconductor ICs combine high-linearity, wideband ADCs [2] and ultrafast digital logic, called rapid single flux quantum (RSFQ). A family of superconductor digital-RF receiver (called ADR) chips (Fig. 1), comprising an ADC and a digital channelizer circuit, performing digital down-conversion and filtering, have been demonstrated. Notably, a digital-RF receiver system, comprising a cryocooled ADR chip, was demonstrated reception of live satellite communication signals in the X-band (7.25-7.75 GHz) [3]. In this paper, we focus on ADCs for various microwave frequency bands ranging from 1 GHz to 21 GHz.

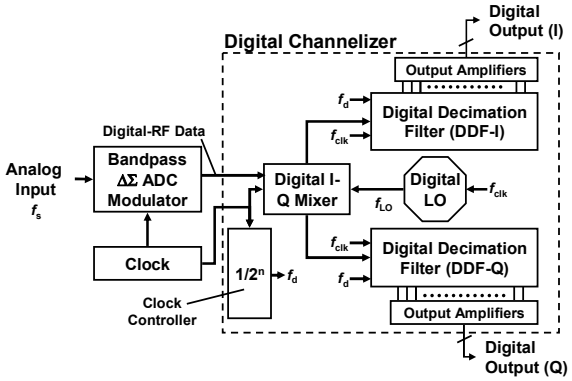

Fig. 1. Block diagram of a digital-RF receiver (ADR) chip.

II. Digitization of Microwave Signals

Superconductor ADCs combine comparators with ultra-fast switching speed and natural quantization of magnetic flux to enable fast and accurate data conversion. There are various types of superconductor ADCs, including lowpass phase-modulation-demodulation (PMD) [4] and wideband flash ADCs [5], for different applications. Most suited for maximizing signal-to-noise ratio (SNR) in a microwave band is a bandpass delta-sigma (BPΔΣ) modulator [6].

An ideal oversampled delta-sigma modulator of order n, using an m-bit quantizer sampled at f_{clk}, produces a signal-to-noise dynamic range given by

$$SNR = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right)\left(2^m - 1\right)^2 R^{2n+1}, \qquad (1)$$

where $R = f_{clk}/2\Delta f$ is the oversampling ratio. There are various methods to increase SNR of such a BPΔΣ modulator: (1) increasing the order (n) of the modulator to produce deeper and/or wider quantization noise minimum, (2) increasing the

number of quantization thresholds (2^m-1), (3) increasing oversampling ratio by increasing sampling rate (f_{clk}). Besides, there are multi-modulator ADC schemes, such as the subranging architecture.

Oversampling spreads the quantization noise over a wider bandwidth of $f_{clk}/2$. Subsequent digital filtering rejects noise outside the band-of-interest (Δf), delivering higher SNR. Therefore, the higher the oversampling ratio the larger is SNR. With a high oversampling ratio (HYPRES X-band ADR uses R=256) one can generate many bits of resolution over the bandwidth-of-interest starting from just one (m=1). Delta-sigma modulators provide further enhancement by shaping the quantization noise to have minima in the band-of-interest. The higher the order of the modulator the better is the minimization of noise in a given bandwidth. For BPΔΣ modulators, the order (n) is the number of complex conjugate pairs of poles in the loop filter.

The basic first-order, continuous-time, single-threshold BPΔΣ modulator design involves an analog resonator as the loop filter and a pair of Josephson junctions forming a clocked comparator [6]. One of the unique features of the superconductor delta-sigma ADC modulators is implicit feedback: when the clocked comparator switches, it subtracts a single flux quantum (Φ_0 = 2.07 fWb) from the input while producing a digital output SFQ pulse. Therefore, no explicit feedback loop is needed to construct a first-order modulator. Fig. 2 shows the digitized spectrum of a Ka-band (20.2-21.2 GHz) single-chip digital-RF receiver (called ADR), comprising a 1st-order BPΔΣ modulator and a digital channelizer, sampled at $f_{clk} = 4f_s/3$ for minimizing noise from digital local oscillator harmonics [3].

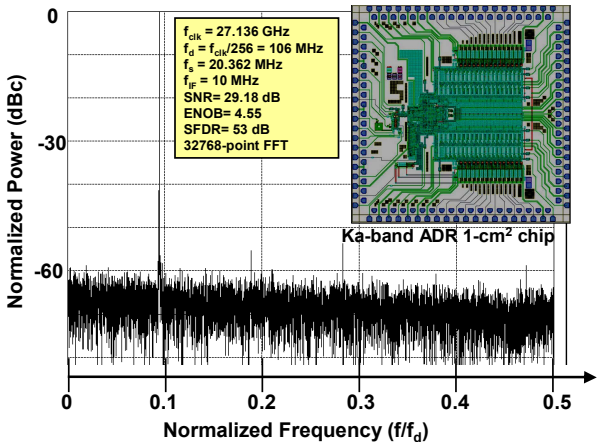

Fig. 2. Spectrum of a 20.362 GHz RF signal directly digitized with a 1-cm^2 Ka-band ADR chip containing over 10,000 Josephson junctions. It was fabricated with J_c = 4.5 kA/cm^2 process at HYPRES. The sampling clock frequency was 27.136 GHz. Only half the spectrum, from the output of one DDF, is shown.

Increasing the sampling clock frequency is ultimately limited by the switching speed of JJs. This, in turn, is constrained by the junction fabrication technology, currently limited by lithography (1.5 μm minimum JJ diameter, critical current density, J_c = 4.5 kA/cm^2) to a sampling speed of about 50-60 GHz. With current fabrication technology, we have demonstrated sampling rates up to 32 GHz in BPΔΣ and 49 GHz in lowpass PMD ADCs. In the original designs, the ADC sampling clock was used to clock digital mixers and filters on the same chip. On-chip digital decimation filter (DDFs) is much more complex than the ADC and its maximum clock speed is limited to about 30 GHz. To circumvent this limitation, we demultiplexed the ADC output by a factor of 2 before using a half-rate filter (X2DDF) operating with a clock at half the ADC sampling clock frequency. Employing the same design concept used for a time-interleaved ADC [7], the X2DDF accommodates two alternately clocked data streams by minimum additional complexity.

A. Higher-order Bandpass Delta-sigma Modulators

Increasing the order of the modulator involves creating a more complex loop filter transfer function. Fig. 3(a) and 3(b) show a block diagram and the corresponding schematic diagram of a type of second-order ADC modulator employing an explicit feedback path. Josephson transmission lines (JTLs) as active delay elements are used in addition to a D flip-flop (DFF) to control the phase of the feedback signal. Called α-BPΔΣ, we have designed and demonstrated a wide range of ADCs with a second-order explicit feedback loop. Often the two resonant frequencies are slightly separated to minimize noise in a band. For example, the MILSATCOM X-band ADC had two resonators at 7.4 and 7.6 GHz respectively, with quality factor estimated to be around 100.

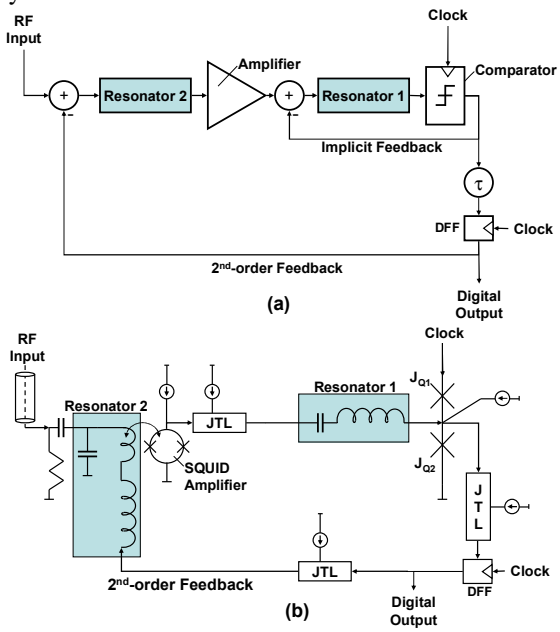

Fig. 3. (a) Block diagram and (b) simplified circuit schematic of second-order α-BPΔΣ modulator with explicit feedback.

Delays in explicit feedback loops present a scaling problem to higher order modulator design. Recently, we designed a modulator with two implicit feedback paths by connecting two resonators directly to the comparator. To distinguish from the explicit feedback scheme, we call this the β-BPΔΣ modulator

(Fig. 4). The RF input was split and applied through inductive coupling to each resonator. In addition, a SQUID amplifier stage was used to connect the two series LC resonators in series to get the desired loop filter transfer function. We recently demonstrated operation of a β-BPΔΣADC chip (Fig. 5). A 1:16 demultiplexer [8] was integrated on the same chip to facilitate data acquisition. We observed the desired noise-shaping despite the data acquisition system limiting f_{clk} to about 10 GHz, and therefore, the maximum SNR.

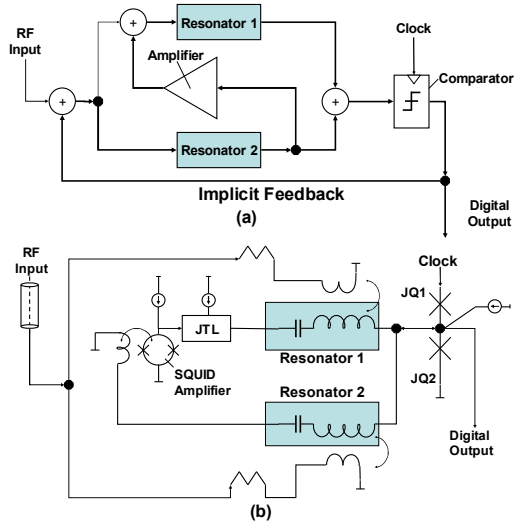

Fig. 4. (a) Block diagram, and (b) simplified circuit schematic of a second-order β-BPΔΣ modulator with double implicit feedback.

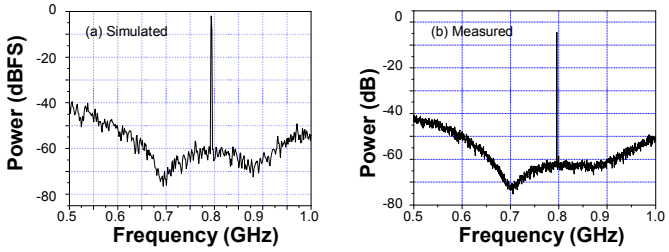

Fig. 5. (a) Simulated and (b) measured spectra of β-BPΔΣ modulator used to digitize a 200 MHz band around 800 MHz. The 5-mm ADC chip included a 1:16 deserializer and was clocked at 10.24 GHz. The input signal frequency is 796 MHz. The SNR of the spectrum shown in (b) is 31.6 dB in 660—915 MHz band.

It is easier to scale such a multiple implicit feedback ADC design to higher order. Furthermore, the quasi-instantaneous feedback allows more freedom in choosing clock frequencies compared to the one with explicit feedback. Unavoidable delays in the external feedback loop constraint the α-BPΔΣ modulator performance to be optimal when the sampling frequency f_{clk} is related to the signal frequency: $4f_s$, $4f_s/3$, etc. The same quasi-instantaneous feedback feature does present a problem for β-BPΔΣ modulator, however, especially at higher frequencies. The feedback timings are imprecise in implicit feedback. The re-synchronization of the feedback pulse with a precise clock pulse reduces, and in special cases of $f_{clk} = 4f_s$, $4f_s/3$, etc., completely eliminates this problem in the α-BPΔΣ modulator. Since the negative effect of feedback timing imperfection on modulator performance is proportional to frequency of the loop filter poles, the β design becomes less preferable as the target signal frequency increases.

B. Multi-threshold Bandpass Delta-sigma Modulators

Another method to extend the dynamic range is to increase the number of thresholds in the quantizer. This direction is the hardest to pursue in terms of circuit complexity, not only for the modulator but also for the subsequent digital circuitry which has to accept and process multi-bit data at extremely high speed.

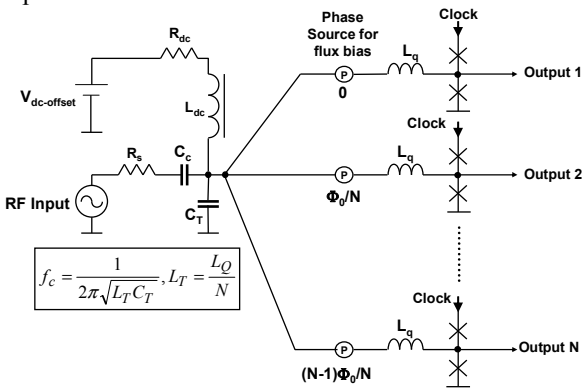

Fig. 6. Multi-threshold 1st-order bandpass delta-sigma modulator.

Typically, such a multi-level quantizer requires precision matching of elements to prevent deterministic errors, which are manifested as nonlinear artifacts. Our scheme employs a parallel combination of Josephson junction comparators, together with a sequence of magnetic flux bias levels, to yield an automatic cyclic permutation of the quantization levels. Fig. 6 shows our multi-threshold quantization circuit, comprising a set of N clocked comparators. The thresholds are spread uniformly between 0 and Φ_0, by applying an appropriate flux bias in each arm. For N comparators, there are N thresholds separated by Φ_0/N. For a given input signal level, k comparators will switch, each sending back a feedback signal of Φ_0, and causing a $k\Phi_0/N$ shift of flux bias. Another way to think about this is by considering step-wise rotation of a wheel. When the signal is greater than k thresholds (k=0,1,…,N), all the thresholds rotate by k steps. This dynamic rotation serves to randomize small mismatches in bias and element values, reducing nonlinear artifacts.

In a digital-RF receiver, the ADC modulator is followed by a digital channelizer circuit comprising in-phase and quadrature (I&Q) mixers and two decimation filters with appropriate output drivers [1]. Our first generation digital channelizer circuit employed a 1×1 digital mixer [9] that operated on 1-bit digital data from both the ADC and the digital local oscillator (LO). The multi-threshold ADC implementation requires extension of the digital mixer design to multi-bit input, as well as a summing circuit to add all the N individual comparator outputs into a multi-bit binary word for compatibility with the DDF. Our DDF consists of bit slices, each designed to accept an appropriately weighted binary input, except the first slice which accepts two inputs of equal

(least) significance. To validate the multi-threshold BPΔΣ modulator design concept, we designed a chip with a two-threshold ADC, a 2×1 digital I and Q mixer (Fig. 8) using RS flip-flops with non-destructive readout (RSN) cells [1], and two digital filters. The ADC sends digitized data (D1 and D2) along with the clock to the mixer, which produces two sets of outputs (M1 and M2) for I and Q DDFs using 4 phases of a digital local oscillator. This ADR produced 63 dB SFDR and 41 dB SNR in 96 MHz instantaneous bandwidth (only one half shown in Fig. 7 for clarity).

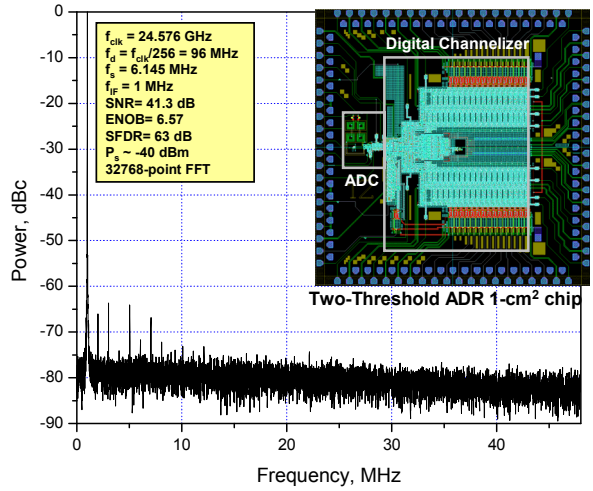

Fig. 7. One half of the digitized spectrum (from one DDF) of a two-threshold ADR chip. Following complex mixing and decimation by 256, the output rates of the I and Q words are 96 Msample/s each.

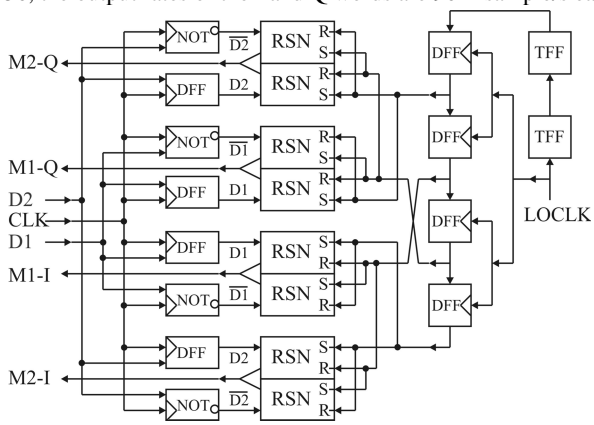

Fig. 8. Block diagram of a 2×1 digital I and Q mixer.

The logic for generating the 4 phases of the local oscillator is also altered to overcome the susceptibility of the previous design [9] to any error in the toggle flip-flop (TFF) tree causing a permanent phase slip between I and Q streams. Here, a single data pulse is injected to the first DFF every 4 clock pulses by dividing with a cascaded pair of TFFs. The data pulse gets sequentially shifted to the next DFF cell by subsequent clock pulses. In any given period local oscillator (LO) period, $\tau=1/4f_{LO}$, only one DFF is 'set' and produces an output pulse ('1'). The effect of any error is limited only to a short interval (τ or 2τ depending on which TFF malfunctions). The error does not propagate and there is no phase change between the I and the Q streams, and no disruption in the receiver operation.

III. CONCLUSION

Direct digitization of microwave signals in the 0.8-21 GHz range has been demonstrated using superconductor ICs. Bandpass delta-sigma ADCs, sampled at clock frequencies up to 30 GHz, have been used to perform wideband digitization in various frequency bands. All the ADCs use one or more resonators to minimize quantization noise over a band-of-interest (such as 7.25-7.75 GHz). Single-chip digital receivers, combining an ADC with a digital channelizer performing down-conversion and filtering, have been demonstrated for satellite communication and other applications.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of U. S. Army CERDEC and the Office of Naval Research.

REFERENCES

[1] D. Gupta, T. V. Filippov, A. F. Kirichenko, D. E. Kirichenko, I. V. Vernik, A. Sahu, S. Sarwana, P. Shevchenko, A. Talalaevskii, and O. A. Mukhanov, "Digital Channelizing Radio Frequency Receiver," IEEE Trans. Appl. Supercond., vol. 17, pp. 430-437, June 2007.

[2] O. A. Mukhanov, D. Gupta, A. M. Kadin, and V. K. Semenov, "Superconductor analog-to-digital converters," Proceedings of the IEEE, vol. 92, pp. 1564-1584, Oct. 2004.

[3] J. Wong, R. Dunnegan, D. Gupta, D. Kirichenko, V. Dotsenko, R. Webber, R. Miller, O. Mukhanov, and R. Hitt, "High Performance, All Digital RF Receiver Tested at 7.5 GigaHertz," Military Communications Conference, 2007 (MILCOM 2007). IEEE Digital Object Identifier: 10.1109/MILCOM.2007.4455052, pp. 1-5, 2007.

[4] S. V. Rylov and R. P. Robertazzi, "Superconductive high-resolution A/D converter with phase modulation and multi-channel timing arbitration," IEEE Trans. Appl. Supercond., vol. 5, pp. 2260-2263, June 1995.

[5] P. Bradley and H. Dang, "A 6-bit Josephson Flash A/D Converter with GHz Input Bandwidth," IEEE Trans. Appl. Supercond., vol. 3, pp. 2550-2557, March 1993.

[6] J. X. Przybysz, D. L. Miller, E. H. Naviasky, and J. H. Kang, "Josephson sigma-delta modulator for high dynamic range A/D conversion," IEEE Trans. Appl. Supercond., vol. 3, pp. 2732-2735, March 1993.

[7] T. V. Filippov, S. V. Pflyuk, V. K. Semenov, and E. B. Wikborg, "Encoders and decimation filters for superconductor oversampling ADCs," IEEE Trans. on Appl. Supercond., vol. 11, pp. 545-549, Mar. 2001.

[8] P.S. Shevchenko, D.E. Kirichenko, R. Miller, and D. Gupta, "Polyphase Sliding Goertzel Demodulator for Continuous Phase Frequency Modulated Signals," to appear in IEEE Trans. Appl. Supercond., June 2009.

[9] A. Kirichenko, S. Sarwana, D. Gupta, and D. Yohannes, "Superconductor digital receiver components," IEEE Trans. on Appl. Supercond., vol. 15, pp. 249-254, June 2005.