High Quality On-Chip Long Annular Josephson Junction Clock Source for Digital Superconducting Electronics

Dmitri E. Kirichenko and Igor V. Vernik

***Abstract*—We have developed clock sources for rapid single flux quantum (RSFQ) digital circuits using high-quality long Josephson junction (LJJ) resonant oscillators of annular geometry. Being a topologically closed system and unperturbed by reflections from boundaries and collisions among the fluxons (flux quanta), the annular LJJ oscillator has demonstrated a high quality factor. The novel design of an annular junction clock that allows easier interface with RSFQ circuitry has been realized. Magnetic fluxons are inserted into an annular LJJ by local injection of current into the control line of the junction. This technique resolves the long-standing problem of achieving superior stability of the fluxon state for application as a clock source. The linewidth of the phase-locked clock source is measured as low as 24 Hz relative to a reference oscillator at 40 GHz. The cycle-to-cycle jitter was measured to be 9 fs at a frequency of 36 GHz, or 0.04% of the clock period which is in good agreement with theoretical estimation.**

***Index Terms*—Long Josephson junction, on-chip high frequency clock source, superconductor digital electronics.**

I. Introduction

THE prospect of cryogenic superconductor digital electronics is encouraging for a number of commercial and military applications, where its advantages in high speed (10–100 GHz), low power consumption (∼mW per chip) and quantum accuracy are superior to other technologies. Almost all superconducting digital electronics require a clock signal in the multi-GHz range. External clock generators capable of such high frequency are very expensive and require extensive waveguides and transmission lines, which makes a dominant contribution to the thermal load on the cryogenic system by conducting heat from room temperature. In spite of significant advances in closed-cycle refrigerators, the major hindrance to introduction of superconductor electronics in a range of products, such as wideband radios for wireless communications, high-speed network switches and routers, remains the cost and complexity of the cryogenic support system. An on-chip high-frequency clock source eliminates the need for expensive external generators, increases system integration, while diminishing the system power requirements by reducing the thermal load.

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We have chosen an clock generator based on resonant fluxon (or a magnetic flux quanta, $\Phi_0 = h/2e$) modes in a long Josephson junction (LJJ), referring to a two-dimensional geometry, which is much larger than the Josephson penetration depth (λ_J) in one dimension and much smaller in the other [1]. This selection among various on-chip clock sources for superconductor electronics is justified by the high quality factor of this oscillator [2]. Usually, the higher the quality factor, the lower is the time jitter of the corresponding clock signal. The accuracy of large scale digital circuits, e.g. data conversion devices like analog-to-digital, digital-to-analog, and time-to-digital converters depend on the quality of the clock source, especially at very high (>10 GHz) clock speeds. RSFQ clock sources based on LJJ resonant oscillators have demonstrated Q greater than 10^6 [2] and a time jitter of 50 fs [3].

LJJ oscillators of two geometries; linear and annular, have been realized before. Due to its closed topology and unperturbed by reflections from boundaries and collisions among the fluxons, the annular LJJ has demonstrated superior stability and higher quality factor than the linear LJJ oscillator.

Two major problems in utilizing annular junctions for on-chip clocking of superconducting electronics are: 1). Preparation of the *stable* initial fluxon state of the junction and 2). *Interfacing* of the annular clock generator with digital circuitry.

II. Phase-Locked Annular Long Josephson Junction Oscillator

In order to realize fluxon states, magnetic flux quanta have to be trapped in the junction, i.e., between its superconducting electrodes. The most reliable and reproducible technique requires a rather exotic and complicated facility, namely a low-temperature scanning electron or laser microscope [4]. Another possible method is trapping fluxons while cooling the sample below the critical temperature of its superconducting electrodes in the presence of a magnetic field. This can be facilitated by sending a current through a coil placed above the junction [5] or by applying a small bias current [6]. Unfortunately, the latter techniques are often not reproducible. An improved technique of inserting fluxons into the annular junction in a controllable fashion has been realized following [7]. This is based on injection of a local current I_C into the control line as is schematically shown in Fig. 1. When the current I_C is turned on, it generates a local magnetic flux Φ_C in the junction area between the injection leads. While the net current across the Josephson barrier remains zero, if the current I_C is large enough such that $\Phi_C > \Phi_0$, it nucleates a magnetic fluxon, which remains pinned in the region

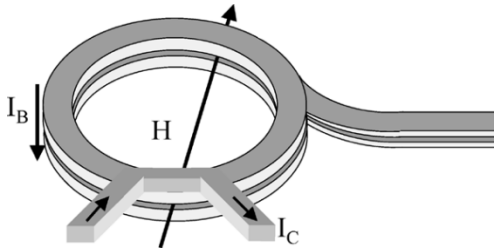

Fig. 1. Sketch of the annular Josephson junction with control current leads and "tail" (dimensions are not to scale).

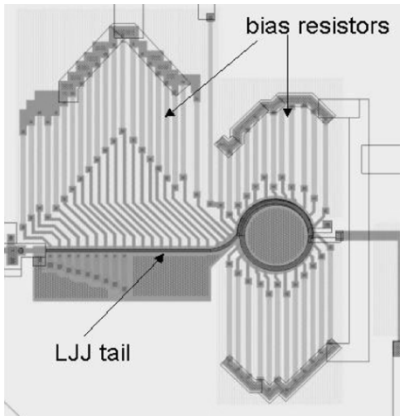

Fig. 2. Layout of annular Josephson generator.

where the current is injected. Simultaneously, due to magnetic flux conservation in the ring, there appears a free fluxon of opposite polarity (antifluxon). The antifluxon can be driven along the junction by the bias current $\mathrm{I_B}$. Similarly, if $\Phi_\mathrm{C} > 2\Phi_0$, there appear two free antifluxons, and so on.

The difficulty of interfacing with RSFQ digital circuitry arises from the absence of well-defined boundaries in the annular junction. Straightforward coupling of digital circuitry to the annular LJJ breaks the system symmetry and has an adverse effect on the stability of the resonant mode. In our novel design first interfacing the annular LJJ has a tail-like part (shown in Fig. 1) when interfaced to ordinary JTL. This allows easier coupling with RSFQ circuitry. Fig. 2 shows the chip layout in the vicinity of the annular junction. In order to improve uniformity, bias current is fed through resistors. The designated bias lead is employed for the junction tail. The annular junction has a mean radius of 40 $\mu\mathrm{m}$ and a width of 5 $\mu\mathrm{m}$.

The local control line and tail-like LJJ significantly improve the stability and current amplitude of the resonant mode. Fig. 3 shows the layout of the 5 mm chip composed of annular LJJ oscillator coupled to the chain of binary frequency dividers and phase-lock circuitry through the LJJ tail.

The chip was fabricated using the standard HYPRES 3 $\mu\mathrm{m}$ 1 $\mathrm{kA/cm^2}$ process [8]. The major part of phase-locked loop, phase detector, was realized by RSFQ RS latch and integrated on-chip. The circuits on chip include a binary counter (T flip-flop chain) with output monitors and an array of RS latches synchronized with an external room temperature reference source. Each RS latch acts as the phase detector with dc voltage proportional to the phase difference between decimated output from the annular LJJ and the external reference input. The

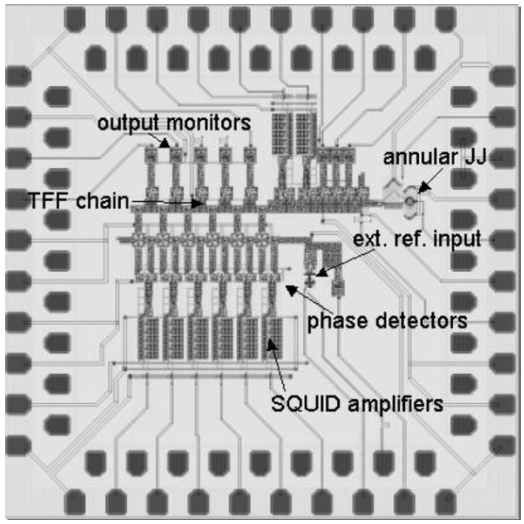

Fig. 3. Layout of a chip containing annular JJ generator and digital circuitry.

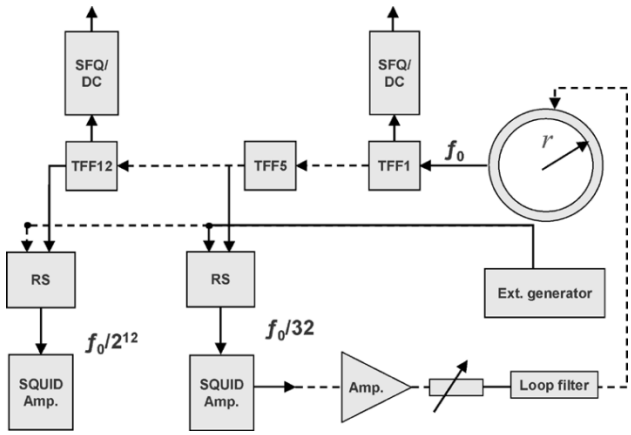

Fig. 4. The complete block diagram of the experimental setup for phase-lock measurements.

digital outputs for monitors and RS latches were obtained using TFF-type SFQ/DC converters that convert SFQ pulses into transitions of a voltage waveform of $\sim$ 250 $\mu\mathrm{V}$ amplitude, which was subsequently amplified in a phase-locked loop (PLL) to at least 2 mV by on-chip SQUID amplifiers.

The complete block diagram of the experimental setup for phase-lock measurements, including the chip circuitry and room temperature instruments is shown in Fig. 4. The amplifier increases the ability of the PLL to handle a current load by broadening the phase-locked current range on the fluxon step.

III. Experimental Results

The annular LJJ is a topologically closed system such that the number of trapped fluxons is conserved and new fluxons can be created only in the form of fluxon—antifluxon pairs. A control current of 10.4 mA introduced single fluxon-antifluxon pair into the annular junction. The same control current produced the magnetic field H (see Fig. 1) that pinned the trapped antifluxon while the fluxon is accelerated along the junction toward the "tail" by the applied bias current. This motion gives rise to the dc voltage across the junction, which is proportional to the fluxon's mean velocity. Single fluxon dynamics is reflected by

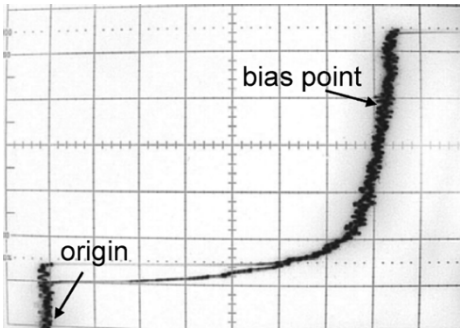

Fig. 5. The I-V curve of annular Josephson junction with 10.4 mA control current. The horizontal and vertical scales are 10 mV/div and 1 mA/div.

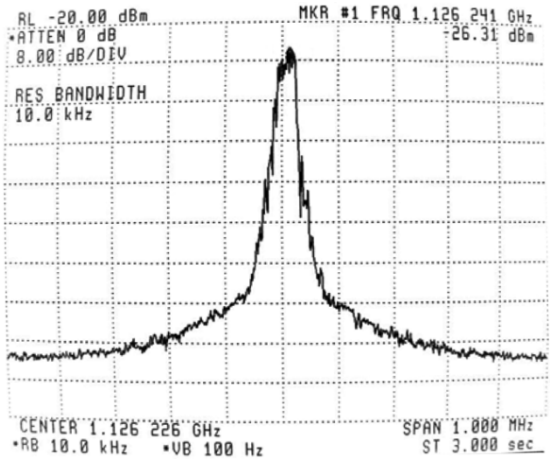

Fig. 6. The spectrum of free running annular LJJ set up at f $= 36$ GHz.

the appearance of a pronounced vertical step in Fig. 5, which shows the current voltage dependence (I-V curve) of the annular LJJ. The bias of the LJJ tail strongly affected the stability and height of the fluxon step and was adjusted to obtain a step with the largest current amplitude. The LJJ tail was caused the I-V curve to be asymmetric with respect to the origin, with only the positive quadrant exhibiting pronounced fluxon step that is shown in Fig. 5. The annular LJJ acts as a clock source with frequency of $f = V_{dc}/\Phi_0$, when junction is biased at V_{dc} voltage.

For the annular junction biased at 4.2 mA, the quality factor $Q\ (= f/\Delta f)$ is equal to 4.8×10^6 at $f = 36$ GHz using the thermal noise model formulae for the linewidth Δf of the oscillator [9]:

$$\Delta f = \left(\frac{4\pi k_B T}{\Phi_0^2}\right)\left(\frac{R_d^2}{R_s}\right) \tag{1}$$

where $k_B = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant and R_d and R_s are the differential and dc resistance at the bias point, respectively. Fig. 6 shows the spectral characteristic of the free running annular LJJ clock set up at the bias point of Fig. 5 after division by 32, i.e. TFF4 in the divider chain (see Fig. 4), and the TFF based SFQ/DC converter. In this paper for the direct spectral measurements, the output from chip was amplified by 30 dB with three Picosecond Pulse Lab amplifiers (model 5830) connected in series and then fed to HP70000 spectrum analyzer.

For the first set of phase-lock results, injection phase-locked measurements, the junction was phase-locked to the 16th harmonic of a room temperature synthesizer set up at 2.48 GHz and fed to the junction through the bias lead.

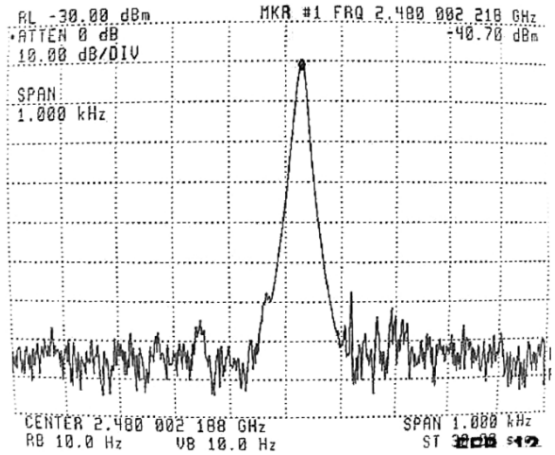

Fig. 7. The spectrum of annular LJJ set up at f $= 39.7$ GHz. The junction was phase-locked to 16th harmonic of room temperature synthesizer set up at 2.48 GHz and fed to the junction through bias lead.

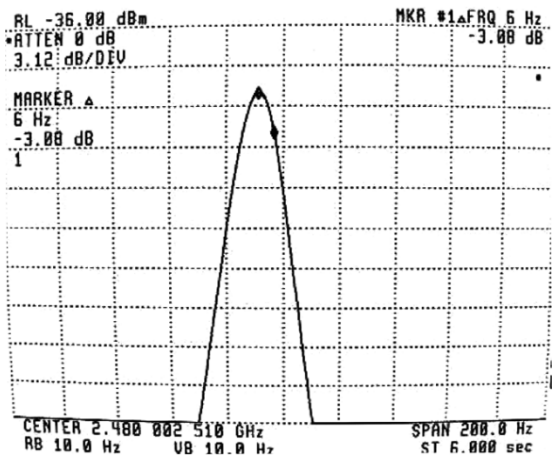

Fig. 8. The spectrum in Fig. 6 set up for –3 dB linewidth measurements.

Fig. 7 shows the spectral characteristic of the injection phase-locked annular Josephson junction clock source set up at $f = 39.7$ GHz at the bias point slightly above on I-V curve then shown in Fig. 5. A spectrum is shown after division by 16. The same spectrum in more details for the -3 dB linewidth measurements is presented in Fig. 8. For every TFF in the divider chain, assuming uncorrelated fluctuations in successive clock cycles, the standard deviation of the TFF output period is $\sqrt{2}$ greater than the standard deviation of the period of its input. For a TFF, the output period is twice the input period; then, the linewidth is a factor of $\sqrt{2}$ lower after every TFF. Therefore, a 6 Hz linewidth in Fig. 7 after four sequential TFFs translates into a 24 Hz linewidth of the phase-locked annular LJJ clock generator.

The second set of results on phase-locked annular LJJ clock was obtained using the PLL block diagram shown in Fig. 4. Fig. 9 shows the spectrum of the phase-locked annular LJJ clock biased at the bias point of Fig. 5 at $f = 36$ GHz.

The frequency is measured after division by 32. The annular junction has been locked by an external 70 MHz signal from a

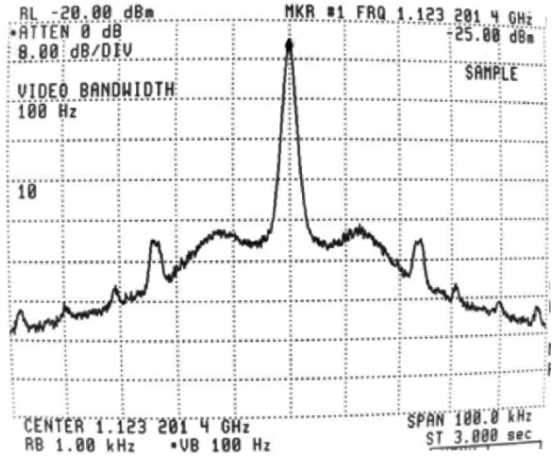

Fig. 9. The spectrum of the phase-locked annular LJJ clock generator. See text for details.

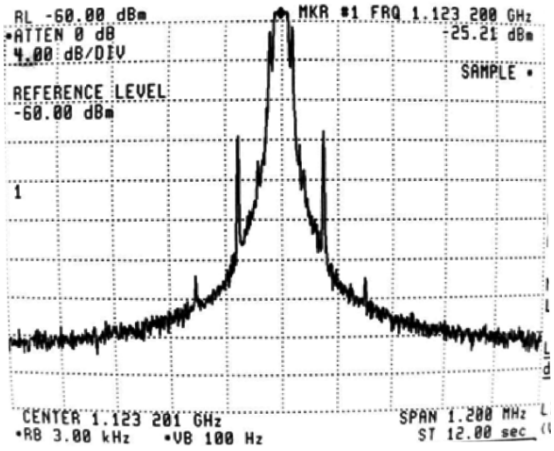

Fig. 10. The spectrum of the phase-locked annular LJJ clock generator used to calculate cycle-to-cycle jitter.

room temperature generator after an extra division by 16. The spectrum clearly shows the phase-lock range of about 25 kHz.

For the annular LJJ oscillator the cycle-to-cycle jitter, or timing fluctuations in two consecutive clock cycles can be calculated following the approach developed in [10] by analyzing the frequency spectrum shown in Fig. 10.

This oscillator can be modeled as noiseless current-controlled oscillator (CCO), whose input is fed by current noise source. Assuming, the noise process has uniform power spectral density $S_I(\omega) = n_i^2$, then the power spectral density of the phase S_Φ varies as $1/\omega^2$:

$$S_\Phi(\omega) = \frac{K_0^2 n_i^2}{\omega^2} \tag{2}$$

and cycle-to-cycle jitter expressed as:

$$\sigma_T = \frac{K_0 n_i}{2\pi} T_0 \sqrt{T_0}, \tag{3}$$

where K_0 is the CCO current-to frequency conversion constant and T_0 is the average clock cycle. The cycle-to-cycle jitter of phase-locked annular LJJ clock generator is determined from (3) to be 9 fs or 0.04% of period of the clock at a frequency of 36 GHz by accomplishing the following steps [10]. First, the power spectrum $P(f)$ as measured in the instrument and shown in Fig. 10 is transformed into phase noise spectrum $S_\Phi(f)$ in units of dBc/Hz as following:

$$S_\Phi(f) = 10 \log \left(\frac{P(f)}{P_C BW_N} \right) \tag{4}$$

The total output power of the signal P_C must be is computed by integrating the power spectral density. Then the spectral data is normalized by the total power and the noise-equivalent bandwidth BW_N of the resolution bandwidth BW_{res} of the instrument used for the measurements. For the spectrum analyzer used in our experiment $BW_N = 1.2BW_{res}$. Then, the factor $K_0 n_i$ in (3) required for cycle-to-cycle jitter calculation is obtained from a least-squares fit of a single sideband of the phase noise spectrum on a log-log scale.

Following the full statistical treatment of thermal fluctuation in the fluxon velocity [9] the cycle-to-cycle jitter was calculated to be 5 fs at frequency of 36 GHz, which is in good agreement with the measured results.

IV. Conclusions

Clock sources for RSFQ digital circuits using high-quality annular LJJ resonant oscillators have been developed. A novel design of annular junction clock that allows easier interface with RSFQ circuitry and controllable preparation of fluxon state has been realized. This design resolves the long-standing problems of interfacing with digital circuitry and achieving superior stability for prepared fluxon state in application as a clock source. In addition, annular LJJ clock was incorporated in phase-locked loop with its major part, phase detector, integrated on-chip next to the clock source. A linewidth of the phase-locked clock source as low as 24 Hz is measured relative to a reference oscillator at 40 GHz. The cycle-to-cycle jitter of phase-locked clock source was measured to be 9 fs at a frequency of 36 GHz, or 0.04% of the clock period.

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