Real-Time Digital Error Correction for Flash Analog-To-Digital Converter

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Abstract-- **We have designed, fabricated and successfully tested digital error-correction circuits to improve the performance of superconductive flash analog-to-digital converters (ADCs). The comparators coding the most significant bits (MSBs) are the least sensitive to the input signal, and therefore have the most threshold errors due to jitter and threshold misplacement. These errors are completely eliminated by implementing an ADC architecture using two comparators per bit, and employing logic to encode bit N by looking back to the state of the (N-1) bit. In this way, all code transitions are derived from the least significant bit (LSB) comparators. The MSB comparators are used only to encode the LSB data.**

I. Introduction

The digitization of non-repetitive signals with multi-GHz bandwidths is becoming increasingly important for commercial enterprises such as communications networks, scientific applications such as recording particle collision events, and highly developed technological applications such as digital receivers. Digitizer performance is generally limited by the analog-to-digital converter (ADC) circuitry. Although semiconducting digitizers have been operated with multi-GHz bandwidths, HYPRES' superconductive flash ADC has already demonstrated input bandwidths exceeding 10 GHz [1].

The largest reported input bandwidth of GaAs HBT ADCs currently is 3 GHz [2], with a dynamic range of 6.5 Effective Number of Bits (ENOB). GaAs HBT ADCs may ultimately be capable of a resolution of 6 effective bits at 4 GHz. In comparison, we expect our ADC to ultimately be capable of better than 7 ENOB at 10 GHz. Using the theoretical relation between the input bandwidth f and the aperture uncertainty time τ,

$$\tau = (2^N \pi f)^{-1},$$

we find this is equivalent to τ = 250 fs.

The signal is delivered to the flash ADC by an R/2R ladder (see Fig. 1) that successively divides and distributes the signal to the comparators. The comparators coding the MSBs are therefore the least sensitive to the input signal. The resulting MSB thresholds exhibit jitter and threshold misplacement leading to digital errors. This paper describes on-chip circuitry to correct these digital errors in real time using Rapid Single Flux Quantum (RSFQ) logic [3]. Experimental results will be described.

Manuscript received August 26, 1996.
This work was supported in part by the United States Department of Energy under Phase I SBIR Grant No. #DE-FG02-95ER81989.

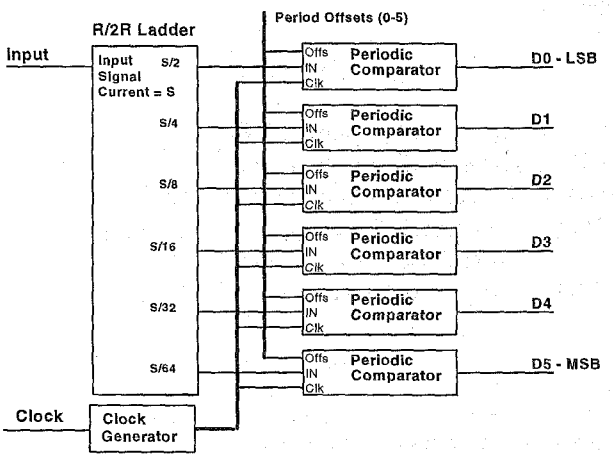


Fig. 1. The block diagram for the present ADC architecture shows each periodic comparator is driven with half the current of the previous one. The R/2R ladder allows all the periodic comparators to be identical. Only N comparators are needed, as compared to the more conventional 2^N devices in most semiconductor flash ADCs.

II. Real-Time MSB Error Correction

Coding errors arising from clock skew and threshold uncertainty reduce ADC dynamic range and increase the aperture uncertainty time. Correcting these errors is necessary to obtain full flash ADC performance. Threshold misplacement can be caused by threshold jitter and clock skew between devices. Threshold jitter primarily affects the MSB comparators because they receive the smallest analog signal from the R/2R ladder. The MSB comparators are therefore more susceptible to non-ideal threshold characteristics. Most of the clock skew has been designed out; the remaining skew can cause errors.

We propose an architectural change to correct these digital errors with the so-called Barker code [4], using a "look-back algorithm" [5,6]: In this binary-coded correction scheme, the state of the (N-1) bit is used to encode the Nth bit. Our look-back algorithm is similar to that of Ref. 6: it uses *two* comparators for each bit, with thresholds offset from each other by a 1/2 period. The state of the N-1 bit is used to select which comparator threshold of bit N is farthest away from the relevant LSB code. All code *thresholds* are determined by the LSB comparators. The MSB comparators are only used to correctly encode the LSB data. The LSB thresholds must be well placed to make this method work effectively. To ensure this, a parallel design and test effort has been undertaken to minimize dynamic comparator distortions. Our logic circuits are being designed to work with these flash ADC comparators at a clock rate of at least 20 GHz.

A. Simulation of MSB Errors and Look-Back Architecture

We simulated look-back ADC response using MathCad™ software to determine how much threshold jitter can be tolerated. The architecture for real-time error correction utilizes *two* comparators per ADC bit, except for the LSB. The look-back algorithm determines which of the A or B comparators is farthest from the code threshold, by referring to the result from the previous bit. If the previous bit is a "0"("1"), the A(B) comparator is used to encode the result.

Fig. 2 shows simulation results for a 3-bit ADC. The LSB comparator response is represented by A_0. The responses for the next bit are represented by traces A_1 and B_1. Traces A_2 and B_2 represent the comparator response for the MSB. The inputs for the two MSBs were simulated with threshold jitter, assuming a signal-to-noise ratio of 4:1. (The noise is evident near the MSB thresholds.). The results for bits 0, 1 and 2, labeled R_0, R_1 and R_2, are shown to be free of noise. Our simulations reinforced the intuitive notion that the results are noise-free as long as the threshold uncertainty is less than 1/8 of a period.

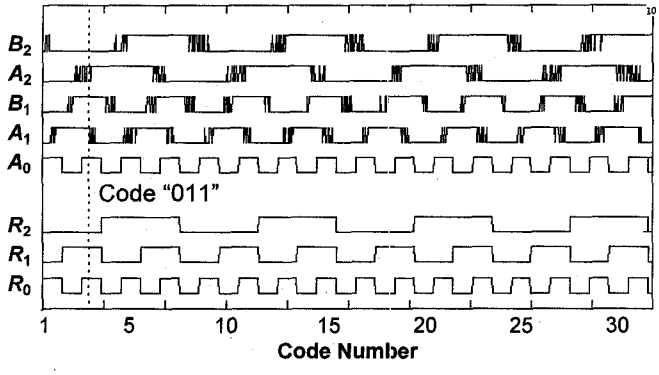


Fig. 2. Simulations of a look-back algorithm for real-time error correction such as this show that the outputs R_1 and R_2 are error-free as long as the threshold jitter is less than 1/8 of a period.

We have experimentally measured the threshold placement for a flash ADC with two comparators per bit. We find the threshold placement acceptable for the look-back algorithm. The new architecture will allow an increase in the number of effective bits by at least three, and possibly four. When this improvement is coupled with other architectural and device design changes, we should be able to reach a dynamic range of 7 effective bits at a 10 GHz input bandwidth.

B. RSFQ Implementation of the Look-Back Architecture

Anderson implemented a look-back correction algorithm in a superconducting ADC (see Ref. 6). Although his look-back circuitry was partially successful, the speed and margins of his demonstration were limited by the rather unstable Pb-alloy tunnel junction technology. The ADC and look-back circuitry in Ref. 6 could only be run up to a clock frequency of 534 Megasamples/s at three bits of resolution. HYPRES' Nb tri-layer technology could be used to implement Anderson's circuitry, but the circuits could not be clocked faster than about 2 GHz before the error rate would become unacceptable.

We choose instead to use RSFQ logic circuits , which have the demonstrated ability to be clocked at *tens of GHz.* These circuits are built with SQUIDs containing resistively-shunted Josephson junctions. Circuits can be driven with dc power, and clocked with either a sine wave or pulses. Information is stored as single flux quanta within SQUIDs. A voltage pulse is produced by one or more of these overdamped junctions each time a flux quantum enters or leaves a SQUID, thereby allowing flux quanta to be transmitted from one logic gate to another. A logic family has been assembled [7,8] allowing any logical operation to be executed.

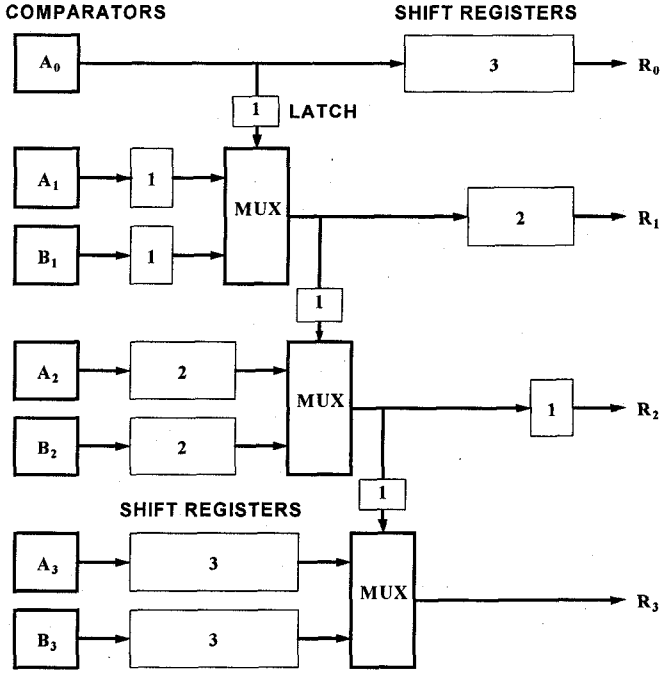


Fig. 3. This block diagram of the look-back architecture shows three bits of look-back logic. Synchronizer latches and shift registers are used to synchronize the bit streams. The number of latch elements in each shift-register stage is shown in each register block.

The implementation of the look-back circuitry is conceptually simple. As shown in Fig. 3, a multiplexer (MUX) with a control bit provides the logical function of choosing the appropriate A or B comparator. If the control datum from the previous bit is a "1" ("0"), the B (A) comparator output is sent to the output of the MUX.

There is a latch for each MUX control to guarantee control data arrive before the A and B comparator data. Input and output synchronizer latches are used to appropriately delay the data so the processed bits of each 4-bit word (R_0 ... R_3) arrive synchronously. The latency equals the number of bits.

The RSFQ look-back implementation is much simpler than that of Reference 6. Anderson's latching Josephson logic implementation was much more complicated because of the necessity of using a timed inverter. In addition, the internal

gate memory of the RSFQ logic gates such as the MUX helps to simplify the circuitry. The RSFQ implementation will also run at vastly higher speeds than its latching counterpart. Shift registers such as those proposed here have already been demonstrated to run at speeds of ~20 Gigasamples/s with good margins [9]. Several ideas for multiplexers with promising performance have been shown in the literature [10].

III. Multiplexer Design and Layout

The look-back implementation for error correction requires multiplexers, synchronizers and shift registers of synchronizer cells. The state of the art of shift register design has been extensively described in the literature. We therefore concentrate here on the design of the multiplexer, which is the important logical function for the look-back scheme. As shown in Fig. 3, the multiplexer uses the data from the previous ADC bit to choose which comparator data to pass.

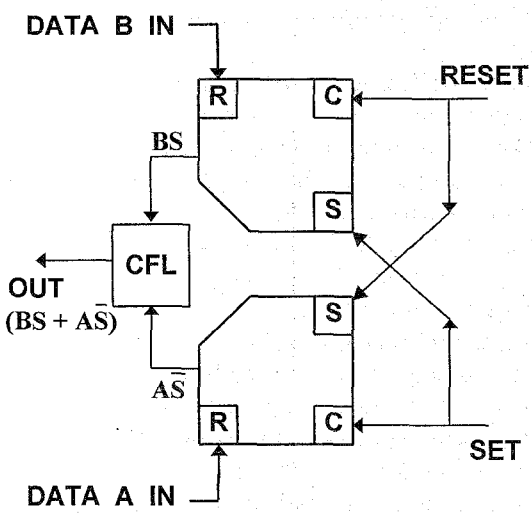
We developed a MUX based on a flip-flop called the SET/READ/CLEAR (SRC) cell, designed and implemented for another program. Its function is to pass data to the output only if SET=1, and to be cleared by a clock pulse. The SRC cell schematic looks essentially like the right or left half of the B flip-flop (see Ref. 10). The SRC cell was simulated and experimentally observed to have dc power margins of greater than ±30%. The large experimental margins suggested using two SRC cells with cross-coupled inputs as a multiplexer.

The circuit schematic, shown in Fig. 4(a), shows that when the global SET = 1, one of the SRC gates is set to allow data at the B input to be routed to the output. The other SRC gate is cleared. When RESET=1, the other gate is set to route its data to the output. A confluence buffer collects the data from each gate. The logical combination can be written BS + AS', where S' represents the complement of the SET pulse. The SRC-based MUX has no problems with simultaneous data inputs, since only one SRC gate is set to route data at a time.

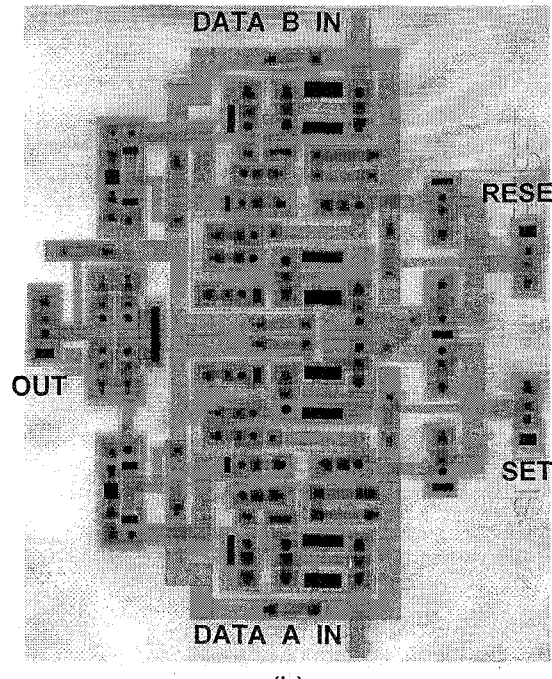
IV. Test Results

The SRC MUX was fabricated using the standard HYPRES process, except the Josephson current density (2.5 kA/cm^2) used for the flash ADC was chosen. (See the layout in Fig. 4(b).) The MUX was tested at low (~100 kHz) and intermediate speeds (up to 200 MHz). Experimental data are shown in Fig. 5. When SET=1, the data pattern for the B input port is seen in the output data stream. When SET=1, the data pattern entering the A input port is transmitted to the output.

The margins for the SRC MUX were ±18% for both A and B inputs up to a clock rate of 200 MHz, limited by the cables and connectors in this test. After a re-design, low-speed margins of ±25% were obtained. We believe this design will operate well over 10 GHz with no engineering changes, and may operate over 20 GHz. A test chip has been fabricated to allow MUX testing to proceed at clock rates up to and beyond 20 GHz. This chip uses high-speed on-chip test circuitry [11] with low-speed data input and output shift registers..



(a)



(b)

Fig. 4. (a) Schematic and (b) layout of the multiplexer based on the SRC MUX. This design requires 37 junctions and an area of 240 μm by 310 μm. This design has the advantage of delivering a correct output when the input data arrive simultaneously.

Synchronization of RSFQ pulses in the look-back ADC (see Fig. 3) is accomplished by registers of RS flip-flops. We successfully designed and tested shift registers with lengths up to 32 of these RS synchronizer cells. The bias margins of about ±20% were essentially independent of length for shift registers of 8 or greater stages, at both 1 and 2.5 kA/cm^2. The independence of these results upon length and current density demonstrates a strong design, with well-centered cell margins.

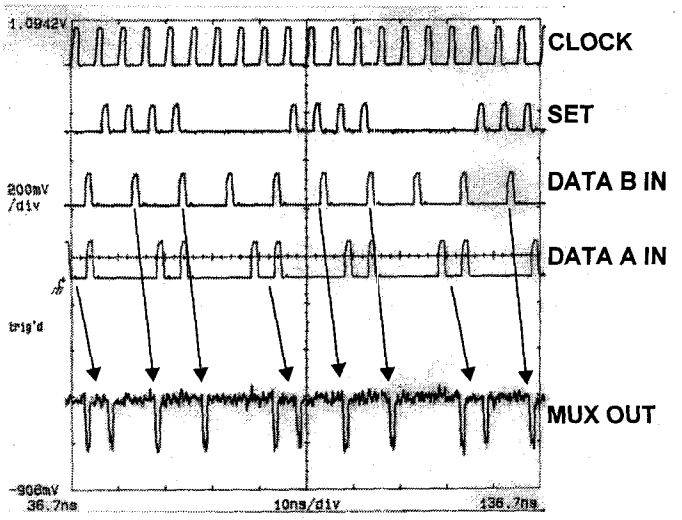


Fig. 5. This plot shows the results of testing the SRC multiplexer design at a speed of 200 MHz. The MUX outputs (amplified and inverted) correspond to DATA A(B) when the set pulses are 0(1).

IV. Discussion and Conclusion

We have designed, fabricated and tested multiplexers and synchronizers for an RSFQ look-back ADC. These circuit components already have adequate margins for real-time error correction, but will be further optimized to increase margins.

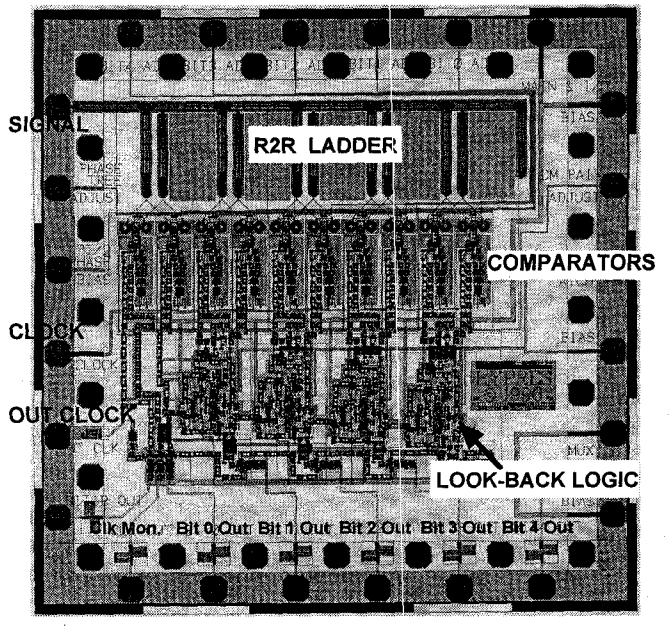


Fig. 6. This layout of a five-bit look-back ADC shows two comparators per bit, and four stages of RSFQ look-back logic.

We designed and executed a layout for a 5-bit look-back ADC with 4 stages of look-back error correction, using the SRC multiplexer and synchronizer cells described above. The layout is shown in Fig. 6.

The ADC comparator spacing is 520 μm. For each stage, the latch for the MUX control bit (originating at the previous stage) is placed adjacent to the MUX. The clock pulse runs through that latch first, before splitting and clocking the latches for the A and B comparator data bits. Then, the clock clears (resets) the MUX before clocking the synchronizer latches at the ADC outputs. All critical clock and data paths in this design were designed to attain the highest possible clock rate.

The look-back method of real-time error correction is an effective way to obtain the full potential performance of the superconductive flash ADC. Data encoding is performed by the comparator farthest away from the (LSB) code threshold. This technique removes the reliance on MSB thresholds, leading to error-free operation even in the presence of MSB threshold noise or jitter.

The look-back scheme depends on precise placement of LSB thresholds. Optimization of the look-back circuits, along with ADC architectural improvements to deliver correct LSB placement, is expected to deliver three more effective bits at a clock speed exceeding 20 GHz. This will increase the ADC high-speed dynamic range by approximately 3 effective bits.

Acknowledgment

The authors would like to thank O. Mukhanov for stimulating conversations, and D. Gaidarenko for testing support.

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