High-Speed Experimental Results for an Adhesive-Bonded Superconducting Multi-Chip Module

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***Abstract*—We report experimental results for chip-to-chip data communications on a superconducting Multi-Chip-Module (MCM) using a novel fabrication technique. The MCM was produced using a non-conductive adhesive to bond a 5-mm $\times$ 5-mm test chip to a 1-cm $\times$ 1-cm carrier. To our knowledge, this is the first time this technique was used for MCM assembly at cryogenic temperatures. The module demonstrated superior mechanical stability and protection from its environment during thermal cycling. The MCM also retained its electrical properties after multiple thermal cycling from room temperature to 4 K. We designed test circuits including various digital test benches, as well as analog test structures for bump characteristics. The superconducting circuitry successfully passed single-flux quanta at rates exceeding 50 Gbps. We measured error rates lower than 5×10^{-14} at 36 Gbps using 100-micrometer-diameter In-Sn solder bumps, and lower than 6×10^{-14} at 57 Gbps using 30-micrometer-diameter solder bumps.**

***Index Terms*—Chip-to-chip communications, cryogenic package, multi-chip module, superconducting.**

I. Introduction

THE increasing complexity of superconducting microelectronic circuits requires techniques and strategies for increasing system yield, robustness and reliability. Along with advanced fabrication techniques to increase both circuit count and circuit yield on chip, we are pursuing the option of a multi-chip package. The use of an MCM enables known good die with reduced complexity to be combined to produce a complex system. This approach for superconducting microelectronics was proposed as a 3-dimensional package [1] using a controlled collapse micro-solder reflow technique [2].

A two-dimensional package using a micro-soldered MCM was used to demonstrate Josephson latching-logic [3], with a packaging technique that enabled multi-GHz clock and data rates. The advent of Rapid Single Flux Quantum (RSFQ) circuits [4] enabled a vast increase in speed, partly because of the picosecond pulse widths of single-flux-quantum (SFQ) clock and data signals. Transmitter and receiver circuits were developed to enable chip-to-chip (C2C) communication using *passive* transmission lines (PTLs) to keep up with on-chip clock and data rates [5]–[8]. This has now been accomplished at a repetition rate of greater than 100 Gbps [9], [10].

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Nevertheless, practical Josephson systems are being developed for many applications requiring extremely robust packages. These applications include all-digital RF receivers and transceivers for deployment on platforms such as ships, motor vehicles, airplanes, and satellites [11]. The existing techniques for die attachment for superconducting MCMs are not adequate for the demanding ambient conditions these systems must endure. We have therefore developed a more robust bonding technique that makes use of a non-conductive adhesive to provide a very stable bond. This technique has been used for modules that utilize either In-Sn solder or gold-stud bonds for electrical contact between chip and carrier.

II. Motivation and Experimental Bonding Technique

A. A Limitation of Previous In-Sn Solder-Bump Packaging

Our immediate goal is to provide clock and data links between receiver front ends and subsequent digital signal-processing circuits at rates above 40 Gbps. We fabricated single-chip modules (SCMs) consisting of 5-mm $\times$ 5-mm chips bonded to 1-cm $\times$ 1-cm silicon carriers with Sn-In eutectic solder, using a well-practiced solder-reflow die-attach method [12]. We were able to obtain very impressive high-speed data with these samples, as discussed below in Section II-B.

After several thermal cycles, we cleaned the contact pads of an SCM carrier by immersing it in acetone and placing it in an ultrasonic bath. The chip immediately detached from its carrier. Solder was still attached on both the chip and carrier pads. We followed this discovery by using an ultrasonic probe to excite sound waves in another carrier. The results were similar: the chip detached. We decided that solder bumps alone enabled repeatable thermal cycling, but a robust package requires a better mechanical chip-to-carrier bond. We decided to use a non-conducting adhesive.

B. First Experiments With Solder-Bump Packaging

We designed, fabricated and tested chips containing C2C links, implemented with passive transmission lines, double-flux-quantum (DFQ) drivers [7], and appropriate receivers to reconstitute the SFQ pulses [5], [7], [9], [10].

Herr *et al.* [7] used a pseudorandom sequence generator (PRSG) and an XOR gate to test for bit errors. We used a 6-stage RSFQ PRSG and a multiple-XOR correlator array to compare the original data with the data sent through the solder bumps (see the test circuit block diagram shown in Fig. 1). The data should be nearly simultaneous in the middle-XOR

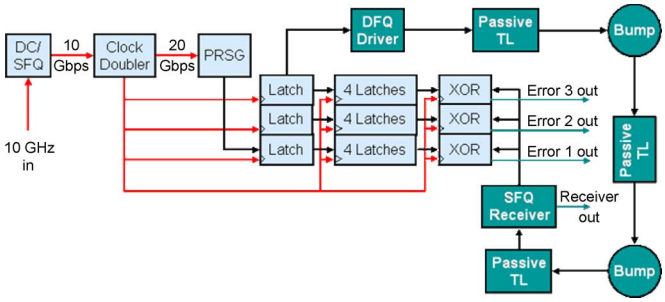

Fig. 1. This experiment compares pseudorandom data generated on chip with copies of the data returning from an off-chip excursion.

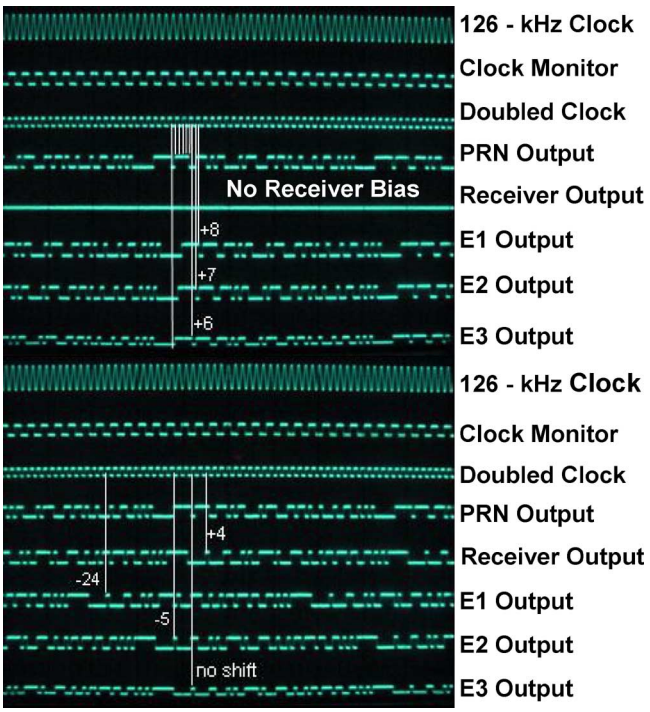

Fig. 2. These data show HYPRES' first functional test of the C2C transmitter/receiver test circuits on an SCM, using the circuit described in Fig. 1. The top traces show data for no receiver bias. The bottom traces show the change (shift) in the data when the receiver circuit's DC bias is turned on.

at a 20-GHz clock rate. At low speed, however, there is a predictable difference between the data paths. As it turns out, the PRSG generates a so-called "Gold" code. Such codes do not change under mathematical operations such as XOR; they merely shift in time. The receiver output is delayed by 4 clock tics ($4\tau_C$), and the resulting XOR outputs are:

- $E1 = XOR(4\tau_C, 7\tau_C) = 24$ clock ticks to the left
- $E2 = XOR(4\tau_C, 6\tau_C) = 5$ clock ticks to the left
- $E3 = XOR(4\tau_C, 5\tau_C) =$ no shift

The results of functional testing at 126 kbps are shown in Fig. 2. We see exactly what is mathematically predicted.

These results show we successfully transformed an SFQ data stream to voltage pulses, transmitted these pulses from chip to carrier and back to the chip, and then converted these pulses back to SFQ pulses. Although these data were taken at low speed, they show that the solder bumps have high enough bandwidth to pass RSFQ-generated data pulses without errors.

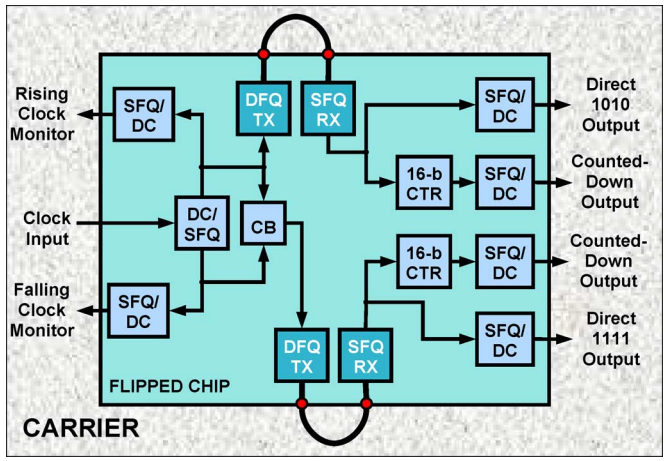

Fig. 3. This block diagram describes a high-speed C2C test module. The top two outputs toggle at the same rate as the rising edge of the clock input. A confluence buffer (CB) time-interleaves the two DC/SFQ pulse train outputs to produce a clock-doubled output. The bottom part of the circuit therefore produces outputs that toggle at twice the input clock rate. A 16-bit counter (CTR) divides down the high-speed data.

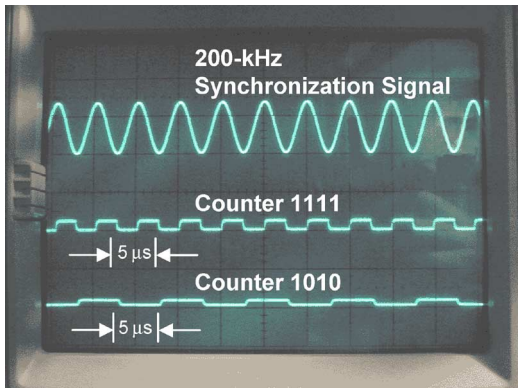

Fig. 4. This scope photo was taken using an input sine wave of 13.1072 GHz. The down-counted clock-doubled pulses are spaced by 2.5 μs, as expected. The 200-kHz 'scope synchronization waveform is also shown for comparison.

C. High-Speed Experiments With Solder-Bump Packaging

After demonstrating the pseudorandom sequence can be transmitted off- and on-chip without errors, we proceeded to design less complex test circuits containing simpler data patterns to demonstrate high-speed C2C data transmission.

Fig. 3 shows a block diagram of such a test chip. A sinusoidal input generates a train of SFQ pulses on its rising edge and another train of pulses on its falling edge. The rising edge pulse train is sent directly to a DFQ transmitter (TX). A confluence buffer (CB) combines rising and falling edge pulses to double the data rate and transport the resulting pulse train (1111...) to a DFQ transmitter.

Fig. 4 shows the operation of a 5-mm test chip on a 1-cm carrier fabricated with HYPRES' 1-kA/cm^2 process [13]. Each transmitter launches a pulse train onto a 1.6-Ω PTL, off chip through a bump, back on chip through another bump. Each pulse train is received by an SFQ receiver. At low speed, rising- and falling-edge SFQ/DC monitors are used to find the operational margins and to tune the DC bias level so the rising and falling edges are properly time-interleaved. Direct outputs

for the single (1010) and doubled (1111) pulse streams shown in Fig. 3 are observable at low speed. The down-counted data are visible only at high speed, because their toggling frequency is a factor of 2^{16} slower.

The input sine wave frequency for the data shown in Fig. 4 is 13.1072 GHz. After clock doubling, the SFQ data rate is 13.1072 Gbps (for data labeled 1010) and 26.2144 Gbps (for data labeled 1111). The top speed appears to be limited not by the bumps themselves, but by the clock-doubler circuit.

Our goal is to provide C2C data links for multi-chip digital receivers operating at clock rates of 40 to 80 Gbps. We have therefore migrated towards higher Josephson current density to increase maximum data rates. Moreover, our calculations and the work of others points to less parasitic inductance and therefore higher speed using smaller signal and ground bump geometries [10], [14].

D. Packaging Requirements

The packaging technique we are developing is intended to improve system assembly time and yield by culling known good die and permanently bonding them to the carrier.

- Chips must first be tested on a test carrier
- Chips must be demounted from the test carrier and remounted on MCM system carrier
- The adhesive used for initial chip testing must provide a strong bond while enabling rework.

E. Experimental Bonding Technique

Our packaging technique is intended to guarantee MCM integrity for operation in cryocoolers and on mobile platforms. These MCMs must withstand significant mechanical and thermal stress. We have developed a simple adhesive bonding technique that meets the criteria outlined in Section II-D.

The solder bumps were produced by dunking a carrier into a bath of liquid solder [12]. The chips were then aligned and bonded to the substrate using a Karl Suss model 150 chip bonder. A drop of adhesive was applied to the substrate just before assembly. The bumps easily pushed through the adhesive to make excellent electrical contact. After curing, epoxy shrinkage resulted in reliable electrical connection and mechanical stability. Many kinds of bumps can be used with this technique, including solder, gold studs, and polymers.

Solder bump heights were measured with a Veeco model NT1100 profilometer. We experimented with several fluxes, but our results frequently yielded bump height variations of as much as $\pm 50\%$ for 5-μm-high bumps, thereby reducing yield. More recently, we produced modules with gold stud bumps provided by Palomar Technologies. Their superior bump uniformity ($\pm 1\ \mu\mathrm{m}\ 1\sigma$) resulted in excellent electrical contact.

We experimented on re-workable modules as well as modules bonded with permanent adhesives that could not be disassembled even after weeks of soaking in solvents and hours of immersion in an ultrasonic bath.

Thermal cycling experiments were conducted for these modules in which the SCM was cycled between 4K and room temperature more than 10 times without any mechanical or electrical failure. These experiments were deliberately carried on under harsh conditions, in which the SCM was subject to moisture condensation and quick changes in temperature.

Although the re-workable adhesive method shows promise, it is difficult to removing adhesive residues. Some chips could be re-bonded, but at present, the yield is imperfect.

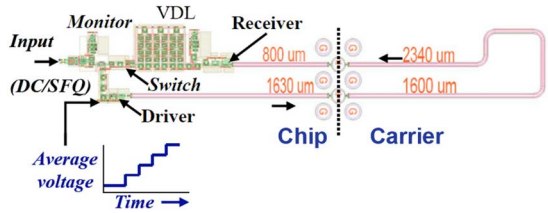

Fig. 5. This layout shows the SFQ racetrack experiment. A DC/SFQ converter produces SFQ pulses. These pulses travel through a JTL to a driver, through a PTL, through a bump to the carrier, through another PTL, back onto the chip, through an active variable delay line (VDL), and through a switch. When the switch is off, the SFQ pulses are swept out of the loop.

III. Experiments With Adhesive-Bonded Modules

In addition to the measurements described in Section II, we have most recently concentrated on a simple and elegant experiment: an SFQ racetrack similar to that described in [9].

With this technique, one monitors the average voltage while a definite number of flux quanta circumnavigates a loop. This is an excellent method of determining the maximum sustainable data rate in circuits with PTLs and C2C bump connections. We adopted this method, and designed a test chip using a target critical current density of 4.5 $\mathrm{kA/cm^2}$, and increased the DFQ matching resistor and PTL impedance to 3 Ω. We assembled the SCMs with electrical solder bump bonds and adhesive mechanical bonds. The layout is shown in Fig. 5.

The racetrack experiment enables a specific number of flux quanta to enter the loop, and to remain circulating while the switch is on. The racetrack speed can be varied by changing the bias of a variable delay line (VDL), which contains a 70-junction Josephson transmission line (JTL). The average voltage is $\mathrm{n}\Phi_0/\Delta t$, where Δt is the sum of the circuit delay (mostly in the VDL), and the time to pass through the PTL and bump transitions.

We simulated the circuit, and estimate that Δt is approximately 340 ps, or 6.1 $\mu\mathrm{V}/\Phi_0$ at nominal bias. An example of our experimental data is shown in Fig. 6. While the switch is off, there is no observed change in the average voltage. When the switch is turned on, a ramped input voltage is applied to a DC/SFQ converter. As each flux quantum is popped into the loop, the average voltage [15] increases by approximately 6 $\mu\mathrm{V}$, as expected.

Further increases in the number of flux quanta eventually results in a marked decrease in the step height, indicating a significant increase in the bit error rate (BER). Fig. 7 shows that for our module, the linearity holds up to $\sim 90\ \mu\mathrm{V}$, corresponding to a data rate of approximately 43 Gbps.

A quantitative estimate of the bit error rate can be obtained by observing how long the average voltage stays on the same voltage step. We observed a voltage of 72 $\mu\mathrm{V}$ could be sustained for more than 10 minutes, indicating that the BER is less than 5×10^{-14} at a data rate of 36 Gbps.

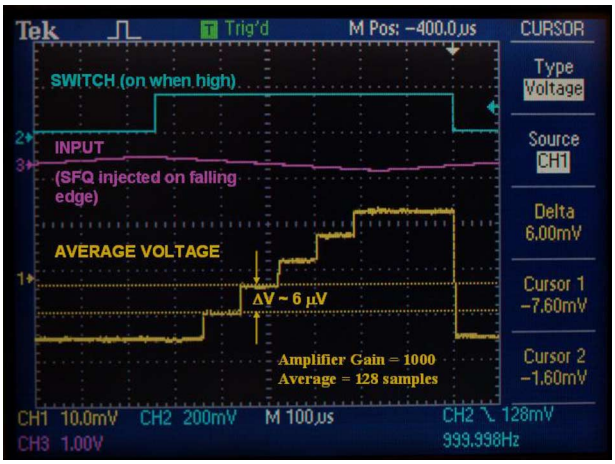

Fig. 6. These experimental data show the increase in voltage as the number of flux quanta in the racetrack loop is increased. These data were taken for nominal VDL bias.

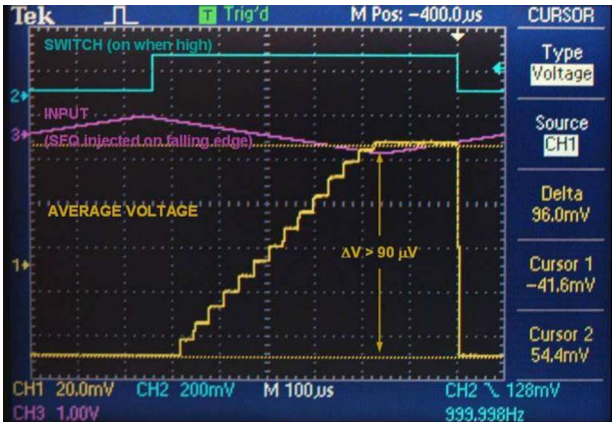

Fig. 7. The linearity of the voltage steps begins to degrade when the bit error rate becomes significant. We see here that the top data rate corresponds to $\sim 90\ \mu\mathrm{V}$, or approximately 43 GHz.

We have recently experimented with 30-μm solder bumps. with signal bumps spaced 80 μm apart and five nearest-neighbor ground bumps.

Our initial results show for $\mathrm{n} = 20\Phi_0$ the maximum sustainable voltage was 119 μV, corresponding to a maximum data rate of 57.5 Gbps. The measured BER was less than 6×10^{-14} at this data rate.

IV. Conclusion and Plans for Future Work

The mechanical bonding method we are developing satisfies the requirements we listed in Section II-D. However, we still need to increase data rate while keeping the error rate low. To that end, we have designed and are beginning to test bump geometries with more closely spaced 30-μm bumps.

The chip-immersion bump-deposition technique results in unacceptable bump-height variations. We are investigating alternative methods such as vacuum-deposited solder bumps and gold stud bumps that will guarantee better uniformity.

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[15] The voltage to be measured is amplified by an Ithaco Model 1201 low-noise preamplifier, Ithaco, Inc. PO Box 6437, Ithaca NY 14851-6437..