Decimation Filter With Improved DC Biasing and Data Transfer

Amol Inamdar, Anubhav Sahu, and Vasili Semenov

***Abstract*—Decimation filters are still the most complex and valuable superconductor digital circuits, so it is natural to use them to compare different design techniques. In the paper we discuss two new techniques. The first deals with the DC biasing scheme. For debugging purposes it is convenient to use separate power lines for different functional blocks. However, the lines occupy extra space, which could be unacceptable for a final design, when the decimation filters become part of larger circuits, for example, low-pass or band-pass ADCs. We will discuss an efficient rewiring technique that saves space during the connection of separate power lines after the circuit is debugged. The second technique is a selective use of micro-strip lines. Our solution contrasts with "extreme" recommendations for micro-strip lines as a universal tool for inter cell connections. More specifically for each connection we select either Josephson transmission or micro-strip line connection to keep the occupied area as small as possible. This highly "custom" design is possible due to parametric cell technique that dramatically accelerates the design procedure. In particular, we easily converted the circuit initially developed for 1 kA/cm2 standard HYPRES technology to the advanced technology with higher (4.5 $\mathrm{kA/cm^2}$) critical current density. The filter has 20 GHz and 40 GHz target sampling frequencies for 1kA/cm2 and 4.5 $\mathrm{kA/cm^2}$ fabrication processes respectively. The circuits are fully operational at low frequency.**

***Index Terms*—Decimation filter, RSFQ, superconductor electronics.**

I. Introduction

DECIMATION filters and ADCs with on-chip decimation filters (for example, see [1], [12]) are probably the most successful digital circuits based on RSFQ technology. This is why they serve as test beds for the development of design and measurement tools [7]–[9], [11] which then are used for many other projects in our and other groups. One of the goals of this paper is to emphasize the strong connection between our progress in design techniques and the development of better digital circuits. Of course the progress of a new technology cannot be reduced to the proper utilization of a few particular techniques, but here we will try to follow this simplified suggestion.

II. A Brief History of RSFQ Design Tools and Techniques

A. The First Steps of RSFQ Technology

The primary motivation for the development of RSFQ technology was that the clock frequency of the most popular latching logics was too low [13]. Physically this limitation was because of the long relaxation of plasma oscillations in underdumped Josephson junctions used in latching logics. It was known that so called SFQ circuits with non-hysteretic voltage-current characteristics are free of this drawback. However, these circuits were dramatically more difficult to analyse. As a result, the first suggested SFQ circuits were impractical or even incorrect mostly due to lack of proper analysis tools.

It was our good luck that in about 1981–83 we developed the COMPASS simulation package [7]. It was just in time to be used for the simulation of a substantial number of SFQ cells and pick up those with reasonably good properties. Now we believe that our simulation package was the best in the world for this particular application. In particular, it allowed us to simulate Josephson junction circuits [14] using the accurate microscopic model [8]. Probably its later revision [9] continues to be the best because even 20 years later there is no other efficient software allowing the simulation of multi-junction circuits using microscopic models for Josephson effect.

The first RSFQ circuits were laid out almost manually using AutoCAD software usually used for mechanical and architectural drawings. Definitely this design environment was sufficient only for simple circuits with one or two dozen Josephson junctions. But this was a reasonable match for the modest fabrication facilities available at that time [15].

B. The First RSFQ Circuits at Stony Brook

At Stony Brook, we had a CADENCE software package that is the best collection of CAD tools available for the semiconductor industry. One of our important steps toward design automation was the incorporation into the CADENCE environment of the now widely known LMETER program [11]. Recently we discovered that in many cases our home-made package is still a more efficient inductance extraction tool than commercially available inductance extractors.

III. 4-Bit-Slice Test Circuit

A. Data Transfer Using JTL and Micro-Strip Lines

Josephson Transmission Lines (JTLs) are the most natural candidates for data transfer between RSFQ cells.

It was assumed from the very beginning that Micro Strip Lines (MSLs) could provide much faster and more efficient data transfer between remote cells [3] (Fig. 1). Besides, MSLs dramatically simplify the wiring and therefore accelerate the design process. However, the decimation filter has a very limited real estate budget. As a result, we have been forced to carry out

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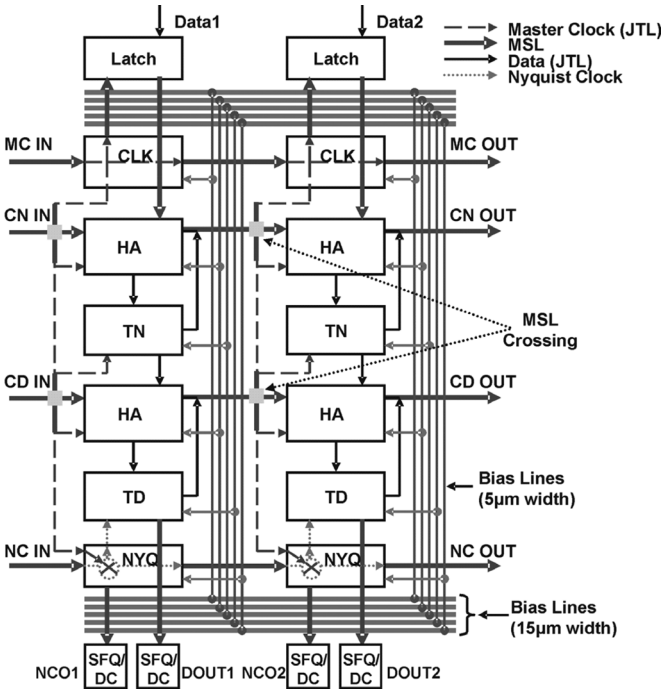

Fig. 1. Block diagram of two bit slices of the decimation filter. The micro strip lines are represented by thick lines whereas the dashed and thin lines represent JTL connections for master clock and data respectively.

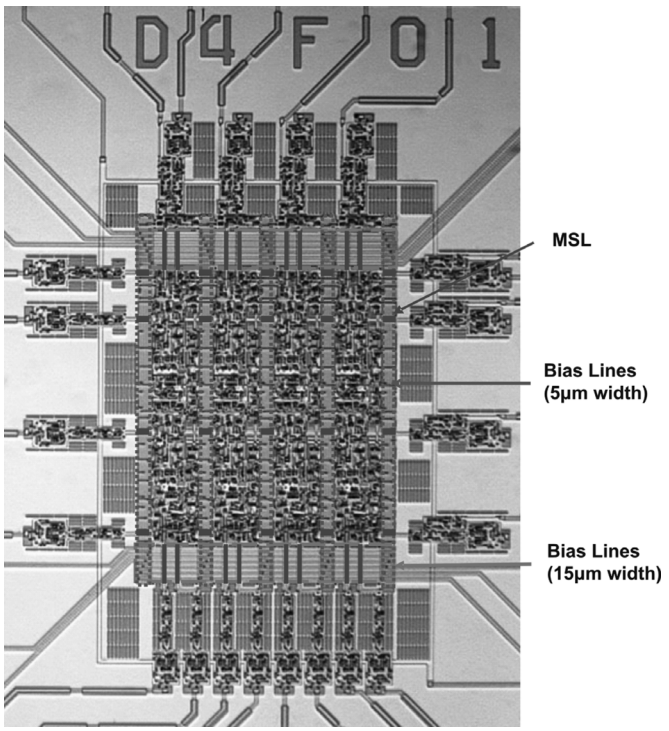

Fig. 2. Micro photograph of a test circuit with 4 bit slices of the decimation filter.

numerous and time consuming re-optimizations of schematics and layouts until the number of long connections (and therefore MSLs) is dramatically reduced. More specifically, MSLs have been left mostly for our new multi-biasing technique that requires cells to be connected with "variable" distance between them (Fig. 2).

As a result one bit slice with 4 logic cells and 3 latches contains almost equal numbers (9 and 14) of JTLs and MSLs.

B. Multi-Biasing Technique

Nominally all components of the decimation filter have been optimized for the same value of nominal bias voltage (2.6 mV). However for many reasons, it is highly impractical to feed all cells via a single bias line.

For example, a single defect could make a whole single-biased circuit completely not operational. Besides, flux trapping, design and fabrication errors could make bias margins of different parts of the circuit to be non-overlapping. In these cases different parts of the circuit would work independent of each other but not as parts of the whole device. In all these situations, an ability to individually control several bias lines allows technological problems and layout errors to be identified.

We introduced the multi-bias technique earlier [2] but now we would like to explain it in greater detail. Evidently, multiple bias lines bring some drawbacks. For example, even tracing several bias lines could be a difficult task. Besides, each line occupies some "real estate" and therefore extra lines increase the area occupied by the whole circuit. Finally each line should be sufficiently remote from magnetically sensitive RSFQ cells. Together these difficulties could and frequently do exceed the advantages of multi-bias techniques.

In our wiring technique, we resolve this contradiction as follows. We keep multiple lines only at the initial (debugging) phase of the design and then remove extra lines (thus releasing space) when the circuit is accepted as fully operational. To do so, we place individual bit-slices of the filter with some vertical gaps. These gaps are filled with the desired number (five) of vertical power lines laid out in one layer, say, M1. (Explanations for layer names can be found, for example, in [10].) All local power lines inside the slices are laid out in another layer, say, M2 and edged at vertical sides of the slices. Now we are free to extend horizontal local power lines as needed to provide connection with selected vertical power lines. We found it convenient to group functionally close local power lines into one vertical line. For example, it is natural to join power lines of timing JTLs and control important time delays by one or two power lines. Now the circuit is ready for debugging fabrication/testing runs. (The testing procedure is discussed below.)

When the test circuit operates as expected and all bias voltages are well overlapped, we can leave only one or two power lines and remove other lines. Of course to do so some minimal rewiring is needed, but it involves only small areas in the vicinity of vertical power lines. This transformation does not require any changes inside functional blocks. As we mentioned earlier, a smaller number of vertical power lines allows smaller gaps between the slices and therefore reduced circuit size. Of course this wiring approach requires that clock and data lines cross the vertical power lines. This is a perfect application for MSLs discussed above (Fig. 3).

C. Experimentation

We made several design iterations. At each iteration, we modified the previous pattern of connections between local and vertical power lines. However, due to the presented technique the

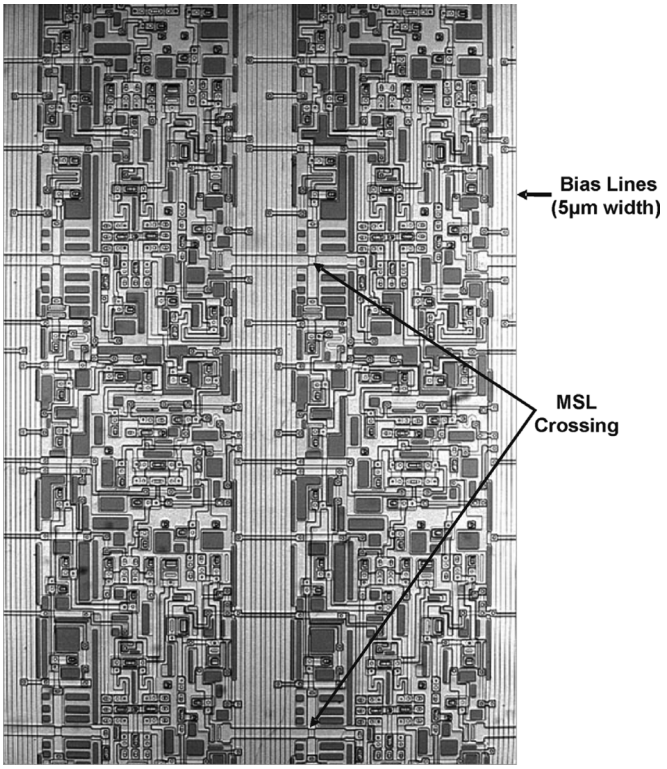

Fig. 3. Fragment of the test circuit showing 2 bit slices of the decimation filter. The crossing between horizontal and vertical micro strip lines shown correspond to that shown in the block diagram in Fig. 1.

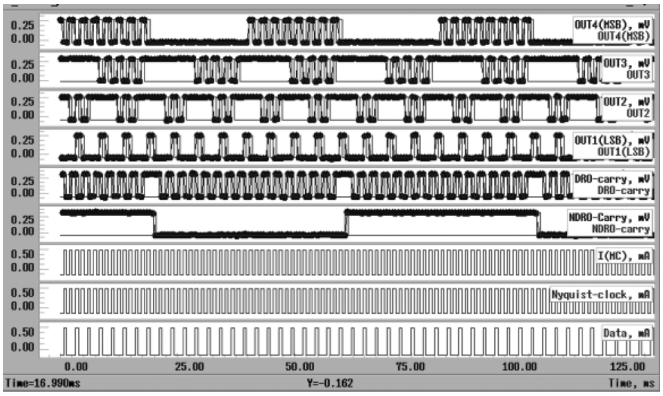

Fig. 4. Response of the test circuit on data pattern "101010. . ." applied to LSB bit and "000000. . ." patterns applied to the other bits.

iterations did not consume much design time. Fig. 4 illustrates correct operation of the filter for a simple input pattern. Bias margins (Fig. 5) were measured using a much longer pseudo-random input pattern to verify a larger number of critical combinations of data pulses. All margins are well overlapped and can be safely connected together.

The presented data have been obtained for 1 $\mathrm{kA/cm^2}$ technology. We obtained similar results for 4.5 $\mathrm{kA/cm^2}$ technology as well.

We would like to draw attention to one more problem which is specific to superconductor electronics, flux trapping [16]. Our investigations showed that almost every cell is affected by flux trapping. In most cases these individual effects are hardly noticeable but occasionally they can be significant or even fatal.

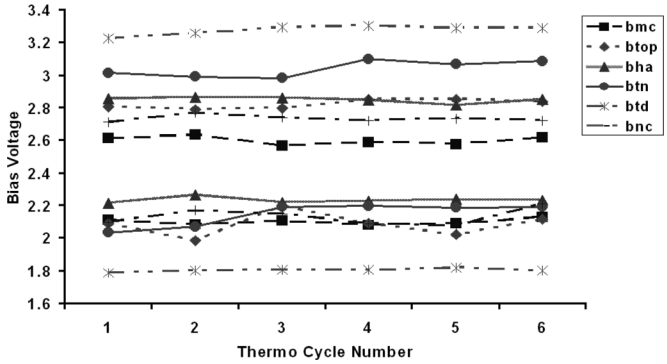

Fig. 5. Variations of bias margins with thermo-cycling.

We cannot give any reference for a theoretical analysis of the cumulative effect of flux trapping in complex circuits. As a result, measurements are the only source of important information about flux trapping in large circuits.

Fig. 5 shows lower and upper margins for each of 6 bias voltages measured after each of 6 thermo-cycles. First, let us note that almost all margins vary from cycle to cycle. We think that such variable parameter margins are common for many other investigated RSFQ circuits. In other words, a statistic of bias current margins could be as important for circuit characterization as the margins themselves.

On the positive side, the measured circuits showed that margins are well overlapped after all thermo-cycles and therefore the bias lines can now be safely unified.

IV. Conclusion

This paper contains several pieces of technical advice and observations that are either original or especially practical from our point of view. Definitely, the value of this information depends heavily on the experience of readers in superconductor circuit design. For the most advanced readers it would be sufficient to browse through the list of our observations:

We stated that bias current margins vary from thermo-cycle to thermo-cycle. This is a well known but rarely stated fact. When accepted the statement dramatically diminishes the value (and even meaning) of bias margin data that can be found in numerous papers.

The next important piece of advice is related to the trade-offs between the simplicity of the design procedure and the functional density of the circuit. One of these trade-offs is very close to the rather popular comparison of data transfer using MSL and JTL intra-chip connections. Here we demonstrated that the number of micro strip lines should be dramatically reduced if circuit size minimization is a critical design issue. The other trade-off is the number of power lines. We would like to share our technique that allows the circuit size to be reduced when the circuit is debugged and the number of power lines reduced.

The last observation is related to the importance of design software tools (Section II). Of course this discussion would be more natural for a review or invited paper. But we would like to keep it here to draw extra attention to the fact that many of the available tools are rather old and that dramatically new tools are needed for any significant progress in digital superconductor electronics to be maid.

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