Retargeting RSFQ Cells to a Submicron Fabrication Process

Darren K. Brock, Alan M. Kadin, Alex F. Kirichenko, Oleg A. Mukhanov, Saad Sarwana, John A. Vivalda, Wei Chen, and James E. Lukens

***Abstract*—There is a desire to move current state-of-the-art niobium Josephson IC fabrication processes (~3 μm) to smaller sub-micron linewidths in order to realize a decrease in gate size and increase in both speed and packing density. However, cost and time dictates that a way be found to reuse the existing RSFQ gate/cell development that has been done at the 3-μm level. Cell retargeting is the process of migrating existing designs to a new technology, with the effort focused on the maximum reuse of existing material. We have investigated a number of issues critical to this process, including both the physical and electrical aspects. Comments are made on methodologies for RSFQ cell retargeting with respect to existing reduced-linewidth JJ fabrication processes. Experimental demonstrations are shown for retargeted RSFQ static digital frequency dividers (toggle flip-flops) operating at 220 GHz, 240 GHz, and 395 GHz.**

***Index Terms*—Cell Retargeting, Cryogenic Electronics, Gigahertz Microelectronics, Rapid Single Flux Quantum Logic, Superconductor Integrated Circuits.**

I. Introduction

PROGRAMS are underway at TRW [1], SUNY Stony Brook [2], MIT Lincoln Laboratory [3], as well as HYPRES, to move towards the reliable fabrication of submicron linewidth very large scale integration (VLSI) RSFQ integrated circuits. The "scaling" of Josephson fabrication processes for RSFQ circuits has been studied [4-5]; however, less attention has been paid to the task of "retargeting". Retargeting involves the practical method of translating large numbers of existing designs for use in a new fabrication process. We have investigated two methods for moving towards this goal. Specifically, we took existing standard HYPRES 3-μm gate designs and scaled them (by factor α^{-1}) using an electrically-based retargeting methodology for fabrication in the SUNY deep submicron (DSM) Nb process with minimum junction sizes of 1.5 μm and 0.8 μm ($\alpha \approx 2$ and $\alpha \approx 4$ respectively). Simultaneously, gates were scaled from the same process for a new HYPRES self-aligned 1.75-μm process using a physically-based retargeting scheme with $\alpha \approx 2$. Section II describes the two retargeting approaches used. Section III outlines the specific gate designs used to generate Toggle Flip-Flops (TFFs) in each of the processes. Section IV reports on the successful low-speed and high-speed test of the retargeted gates. Section V summarizes our conclusions about this work.

Manuscript received September 19, 2000. This work was supported in part by Office of Naval Research grants #N00014-00-C-0024 and #N00014-99-M-0115 to HYPRES and #N00014-99-10374 to SUNY Stony Brook.

D.K. Brock, A.M. Kadin, A.F. Kirichenko, O.A. Mukhanov, and J.A. Vivalda and S. Sarwana are with HYPRES, Inc., Elmsford, NY, USA (e-mail: {brock, kadin, alex, mukhanov, johnv, sarwana}@hypres.com).

W. Chen and J.E. Lukens are with the Department of Physics, State University of New York at Stony Brook, Stony Brook, NY, USA (email: weichen@warp.physics.sunysb.edu and jlukens@notes.cc.sunysb.edu).

II. Retargeting Approaches

Two major approaches can be taken when migrating an IC cell library to a new technology. One method is to focus on the electrical (i.e. schematic/netlist) view of the cell and try to preserve this description, by making an entirely new physical layout of the gate to accommodate the smaller linewidth fabrication process. According to scaling theory [5], this means keeping inductances, critical currents, and McCumber parameter fixed, while scaling junction areas, along with the length and width of resistor and inductors. The other method is to try to minimize changes to the relative geometric properties of the cell; instead, scaling the new fabrication process to meet desired circuit specifications, then re-simulating the electrical characteristics of the gates to verify acceptable performance.

Each method has its advantages. While better packing density can be attained using the electrically-based (EB) scaling approach, quicker (and more readily automated) results stem from a physically-based (PB) scaling approach. A realistic tactic to the task of retargeting inevitably includes aspects of both approaches. In the sections below, we show the results of a combination of these approaches, involving gates scaled for a smaller device process, as well as for a entirely new process. The methodologies discussed in the following sections apply to areal junction sizes $>\approx 0.3\ \mu m^2$ ($\alpha <\approx 6$), where external resistive shunts are included across junctions in layout to ensure the non-hysteretic behavior necessary for RSFQ logic.

A. Electrically-based Cell Retargeting

Electrically-based (EB) retargeting is tantamount to designing from scratch. Although existing gate designs can be used, the physical layout must be completely redone. EB retargeting is the ideal—where gates are physically described

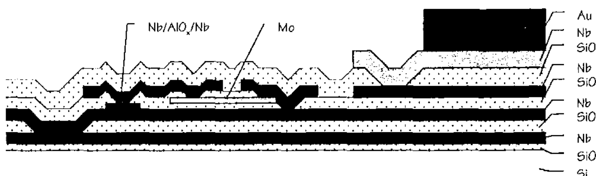

Fig. 1. The HYPRES 3.0-μm standard 10-level Nb/AlO$_x$/Nb IC process contains 4 superconductor metal (Nb) layers for wiring, a junction definition layer, a resistor layer (Mo), 3 vias to contact the metals, and a Au layer for the chip contacts.

1051-8223/01$10.00 © 2001 IEEE

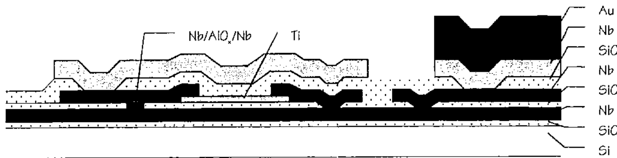

Fig. 2. The SUNY DSM CMP 8-level Nb/AlOx/Nb IC fabrication process contains 3 superconductor metal (Nb) layers for interconnect, a junction definition layer, a resistor layer, 2 vias to contact the metals, and an Au layer for chip contacts.

in the target fabrication process, the parasitic circuit parameters extracted and the gate re-simulated to confirm satisfactory operation (margins, etc.). This involves the building of a complete cell library containing common building blocks such as I/O gates, devices, JTLs, etc.

Fig. 1 shows a cross-section of the standard HYPRES 3-µm Josephson fabrication process [7]. A substantial number of RSFQ gates have been designed and optimized for this process. Fig. 2 shows a cross-section of the first target process for this work – the DSM Josephson fabrication process of SUNY at Stony Brook [2]. This process has been successfully demonstrated for junction sizes down to 0.25 µm x 0.25 µm [8].

Our method used a combination of optically-defined and electron-beam lithography. By pre-designating two or three areas per chip (~250 µm^2) and pre-wiring all I/O's to these regions, the same optical masks can be re-used to pattern the chip pads and coarse wiring for all lots. Individual digital GDS-II files corresponding to each test field are then directly loaded to the e-beam writer for exposure on the wafer. This method has the advantage of quick (and inexpensive) fabrication iteration, but has the disadvantages of very low throughput (due to e-beam exposure), substantial time spent in layout, and little flexibility in experimental configuration.

B. *Physically-based Cell Retargeting*

When translated into VLSI complexity, an EB retargeting methodology involves a substantial investment, in both time and money. One alternative is to achieve the performance accompanied with EB scaling by basing new gates on the existing layouts. A (PB) retargeting methodology seeks to tailor the target process to accommodate the existing physical cell layout as much as possible. This approach forms the basis for a new 1.75-µm self-aligned process at HYPRES utilizing Chemical Mechanical Polishing (CMP) (see Fig. 3). All levels in this process share lithographic masks with the standard 3.0-µm device process. The resulting resistively shunted junction resembles a standard HYPRES junction upside down, with ground plane on top.

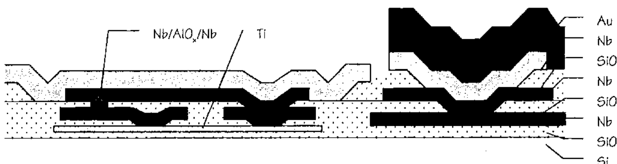

Fig. 3. The HYPRES 1.75-µm CMP 9-level Nb/AlO$_x$/Nb IC fabrication process contains 3 superconductor metal (Nb) layers for interconnect, a device definition layer for the Josephson junctions, a resistor layer (Ti), 3 vias to contact the different wire layers, and an Au layer for the chip contacts.

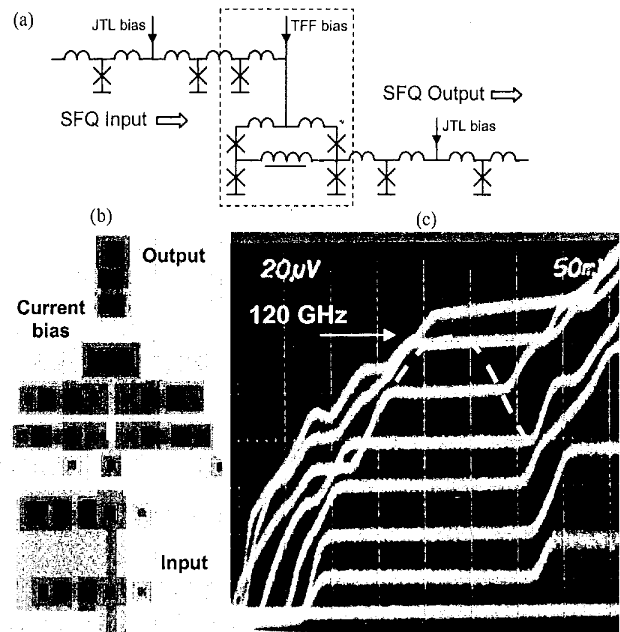

Fig. 4. Reference cell under study – (a) Circuit schematic, (b) physical layout, and (c) measurement of operating margin vs. frequency showing narrowing region (Vert. Axis is 20 GHz/div.)

This is possible because the minimum mask feature size ~ 2.0 µm (formerly used to define the via to contact the top of the JJ) is now used to define the junction itself. Moreover, in this case, this minimum size can be reduced to 1.75 µm because no via-to-junction alignment is necessary.

III. Prototype Gate Designs

The schematic, layout, and test data in Fig. 4 define the reference gate. This 3.0 µm RSFQ TFF is a typical gate fabricated in the HYPRES 1 kA/cm^2 process. It operates up to 120 GHz. This cell was retargeted to the new HYPRES self-aligned 1.75-µm process using a critical current density of 5 kA/cm^2. Beginning with the existing design, several layer translations can be made to existing physical layouts. The only process changes necessary are to split the wafer lot twice – once to grow a thinner tunnel barrier layer and do CMP, and once to deposit a slightly lower conductance Ti resistor layer (~ 2 Ω/sq.). Otherwise, the steps are identical to the standard process. Fig. 5 shows a mask layout and photomicrograph of the retargeted T flip-flop. Note the lack

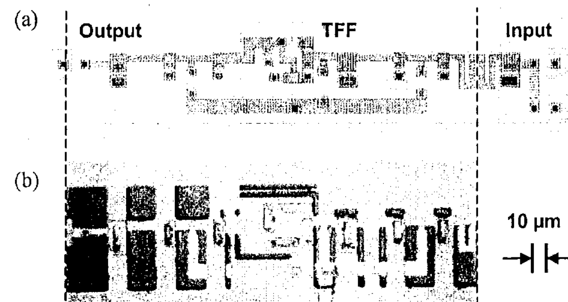

Fig. 5. (a) Mask layout for a TFF in the 1.75-µm self-aligned process and (b) a photomicrograph of the fabricated gate. Note the absence of some features due to the planarization step.

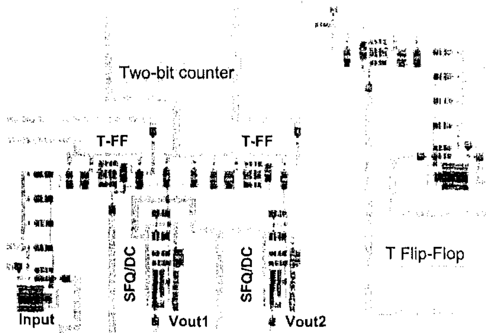

Fig. 6. E-beam field layout for SUNY fabrication process using 1.5-μm, 6 kA/cm^2 junctions. A 2-bit ripple counter is shown on the left, with dc/SFQ taps for measuring each stage. A single TFF is on the right.

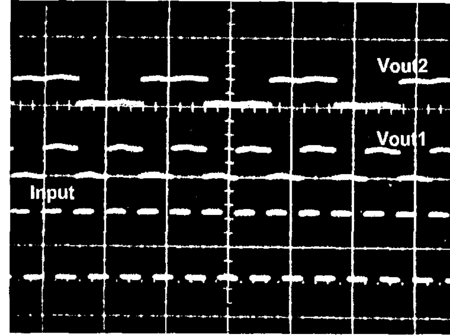

Fig. 8. Low-speed test results of a 2-bit ripple counter (fabricated with 1.5-μm 6 kA/cm^2 junctions in the SUNY process) show correct operation at each stage. The circuit contains over 50 junctions (Vert. axis = 1 mV/div.) All data is in non-return-to-zero (NRZ) format.

of features in the photo compared to the mask layout. This is due to the CMP step. After the translation of layers, the parasitics were re-extracted and the circuit performance verified in simulation. Simultaneously, the same gate was migrated to the SUNY process (Fig. 2), using a minimum junction size of 1.5 μm and a critical current density of 6 kA/cm^2. The mask layouts for a 2-bit binary ripple counter, as well as a single TFF are shown in Fig. 6. Using this 1.5-μm design as a reference, the 0.8-μm design was then directly generated by only scaling the geometry of the junctions and shunt resistors. All other interconnect wiring and geometries were kept fixed and the cell margins were confirmed via simulation.

IV. Circuit Evaluation

All the circuits described in section III have been successful tested at both low-speed (for functionality) and at high-speed (to determine degradation of operating margins with speed and maximum frequency of operation).

A. Low-speed Measurement

After screening chips for junction continuity and appropriate critical current density, circuits were measured at low-speed. As an example, Fig. 8 shows the functional test of the 2-bit RSFQ binary ripple counter of Fig. 6 fabricated at SUNY with 1.5 μm, 6 kA/cm^2 junctions. This circuit contains more than 50 Josephson junctions. Designs were fitted with both dc/SFQ converters for synchronous (low-speed) input testing, as well as single JJs for asynchronous (high-speed) input generation. Once stable operating bias current regions were determined, the input trigger frequency was increased until the maximum speed of the dc/SFQ input stage was reached. Input was then switched to an over-biased junction to create a stream of input SFQ pulses (bits) for additional measurement.

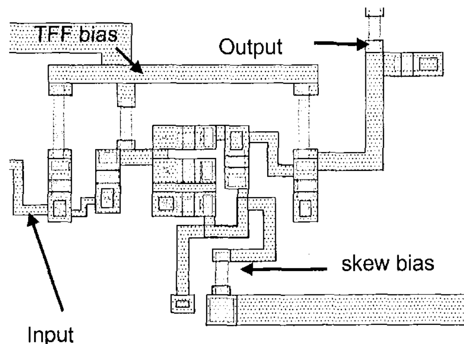

Fig. 7. This layout for the 0.8-μm TFF was directly scaled from the 1.5 μm layout in the same process. The only necessary layout changes were to scale the junction areas and shunt resistors.

B. High-speed Measurement

RSFQ circuits are unique in the field of ultrafast digital electronics because they offer a facility for direct measurement of digital data at microwave frequencies. In most technologies this is simply not possible without resorting to a significant amount of on-chip test circuitry (demux, FIFO registers, etc.) However, in the high-speed testing of RSFQ TFFs configured as digital frequency dividers (DFDs), it is common to perform a "time-averaged voltage" (TAV) measurement to characterize high-frequency operation. This method relies on the fact that, when the data bits are single quanta of magnetic flux Φ_0. (as in RSFQ logic) the Josephson frequency-to-voltage relation [9] sets $\langle V_{\mathrm{in/out}} \rangle = f_{\mathrm{in/out}} \cdot \Phi_0$ [bits/second], where $\Phi_0 \approx 2.07$ mVps. Moreover, this test can be extended to provide additional

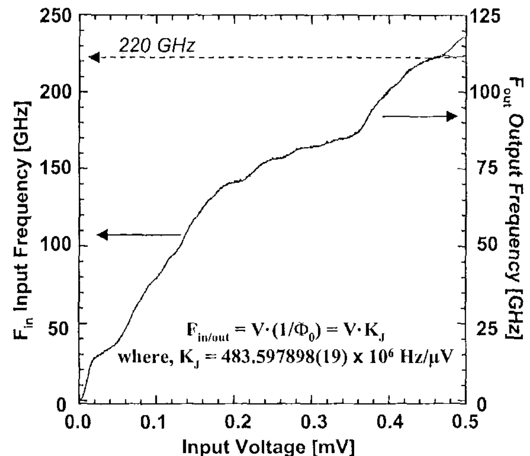

Fig. 9. A plot of the time-averaged input voltage and twice the time-averaged output voltage vs. input frequency using the Josephson frequency-to-voltage relation. of the input and output of the digital frequency divider

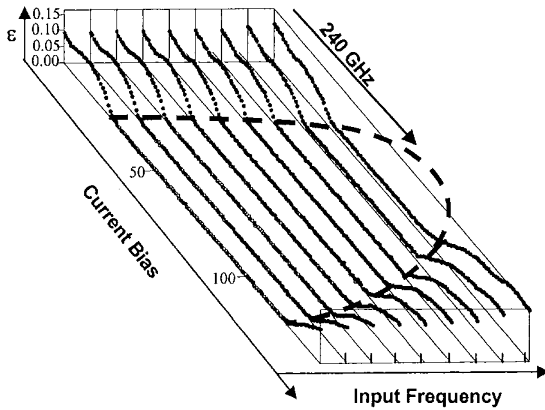

Fig. 10. Constant-frequency curves showing operating margin vs. division error for the 1.5-μm DFD. Maximum operational frequency is defined as the point where the margin shrinks to zero, the lower of the two, in this case 240 GHz.

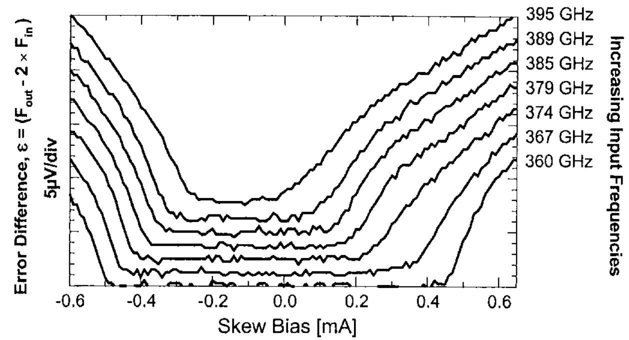

Fig. 11. Constant frequency plots for a 0.8-μm DFD. Plots are offset for clarity. Flat region indicates the size of the dc bias margin of the gate. Highest frequency of operation before a measurable error rate is 395 GHz. Bias margin is constant for all frequencies below those plotted.

information about the highest frequencies of operation. By measuring the operating margins of the dc current bias of the gate as a function of operating frequency (as in Fig. 4) the TAV measurement can be unambiguously demonstrated as a consequence of the intended dynamics of the RSFQ T flip-flop gate.

For the high-frequency characterization of these circuits, all data were collected using an Octopux automated test and measurement station [10]. Fig. 9 shows TAV curves of the 1.75-μm TFF demonstrating correct static digital frequency divider operation up to an input frequency of 220 GHz. Fig. 10 shows the operation of the 1.5-μm DFD operating up to an input frequency of 240 GHz. Each line represents the difference $\varepsilon = (f_{\mathrm{in}} - 2f_{\mathrm{out}})$ for a single operating frequency. This point (240 GHz) is indicated on Fig. 10 for clarity.

A similar group of margin curves for the 0.8-μm DFD are shown in Fig. 11. The maximum operating frequency obtained was 395 GHz. The layout for this gate was corrected with respect to the additional voltage tap to sense operation frequency. Therefore, the corresponding values of frequency for each trace are given at the side of Fig. 11. The traces have also been offset for clarity.

V. Conclusions

Although an electrically-based retargeting methodology is clearly needed to achieve the gate density potential of a submicron RSFQ process, a physically-based approach can offer significant gains in terms of speed, with a substantially lower level of cost/effort. We have used an existing 3.0 μm RSFQ TFF design (schematic and layout), with a maximum demonstrated operating speed of 120 GHz, as a reference for retargeting to smaller linewidth fabrication technologies. An electrically-based retargeting methodology resulted in cells operating at 240 and 395 GHz for scaling coefficients $\alpha \approx 2$ and $\alpha \approx 4$ respectively. A physically-based retargeting methodology resulted in gates operating at 220 GHz for $\alpha \approx 2$. These results are generally consistent with circuit speed increasing as α^1 [5].

The e-beam lithography process at SUNY affords rapid turnaround in the development of new gates with submicron dimensions, while the self-aligned process being developed at HYPRES is better suited for producing VLSI chips.

VI. Acknowledgment

Special thanks to R. Patt, R. Hunt, and M. Brandt of HYPRES as well as to S. Tolpygo of SUNY Stony Brook for advice in the design and fabrication of the sample chips.

References

[1] L.A. Abelson, R.N. Elmadjian, and G.L. Kerber, "Next generation Nb superconductor integrated circuit process," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 3228-3231, Jun. 1999.

[2] V. Patel and J.E. Lukens, "Self-shunted Nb/AlO$_x$/Nb Josephson junctions," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 3247-3250, Jun. 1999.

[3] K.K. Berggren, E.M. Macedo, D.A. Feld, and J.P. Sage, "Low T_c superconductive circuits fabricated on 150-mm wafers using a doubly planarized Nb/AlO$_x$/Nb process," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 3271-3274, Jun. 1999.

[4] K.K. Likharev, "Superconductor devices for ultrafast computing," in H. Weinstock, ed., Applications of Superconductivity, Dordrecht, Kluwer Acad. Pub., 2000.

[5] A.M. Kadin, C.A. Mancini, M.J. Feldman, and D.K. Brock, "Can RSFQ logic circuits be scaled to deep submicron junctions?" paper 4EL02, *this conference*.

[6] P. Stein, "A methodology to retarget designs using formal verification," *Gov. Microcir. App. Conf. Dig. Pap.* vol. 24 pp. 176-179, Mar. 1999.

[7] L.S. Yu, C.J. Berry, R.E. Drake, K. Li, R.M. Patt, M. Radparvar, S.R. Whiteley, and S.M. Faris, "An all-niobium eight level process for small and medium scale applications," *IEEE Trans. Mag.*, vol 23, pp. 1476-1479, March 1987; see also HYPRES Nb Process Design Rules, [online] http://www.hypres.com/.

[8] W. Chen, A.V. Rylyakov, V. Patel, J.E. Lukens, and K.K. Likharev, "Rapid single flux quantum T-flip-flop operating up to 770 GHz," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 3212-3215, June 1999.

[9] See e.g. A.M. Kadin, Introduction to Superconducting Circuits, New York: John Wiley, 1999.

[10] D. Zinoviev and Y. Polyakov, "Octopux: An advanced automated setup for testing superconductor circuits," *IEEE Trans. Appl. Supercond.* vol. 7, pp. 3240-3243, Jun. 1997.