Multi-band Digital-RF Receiver

Saad Sarwana, Dmitri E. Kirichenko, Vladimir V. Dotsenko, Alexander F. Kirichenko, Steven B. Kaplan *Senior Member IEEE*, and Deepnarayan Gupta *Senior Member IEEE*

***Abstract*— A software radio receiver that can be programmed to operate in multiple wide frequency bands is required for many communication and intelligence applications. We have designed a variety of multi-band receivers, comprising a set of band-specific analog-to-digital converters (ADCs) for direct digitization of RF bands and a digital switch matrix for band selection, in two flavors: as a single superconductor integrated circuit chip and also as a multi-chip module. In addition to the ADCs and the switch, these include a 1:16 deserializer and output drivers to facilitate transport of the digitized RF data to room temperature electronics for further processing and analysis. In the single IC flavor, up to four bandpass delta-sigma ADCs minimizing quantization noise in their respective bands were integrated on the same chip and operated at clock rates up to 20 GHz. In the multi-chip module (MCM) implementation, a 1-cm × 1-cm universal active carrier was designed to accommodate any two 2.5-mm × 2.5-mm flipped chips, each containing a single ADC front-end. This standardized approach facilitates customization of two-band ADCs by selecting from a growing library of ADC front-ends, which currently cover bands ranging from HF (0-30 MHz) to Ka-band (20-21 GHz). These Multi-band MCMs and single chip ADC's were fabricated, assembled and tested.**

***Index Terms*— Satellite communication, Digital radio, Sigma-delta modulation, Cryogenic electronics.**

I. INTRODUCTION

THE radio frequency (RF) spectrum is a precious resource. Wideband spectrum monitoring, coupled with the ability to zoom in on narrower sub-bands, is critical for control and dominance over the RF spectrum. The digital-RF channelizing receiver architecture [1], with high-fidelity superconductor analog-to-digital converters (ADCs), lends itself naturally to reception of multiple relatively wide (e.g. 1 GHz) bands across the RF spectrum. Once in the digital domain, the RF signal may be copied without loss and distributed to multiple simultaneous, independent signal processing paths. In other words, while one copy is used to monitor a wide RF spectrum, another copy may be subdivided into communication channels.

Bandpass Delta-Sigma ADCs are tuned to minimize quantization noise at a target RF band [2],[3]. Depending on the application, one can either get continuous spectral coverage with a bank of contiguous bandpass ADCs or select a set of disjoint frequency bands-of-interest to accomplish a specific function. For example, consider a satellite communication system that simultaneously operates over multiple bands (e.g. C, X, Ku, and Ka). A single multi-band receive terminal, equipped with a bank of appropriate ADCs, will be able to receive different bands from the same satellite (such as the wideband global SATCOM (WGS) system), or from different satellites with an appropriate antenna subsystem. A key component of the multi-band, receiver architecture is a digital-RF switch matrix [4] [5]. The rapidly programmable asynchronous switch matrix distributes (within a few clock cycles, less than 100 ps, if necessary) each input, comprising one or more digitized data bit-streams from an ADC along with its own sampling clock, to one or more outputs leading to independent digital signal processing chains. Fig. 1 shows a multi-band digital-RF receiver block diagram showing examples of different functions that may be performed [6]. For simplicity, each RF band is shown as originating from an antenna and being applied to a single ADC. In most applications, there will be some form of analog processing (e.g. filtering) before digitization.

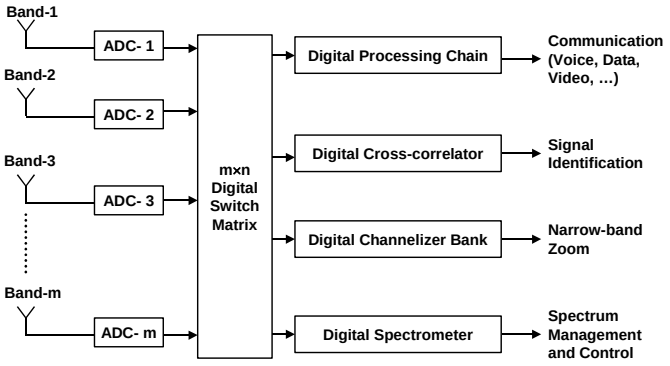

Fig. 1 Block diagram depicting the digital-RF receiver concept, which uniquely incorporates RF distribution. The analog RF inputs are directly digitized with a set of analog-to-digital converters (ADCs), paving the way for the remaining signal processing functions to be performed entirely in the digital domain.

In this paper, we present results for a possible implementation of this Digital-RF receiver architecture, using two or more band-specific superconductor ADCs connected via a switch matrix. With the objective of demonstrating modularity and multi-band capability, the complexity of superconductor digital electronics was kept at a minimum. In most cases, the switch matrix had only one output, which was deserialized (by a factor of 16) on chip and transferred to room-temperature for further processing. To demonstrate chip operation, we acquired the digitized data and performed power spectral density calculations; other real-time data processing could be performed using an FPGA at room temperature. Also, only single-bit ADC front-ends were used to minimize

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The authors are with HYPRES, Inc Elmsford, NY 10523 USA (phone: 914-592-1190; fax: 914-347-2239; e-mail: sarwana@hypres.com).

the total data throughput. The scalability of the switch matrix has been previously proven for multiple outputs and multi-bit data inputs [5].

II. Two Band Integrated Superconductor Electronics Receiver

We designed and tested a version of the multi-band chip covering two disjoint bands: a low pass (LP) HF/VHF front end and a band-pass (BP) 800 MHz front end. The chip also contained a 2x2 switch matrix and two sets of deserializers (top and bottom) for data processing. The block diagram and the photo of this chip are shown in Fig. 2 and a description of its operation and functionality can be found in [5].

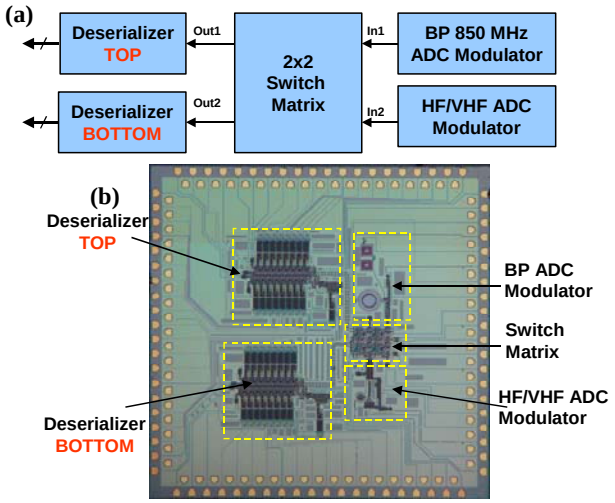

Fig. 2 (a) Block diagram and (b) photograph of a multi-band ADC test chip with 2x2 switch matrix and two 1:16 deserializers.

This chip allowed us to check all modes of operation of the switch matrix. In the broadcast mode, digitized data from either BP or LP front end is copied to both deserializers. In the cross (bar) mode, the BP and the LP outputs are routed to the bottom (top) and the top (bottom) deserializers respectively.

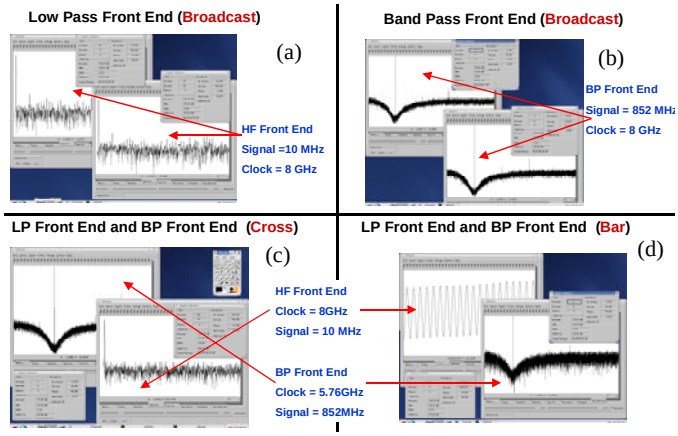

Fig. 3 Test Results for lowpass and 850 MHz bandpass front-ends with two deserializers integrated on the same chip. (a) The same 10 MHz CW on HF front-end broadcast to both deserializers). (b) The same 852 MHz CW applied to BP front-end broadcast to both deserializers. (c),(d) Different 10 MHz and 852 MHz CW applied to the different front ends routed to the two different deserializers (showing the switch matrix cross and bar operation).

We even clocked both front ends at different frequencies of 5.76GHz/8GHz to demonstrate that two asynchronous clocks can be supported at the same time. Test results for all four possible modes of operation are shown in Fig. 3.

A similar chip with ADC Front Ends covering X (7.5 GHz) and Ka (20 GHz) bands was also designed and tested at a 20 GHz sampling frequency.

III. Four Band Integrated Superconductor Electronics Receiver

We also designed versions of the multi-band receiver using four ADC front ends, a 4x1 switch matrix and one 1:16 deserializer. The bands were chosen to be either contiguous in the 9-13 GHz range or be disjoint, for example, covering bands around 850 MHz, 4 GHz, 7.5 GHz and 12 GHz. The chip photo of such a generic four-band chip is shown in Fig. 4. The user can route any of the four ADC front-end digital outputs to the deserializer, depending on the address loaded in the switch matrix.

Acquired spectra from four ADCs covering the 9-13 GHz range are overlapped in Fig. 5. To obtain the best coverage of the band we designed front ends with slightly modified null positions. We then fabricated the four-band chip, measured the null frequencies experimentally, and “tuned” the null positions slightly, via physical trimming, to spread the nulls equally in the band of interest.

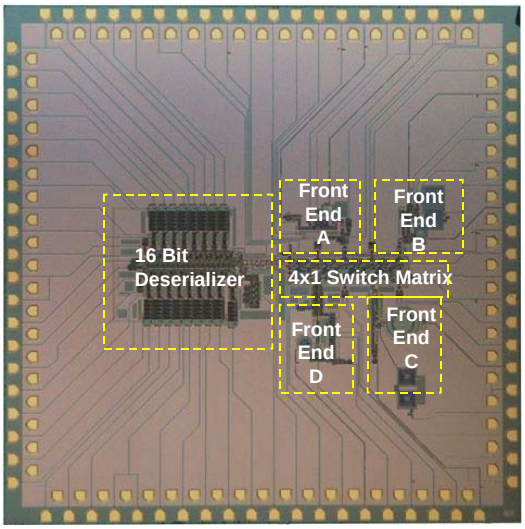

Fig. 4 A four-band 1 cm^2 ADC Chip. The four front-ends, labeled [A], [B], [C], and [D], can either be in disjoint bands or be closer together to monitor a more contiguous spectrum range.

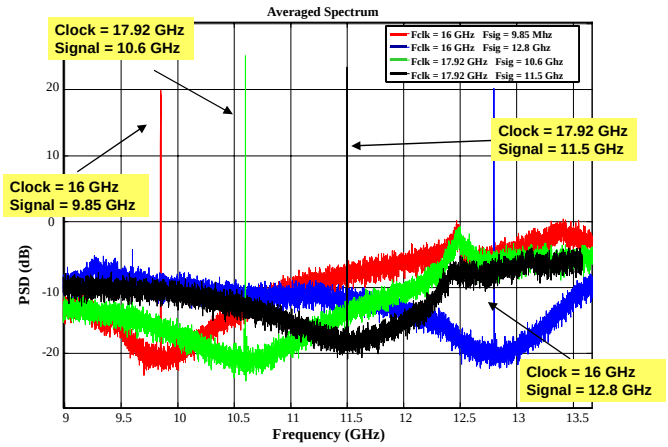

Fig. 5 Ovelapping spectra from four bandpass front ends

Fig. 6 shows the spectra obtained from testing a multi-band ADC chip with four front-ends with center frequencies spanning an order of magnitude. As expected, these spectra show that the null depth is inversely proportional to the center frequency, approximately following a 6 dB/octave trend. The higher frequency signals are more susceptible to timing jitter as well as to the meta-stability in the Delta-Sigma comparator. The null depth also increases with sampling clock frequency but that dependence has not been fully studied.

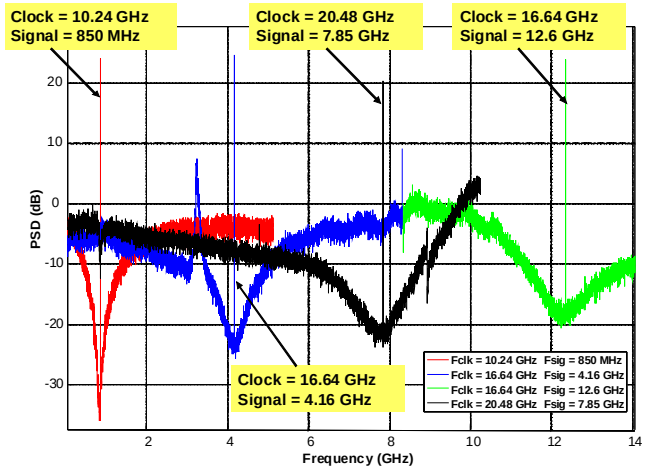

Fig. 6 Spectra obtained from four bandpass ADCs on the same chip.

IV. Multi-Chip Superconductor Electronics Receiver

This modular approach to multi-band ADC design is extremely amenable to extending to a multi-chip architecture. The individual components are well defined and can be placed on separate chips and then integrated into a complete receiver using the flip chip process. For test purposes, we built a universal receiver multi-chip module (MCM) as shown in Fig. 7. The MCM consists of an active carrier hosting a 2×1 switch matrix and a 1:16 deserializer. Any of the band-specific single-bit ADC front ends can be made on a 2.5 mm × 2.5 mm chip and any two such chips can then be flipped on a 10 mm × 10 mm active carrier.

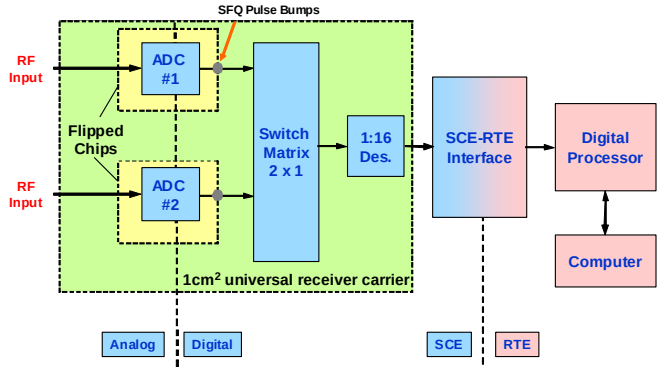

Fig. 7 A block diagram of Multi Band ADC Chip and Test Configuration

There are many implementation techniques for chip-to-chip communication in RSFQ based multi-chip modules [7]-[9]. For our chip, we used MCM DFQ drivers and receivers developed in [7], and an epoxy based MCM bonding technique which has been experimentally verified to work at >50 GHz in [9]. A photo of our test chip, with multiple flipped chips creating a multi-band multi-chip receiver, is shown in Fig. 8(a). It should be noted that HYPRES has developed a wafer bumping techniques which provide >100 GHz data links between chips [10] and we plan to transition the designs to this process in the future.

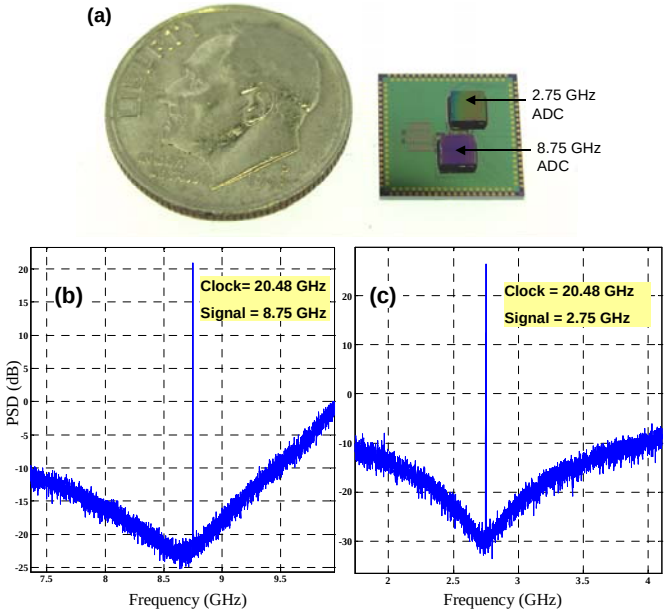

Fig. 8 (a) Chip photo of a bonded two chip multi-band MCM receiver. Signal Spectra from (b) 8.75 GHz ADC and (c) 2.75 GHz ADC front ends.

A version of this MCM with a 2.75 GHz and an 8.75 GHz band pass front-ends was bumped, bonded, tested, and shown to be completely operational at clock speeds up to 20.48 GHz. The resulting spectra are shown in Fig. 8(b) and (c).

This modular MCM approach to multi-band ADC design allows even further benefits when transitioning to a different J_c fabrication process. A multi-J_c MCM integration approach as described in [11] can be adopted so that not all chips used in the receiver have the same critical current density. For example, a higher speed fabrication process (e.g. 20 kA/cm^2) can be used to fabricate the flipped ADC front-ends (the higher J_c enables higher sampling rate and lower jitter, resulting in better ADC front end performance). The oversampled data then can be communicated via the MCM to a more mature lower-J_c process (e.g. 4.5 kA/cm^2) for further data processing. This would enable a faster turn-around time as only the front ends would need to be redesigned for the new process. It would also allow us to capture all the benefits of the higher J_c process while minimizing the impact of low yield which is inherent in any new process.

V. Conclusion

Multi-band digital-RF receivers are useful for a variety of applications in communication and RF spectrum monitoring. We have reported successful integration of multiple ADCs on a single chip and as a multi-chip module. The modular design approach permits selection from a library of ADC front-ends, which continues to grow, and facilitates production of customized multi-band ADCs. The use of a mass-produced common carrier, supporting small-customized ADC front-end chips, also reduces the overall development cost.

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