Modular, Multi-function Digital-RF Receiver Systems

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***Abstract*— Superconductor digital receiver systems of increasing functionality, modularity and user-friendliness have been developed. The modular design methodology ensures that within its input-output and heat load capacity, the system can be reconfigured to perform a different function by changing the chip module and by reprogramming FPGA-based digital signal processors. One of the systems (ADR-004), originally equipped with a 10×10 mm^2 channelizing receiver chip for signals intelligence application, was reconfigured with a 5×5 mm^2 1.1-GHz bandpass ADC chip to perform world's first multi-net Link-16 demonstration in a setting capable of operational use. Substantial improvements in system integration have been obtained in each successive generation of digital-RF receiver systems. The latest (third) generation system (ADR-005), hosting a 5×5 mm^2 7.5-GHz bandpass ADC chip and an FPGA channelizer, successfully repeated the over-the-air SATCOM demonstration performed previously using a 1-cm^2 single-chip bandpass digital receiver with an on-chip superconductor channelizer. This system ran error-free for over 12 hours with and without a low-noise amplifier. To our knowledge, this is the first time an X-band SATCOM receiver has been operated without analog amplification and down-conversion in a military application.**

***Index Terms*— Satellite communication, Digital radio, Sigma-delta modulation, Cryogenic electronics.**

I. INTRODUCTION

MYRIAD radio frequency (RF) applications, for both the commercial and the military markets, would benefit from the flexibility enabled by digital distribution and processing [1]. A simultaneous offering of linear data converters and high-speed digital logic makes superconductor electronics a candidate for such applications. Mixed signal rapid single flux quantum (RSFQ) integrated circuits with niobium (Nb) Josephson junctions (JJs), featuring direct digitization and digital processing of RF signals, are particularly attractive for building a variety of communication, signals intelligence (SIGINT), and electronic warfare (EW) receivers [2].

Founded upon the concept of direct digitization at RF, the digital-RF multi-band, multi-channel receiver architecture (Fig. 1) encompasses a plurality of radio frequency functions. These include strategic and tactical communications through diverse modalities (line-of-sight, over-the-horizon, via satellite, etc.), as well as signals intelligence (SIGINT), electronic warfare (EW), and surveillance radar.

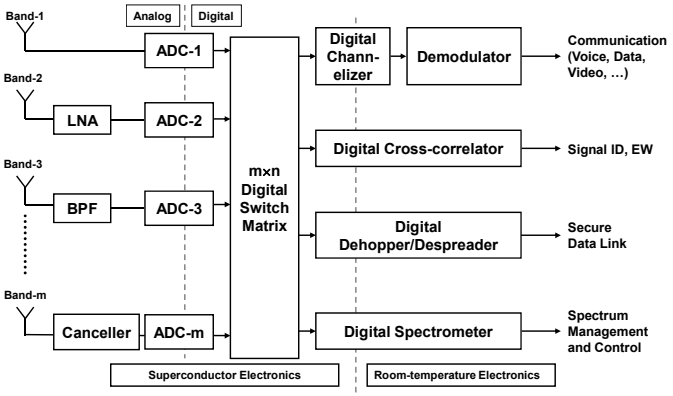

Fig. 1. Generalized block diagram depicting the digital-RF receiver concept, which uniquely incorporates RF distribution. The analog RF inputs are directly digitized with a set of analog-to-digital converters (ADCs), paving the way for the remaining receiver functions to be performed entirely in the digital domain.

A unique feature of the digital-RF receiver architecture is the incorporation of the RF distribution function [3]. The digital switch matrix provides programmable connectivity between a band-specific component chain and one or more digital processing chains. These digital processing units are band-independent and programmable. The simplest example is a channelized receiver function which involves digital down conversion and filtering to extract a narrow sub-band from one of the wider digitized bands [4]. Such channelized receivers have been built and demonstrated for various bands, such as the HF-VHF (2-175 MHz) bands, X-band (7.25-7.75 GHz) and Ka/EHF-band (20.2-21.2 GHz), all featuring direct digitization at RF. A slightly more complex version, specifically for the Link 16 waveform, also performs dehopping with a two-step channelization process.

Superconductor electronics require special system infrastructure, including cryogenic cooling. Therefore, it is advantageous to follow a modular design strategy where the same infrastructure can support a variety of superconductor integrated circuits (ICs). The availability of cooling in a system opens up another dimension in system design. Our hybrid temperature heterogeneous technology (HTHT) system integration approach uses different components, such as superconductor, semiconductor and optoelectronic, at different temperatures supported by a common cryogenic subsystem.

Manuscript received 3 August 2010. This work was supported in part by the Office of Naval Research.

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II. Digital-RF System with Superconductor Electronics

Superconductor ICs operate at a very low temperature (around 4 K), require a set of independent adjustable current sources to bias different circuit blocks for optimum performance, and generate low-power digital outputs that must be substantially amplified before interfacing to standard room-temperature electronics. Moreover, these chips only operate in a low magnetic flux environment. Therefore, any digital system with superconductor ICs has special requirements.

First, a closed-cycle refrigerator (CCR) or cryocooler must be provided to cool the chips. So far, in all the digital-RF system prototypes, we have used a commercial two-stage Gifford-McMahon (G-M) cryocooler, manufactured by Sumitomo Heavy Industries Ltd., with an integrated He damper to quell the temperature oscillations resulting from periodic compression and expansion of He gas at ~1Hz [6]. Second, a computer-controlled multi-channel current source is required to provide bias currents to the chips. Third, dc-coupled broadband amplifiers are necessary to interface with room-temperature electronics, typically a commercial FPGA. In our digital-RF system prototypes, they are assembled as a circuit board supporting a set of amplifier modules. Magnetic shielding is necessary and at least two nested shields have been used in all prototypes. In addition to these basic requirements, there are several other cryopackaging considerations, such as the design of dc bias leads and transmission lines for high-frequency analog and digital input-output signals.

A. Modularity in Digital-RF Systems

A digital-RF system can be divided into an HTHT signal subsystem and a power and control subsystem. The signal subsystem comprises different signal processing modules operating at different temperatures interconnected with specialized input/output (I/O) technology. For simplicity, Fig. 2 shows only three temperatures: ambient (typically, 300 K), low (nominally, 4 K for Nb ICs), and intermediate (typically, 40-80 K). In general, there could be several isothermal modules, each comprising different components, which would be attached to the cryocooler subsystem with thermal links and actively temperature controlled. In addition to superconductor ICs, the low-temperature module might include semiconductor amplifiers for low-noise analog inputs [8] and digital outputs [9]. Since the heat lift at 4 K comes at a heavy premium, the benefits of placing any active electronics at low temperature must be carefully evaluated against the power consumption budget. High-temperature superconductor (HTS) analog filters, and semiconductor low-noise amplifiers (LNAs) are examples of intermediate temperature components. HTS leads and optical fibers are examples of specialized I/O technologies bridging two temperature stages.

Superconductor digital ICs are fast but limited in complexity. Even with optimistic projections for complex digital ICs, enabled by fabrication technology advances, many of the digital signal processing tasks will remain beyond the realm of superconductivity in the foreseeable future.

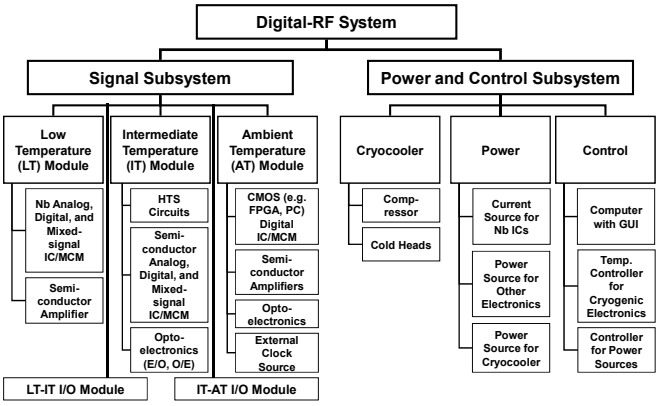


Fig. 2. Digital-RF system comprises a signal subsystem and a power subsystem, which consists of a set of modules.

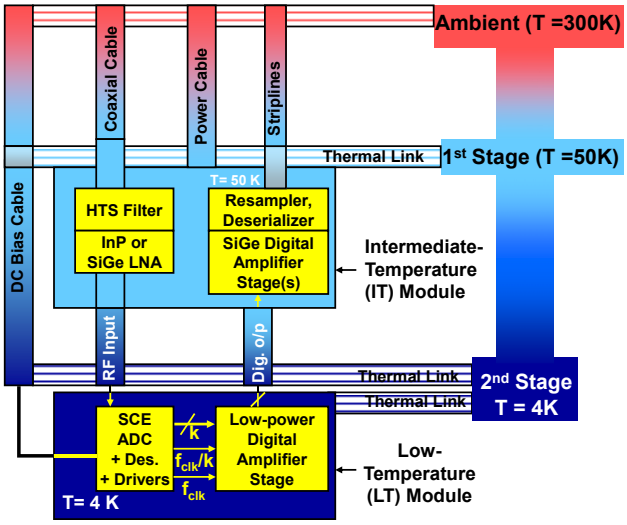


Fig. 3. Hybrid temperature heterogeneous technology (HTHT) system integration.

The HTHT paradigm naturally augments the superconductor electronics capabilities with slower and much more complex CMOS processors at ambient temperature. An example of this is the polyphase Sliding Goertzel infinite impulse response (IIR) digital filters for Link-16 demodulation [7]. It is also conceivable that additional digital processing could be performed at the intermediate stage taking advantage of faster logic families (e.g. SiGe CML) at cryogenic temperatures. Fig. 3 shows an example of an HTHT receiver system with low- and intermediate-temperature modules at 4 and 50 K respectively. This HTHT modular system design concept can be extended to other digital systems, such as a network switch or a high-performance computer, as well as for those with even lower (in the mK range) temperature devices, such as cryogenic energy and particle detectors, and qubits.

The modular design extends to the elements of the power and control subsystem. For example, a different cryocooler may be used in these systems so long as the heat lift capacities are adequate to support the signal subsystem.

III. Modular System Design

In system design, there is an inevitable trade-off between customization and standardization. All aspects of superconductor ICs and their cryopackaging are evolving.

Therefore, early adoption of strict standards can throttle innovation and increase system cost. Full customization for a single chip and a single application is against our multi-function, multi-band digital-RF receiver development philosophy. Instead, our approach has been to build a modular system that can be reconfigured and expanded in response to future needs. The system prototypes built and delivered to date have been relatively simple: a single chip low-temperature (4 K) module, ambient temperature digital interface module and FPGA boards, and occasionally, intermediate temperature HTS filters.

A. Chip Module

Currently, optimization of the dc power and input-output (I/O) leads, which dominate the heat load, and therefore, the power consumption of a cryocooled system, is a fertile area of research. Therefore, we have allowed for customization within each of the different classes of leads used for dc biases, analog signal and clock inputs, high-speed digital outputs, and low-speed digital monitors (used during system set-up and troubleshooting). The mapping between the standardized chip pads and the different I/O leads is performed by a distributor printed circuit board (PCB), which is designed for each class of chips. Thus, a chip module comprises the chip, its customized distributor PCB and a set of impedance matched low-loss transmission lines between them.

The 5 mm × 5 mm and 10 mm × 10 mm chips have 40 or 80 signal pads around their perimeters respectively with another the ring of ground pads inside. The chip sits in a nest and makes pressure contact through a set of pads to another PCB, which has striplines connecting each chip pad to a Cu coaxial cable. The distributor PCB connects the coaxial cables to the appropriate connectors for the aforementioned classes of I/O leads. Reminiscent of the liquid He immersion probe, this design was chosen to adopt the dual mu-metal shields that have been successfully used for over a decade. The chip module is supported by a metallic plate, matching the shape of the distributor PCB. This plate provides thermal connectivity to the cryocooler. The chip module is ideally isothermal, and therefore, the transmission lines are all designed for lowest loss. The module is equipped with a heater and a thermometer for temperature control.

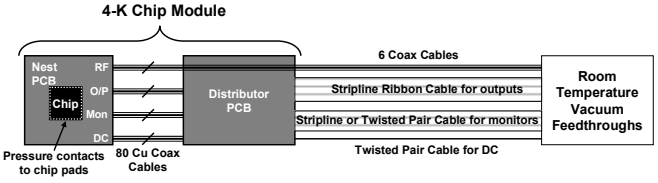
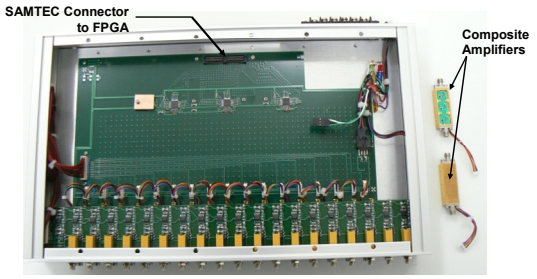


Fig. 4. Electrical connection to the chip. All cables between 4 and 300 K are thermalized at the intermediate temperature stage (not shown for simplicity).

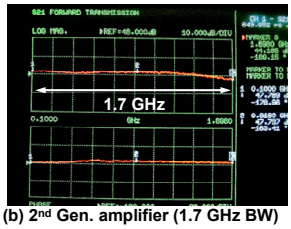
There are several advantages of this modular design. First, a user can conveniently substitute one chip module with another by detaching and attaching a few connectors; no handling of the chip itself is necessary. Second, the chip designer is not constrained to a fixed chip size (cost) and pad assignment. For example, a chip containing a single ADC and a 1:16 deserializer neither requires the area nor the pad count of a chip with two decimation filters (e.g. the X-band ADR)[10]. Even when the chip complexities are comparable, the additional flexibility afforded by the distributor PCB facilitates the superconductor IC layout. Finally, multiple such chip modules may be attached to a single cryocooler. Although only single chip modules are described here, the design concept extends to multi-chip modules (MCMs). In fact, the current design will accommodate an MCM with a 10-mm × 10-mm carrier, such as a multi-band ADC with two 2.5-mm × 2.5-mm front-ends flipped on a carrier [12].

B. Digital Data Interface Modules

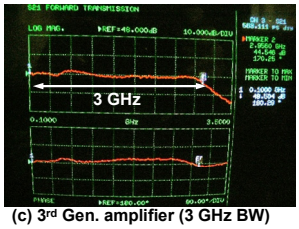
Interface amplifiers are essential for transferring outputs from a superconductor chip to room-temperature electronics. In all systems to date, the digital data link starts with SQUID-stacks on the superconductor chips [4],[5]. These mV-level dc-coupled outputs are amplified with a bank of amplifiers and drivers for standard digital logic. These composite amplifiers have two 3-stage sections—a low-frequency section with Si and a high-frequency section with SiGe bipolar transistors—to provide a flat gain profile of 48 dB over a bandwidth. The initial design, used in the second generation ADR systems, had a bandwidth of 1.7 GHz; these amplifiers were used for data rates up to 1 Gbps. By adding an inductive component to the feedback path, the bandwidth was extended to nearly 3 GHz in the next generation. With these amplifiers, the data link was extended to 2 Gbps (for an ADC with 32 GHz clock and 1:16 deserialization ratio). Fig. 5 shows a multi-channel amplifier assembly and the frequency response of a composite amplifier measured using a vector network analyzer.



(a) Interface amplifier assembly



(b) 2nd Gen. amplifier (1.7 GHz BW)



(c) 3rd Gen. amplifier (3 GHz BW)

Fig. 5. (a) Multi-channel interface amplifier assembly is shown along with individual amplifiers with and without cover. The S21 measurements of (b) second and (c) third generation amplifiers are shown.

Without error-correction coding, the input data rates to FPGA chips (e.g. Xilinx Virtex-4 and Virtex-5 families) are limited to about 1 Gbps. Post-amplification deserialization with commercial ICs is used to accommodate higher ADC sampling rates without increasing on-chip circuitry. A deserializer circuit board, composed of a clock distribution chip (MC100LVEP210), feeding eight Quad D flip-flops (MC100EP131QFN32), was made to couple to an amplifier bank with 1 clock and 16 data channels. Each of the 16 data bits is applied to a pair of D flip-flops that are triggered on

alternating edges of the clock. With the 3-GHz bandwidth interface amplifiers and the 16:32 deserializer board, an aggregate data transport rate of 32 Gbps (from a single-bit bandpass delta-sigma ADC clocked at 32 GHz) has been demonstrated.

C. I/O leads

DC biasing of superconductor chips using metallic leads contributes the largest fraction of heat load. So far, in both generations dc biasing has been done with ribbons of BeCu twisted pairs. Ideally, the resistance of each lead should be inversely proportional to its bias current to equalize the contributions due to Joule heating and heat conduction, and therefore, minimize its heat load. However, this demands custom wiring and is difficult to achieve. Instead, identical wiring has been used with some optimization done by doubling (or tripling) leads for large biases. As the systems scale to accommodate multiple chips, we envisage the use of high-temperature superconductor leads that have been demonstrated to lower heat load by more than an order of magnitude [5].

D. Transmission lines for digital outputs

Ribbon cables, comprising multiple (10 or 20) striplines, are used to conduct high-speed digital outputs directly from 4-K to room-temperature; no intermediate temperature amplification has been employed in these modular ADR systems. As with the dc cable design, there is a trade-off between heat conduction and attenuation. A 20-line BeCu stripline ribbon cable was chosen for the second generation systems (ADR-003 and ADR-004) described in the next section. To reduce losses even further, the center conductor was made with Cu in the third generation systems; the ground planes remain BeCu to keep heat conductivity low.

IV. Digital-RF System Evolution

We have adopted an iterative, spiral development strategy for these modular digital-RF receiver systems. This was done to balance the need to build deliverable functional prototypes on one hand, and to accommodate technology improvements on the other. In each development cycle, two or more digital-RF receiver systems have been produced with the goal of rectifying the shortcomings of the previous generation and incorporating new technology.

A. First Generation Digital-RF Receiver Systems

In what we now refer to as the first generation, two digital-RF receiver systems were produced. The first system (ADR-001), a complete X-band satellite receiver prototype, was delivered to the Joint SATCOM Engineering Center (JSEC) in Ft. Monmouth, NJ and demonstrated direct digitization, digital down conversion and filtering of X-band (7.25-7.75 GHz) signals from XTAR, DSCS and the newly launched WGS, while it was still visible from the U.S. east coast. The receiver was successfully integrated with a digital I&Q MODEM from L-3 communications, demonstrating demodulation of a MIL-STD-188-165A uncoded BPSK-modulated waveform at 1.544 Mbps. A nearly identical second system (ADR-002) was delivered to the Air Force Research Laboratory. It hosted a low-pass digital channelizing receiver chip, clocked at 24.32 GHz, targeting SIGINT functions for bands in the lower RF range. Most of the cryopackage on these first generation systems was custom-made, but the modular design philosophy had been introduced in the form of a chip module. This allowed us to perform a modular upgrade subsequently, replacing the 10-GHz chip made with the 1 kA/cm^2 HYPRES IC fabrication process with a 30-GHz chip made with the 4.5 kA/cm^2 process.

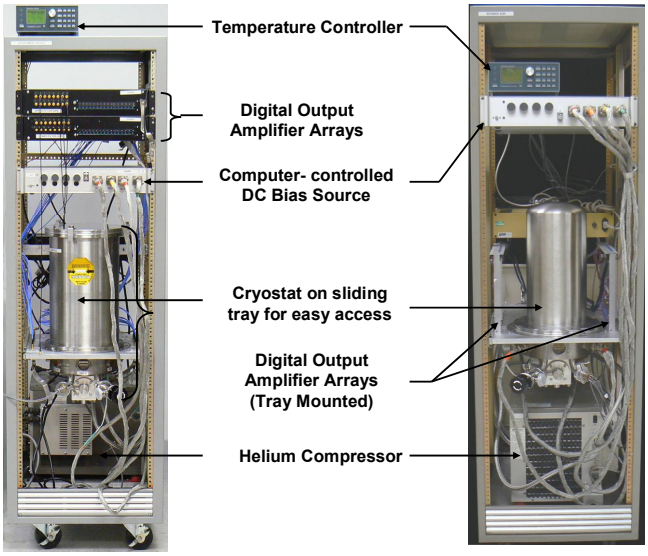


Fig. 6. First (left) and Second (right) Generation Digital-RF Receiver Systems.

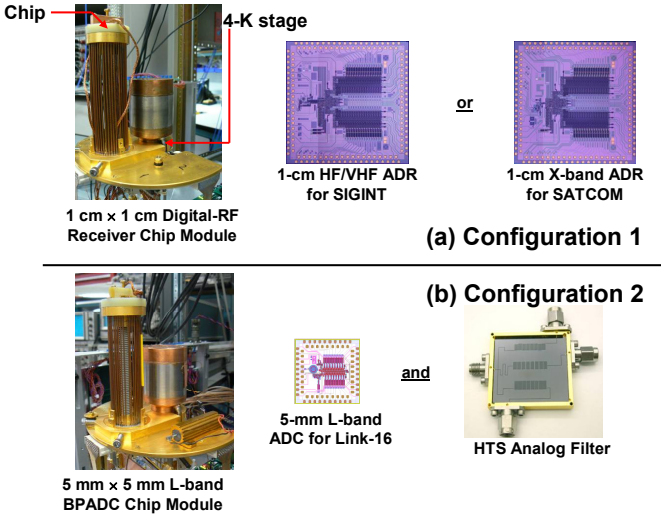


Fig. 7. Two different chip modules were attached to ADR-004 for different applications: (a) a module for 1-cm ADR chips comprising an ADC front-end and a digital channelizer, (b) a module for a 5-mm ADC chip. This second generation system was also equipped with an additional temperature controlled stage for mounting an HTS analog filter.

B. Second Generation Digital-RF Receiver Systems

Although the second generation systems (ADR-003 and ADR-004) have similar appearance to the first (Fig. 6), there are significant differences. First, the digital output data link was vastly improved permitting much higher data rate per line. This was critical for the modular reconfiguration (Fig. 7) of one of the systems (ADR-004) from a channelizing receiver chip with relatively low-speed digital outputs ($f_{clk}/256$ = 100-120 Mbps, where f_{clk} is the clock frequency and the

decimation ratio is 256) to an ADC with deserializer with much higher speed outputs ($f_{clk}/16$ = 600 Mbps for 9.6 GHz clock frequency and the deserialization ratio is 16). This was accomplished by improving the transmission lines inside the cryostat and improving the bandwidth of the interface amplifiers. The output amplifiers were also mounted on the tray, in close proximity to vacuum feedthroughs, eliminating long routing of external cables which are susceptible to electromagnetic interference.

Second, the 40-K radiation shield was completely redesigned to have higher emissivity and heat conductance and lower surface area and volume. Together these improvements substantially lowered the 4-K heat load and reduced outgassing. The need for frequent (weekly) pumping due to outgassing had been identified as a major operational inconvenience for the first generation systems. ADR-003 has been run for over three months with no change in cold stage temperature.

C. *Third Generation Digital-RF Receiver Systems*

The goal of the third generation systems was to double the capacity and reduce the temperature difference between the cryocooler and the superconductor chip. These systems can accommodate two chip modules, have 80 high-speed digital I/Os, and can be equipped with up to four 17-channel interface amplifier assemblies and two current sources. They also include a vacuum pump for user convenience. Fig. 8 shows the major parts of the system.

There are some significant differences from the previous generations. First, all the electrical vacuum feedthroughs are through the "top plate" of the cryostat providing convenient access (Fig. 9). Second, the chip module is flipped vertically and no longer protrudes beyond the cryocooler allowing compaction of the cryostat. The cryostat itself is inverted relative to the orientations of earlier generations.

Cross-talk in the vacuum feedthrough connector for digital data output was proven to be the bottleneck limiting clock frequency in the second generation systems. A multi-coax vacuum feedthrough using Corning Gibert G3PO connectors (each rated at 60 GHz) was designed to remove this problem. The top plate accommodates four such 20-line high-bandwidth coax (G3PO) feedthroughs; only one is used in the current ADR-005 configuration with a 5×5 mm^2 X-band ADC chip mounted.

The third-generation chip module includes a specially machined piece (shaped like a cross on top of the pressure block) acting as a high-conductance thermal link between the chip and the cylindrical Cu block through which all input/output coaxial lines are fed. This design follows the same principles used in construction of the dual-mode cryo-probe [6] and achieves substantial reduction in the temperature difference between the cryocooler and the superconductor chip to about 50 mK. An exploded view of the top section of the superconductor chip module is shown in Fig. 10. The chip sits on a printed circuit board with contact finger (neither is shown for clarity). Contacts are made by applying pressure on the back of the chip.

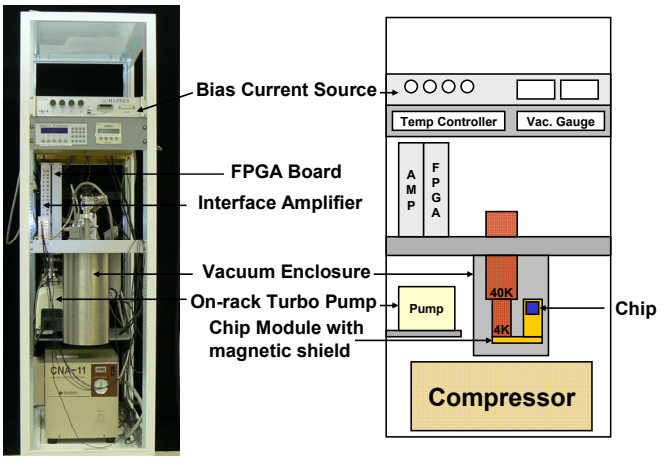


Fig. 8. The first of three third-generation systems (ADR-005).

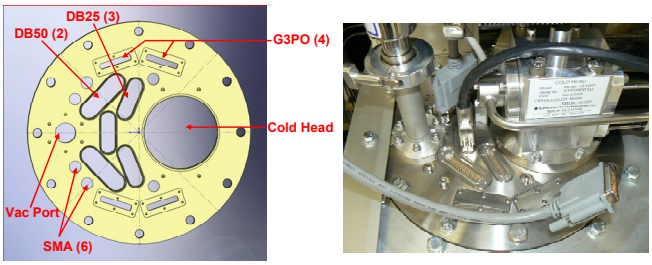


Fig. 9. Vacuum feedthroughs on the cryostat top plate in 3rd generation ADR systems.

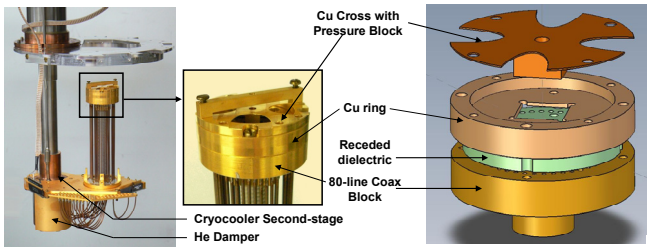


Fig. 10. The 3rd generation chip module is shown attached to the 4-K stage of the cryocooler; two such modules may be attached. The chip nest components are shown on the right.

Modularity is extended to the design of interconnects between the low and the intermediate temperature stages. Once the reliability of low resistance connectors to the HTS ribbon cables are established, they would replace the metallic ribbons. The striplines have been improved as well. In the current design, two 10-stripline ribbon cables are connected to matching 20-G3PO connectors on either end of the 4K-300K digital link.

V. Digital-RF Receiver Applications

A. *Data Links*

One of the promising application areas for digital-RF receivers is in the area of tactical data links employing fast frequency hopping, such as Link-16. Digitization of the entire band of interest (960-1215 GHz) helps expansion to multiple concurrent Link-16 nets in a single radio. First, once in the digital domain multiple copies of the RF signal can be produced without loss of power and fidelity. Second, the expensive analog synthesizers that produce the frequency hopping local oscillator signals are eliminated.

ADR-004 was reconfigured with a bandpass delta-sigma ADC chip (Fig. 12(a)) to demonstrate multi-net Link-16 reception. Digitized RF data were deserialized by a factor of 16 on the superconductor chip and by another factor of 4 on the FPGA before performing two-step channelization. The first step of channelization divided the band of interest into four 75 MHz wide sub-bands (SB-1 to SB-4), each represented as 16-bit complex (I and Q) words at 150 MHz. For two-net reception, two copies of these coarse channelized data are produced for further processing through two independent, identical paths, comprising a switch and a fine channelizer (Fig. 11). The switch, upon receiving the hop sequence, selects one of the four sub-bands containing the current hopped carrier frequency for its output. Next, the fine channelizer translates the carrier to baseband by performing complex multiplication between the I and Q words and the corresponding frequency offset data that is generated and stored for all the carrier frequencies. An analog HTS filter was added on the first (40 K) stage to reject unwanted parts of the spectrum.

Although these chips work at a clock frequency of at least 25.6 GHz, in ADR-004 the clock frequency was limited to about 10 GHz due to the cross-talk between the data outputs at the vacuum feedthrough. Starting with the specified baseband clock rate of 5 MHz, the ADC sampling clock frequency of 9.6 GHz was chosen to obtain an integer decimation ratio (30) together with a power-of-two deserialization ratio (64).

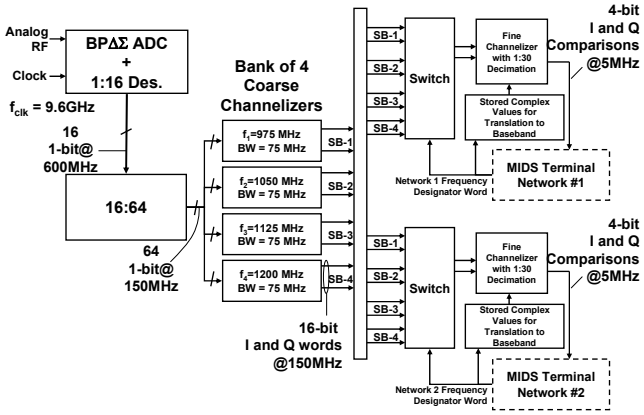


Fig. 11. Link 16 signal processing consists of a coarse and a fine channelization steps along with a switch.

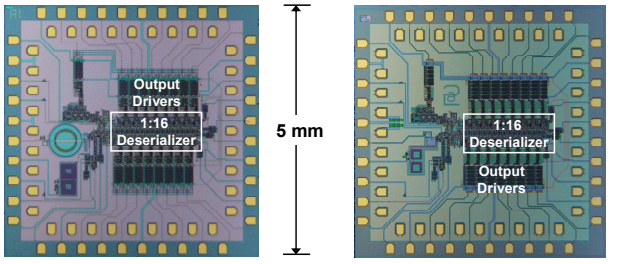


Fig. 12. Bandpass Delta-sigma ADCs integrated with 1:16 deserializer and output drivers with (a) 1.1 GHz and (b) 7.5 GHz loop filter center frequencies.

Two independent frequency-hopping modulated and encrypted Link 16 analog waveforms for two MIDS (Multifunctional Information Distribution System) terminals were power-combined into a single RF input to the ADR-004 system. Two modified MIDS terminals, each sending its hop-net sequence to the ADR-004 and receiving the digitally dehopped data, were used for the demonstration. Each receive terminal could be programmed to receive either of the two transmitted Link 16 networks.

B. Satellite Communications

Another application of digital-RF receivers is in the area of satellite communications (SATCOM). Direct digitization of the entire band (e.g. 7.25-7.75 GHz for X-band ground stations) permits satellite spectrum monitoring and control, as well as channelized communication. Bandpass delta-sigma ADCs have been designed for SATCOM C, X, Ku and Ka bands [11],[12].

Upon completion in 2009, the ADR-005 system was initially configured for X-band SATCOM application with an objective to repeat the 2007 demonstration on ADR-001. The satellite signal frequency (f_{RF} = 7.676 GHz), waveform (uncoded BPSK-modulated data at 1.544 Mbps), ADC sampling frequency ($f_{clk} = 4f_{RF}/3$ = 10.234667 GHz), and decimation ratio (256) were chosen to be identical. In contrast to the 1 cm^2 X-band channelizing receiver chip demonstrated on ADR-001 system, a 5×5 mm^2 X-band ADC chip (Fig. 12(b)) was used in conjunction with a polyphase channelizer implemented on a commercial Xilinx Virtex-4 FPGA; the interface to the L-3 communications digital I&Q MODEM with 16-bit I&Q words at $f_d = f_{clk}/256$ = 40 Mbps was unchanged.

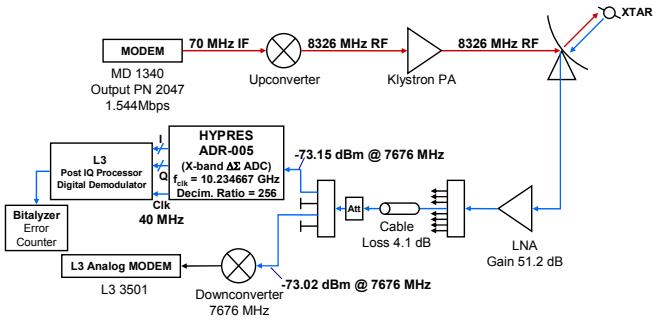


Fig. 13. Comparative measurement of digital-RF receiver with conventional analog-RF receiver.

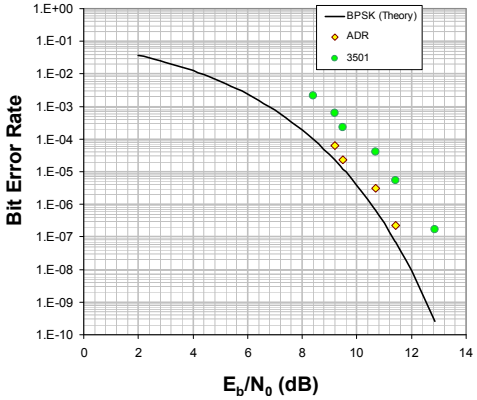


Fig. 14. Measured bit error rate with digital-RF receiver corresponds well to the theory.

First, the ADR-005 system was operated continuously for 12 hours to test its stability. It demonstrated error-free operation. Next, an experiment was set-up to compare the digital-RF receiver performance to a standard SATCOM

receiver with an analog downconverter (Fig. 13). ADR-005 performed favourably showing good agreement of the bit-error rate as a function of energy signal-to-noise ratio (E_b/N_0) with theory (Fig. 14).

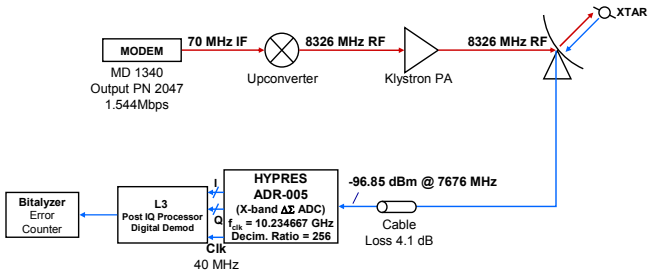


Fig. 15. Comparative measurement of digital-RF receiver with conventional analog-RF receiver.

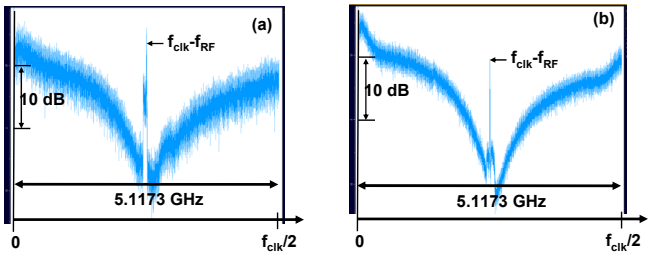


Fig. 16. Digitized power spectra for the experimental configuration shown in (a) Fig. 11, and (b) Fig. 13, with and without LNA, respectively. The sampled replica of the signal-of-interest appears at f_{clk}-f_{RF} = 2.559 GHz.

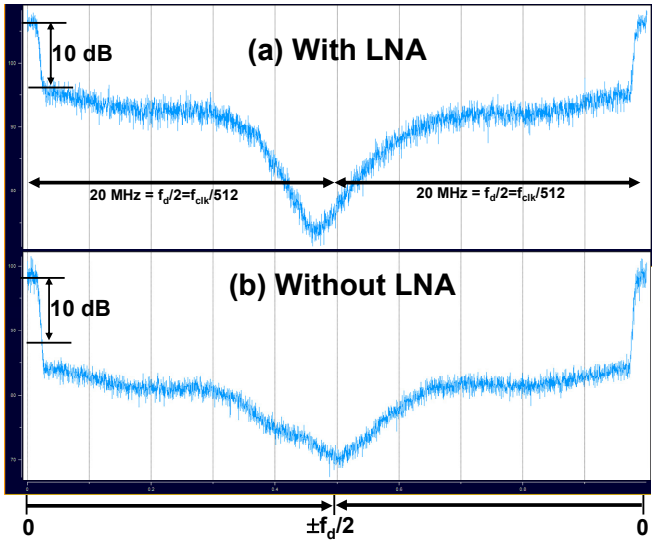


Fig. 17. Down-converted and filtered baseband power spectra for the experimental configuration shown in (a) Fig. 11, and (b) Fig. 13, with and without LNA, respectively.

Next, the ADR-005 was connected directly to the antenna, bypassing the LNA (Fig. 15). Once again, its stability was verified by continuous error-free operation for 12 hours. The digitized spectra in the two configurations, with and without LNA, are shown in Fig. 16. Even without the LNA, no significant performance degradation was observed since the noise pedestal from the satellite's power amplifier was still above the quantization noise floor of the ADC. In fact, the signal-to-noise ratio without the additive noise contribution from the ambient temperature LNA is slightly better. Fig. 17 shows the baseband spectra in the two experimental configurations. In this experiment, the unavoidable cable loss, necessary to cover the distance between the antenna and the ADR-005 system, was substantial.

The same chip (Fig. 12(b)) was subsequently tested in the ADR-005 system at substantially higher (24-32 GHz) clock frequency with a variety of phase and amplitude modulated waveforms at 30 Msymbol/s (Fig. 18). The total deserialization factor was 32, including a factor of 2 in the room-temperature data interface module. Fig. 19 shows the digitized power spectrum with 32 GHz clock frequency.

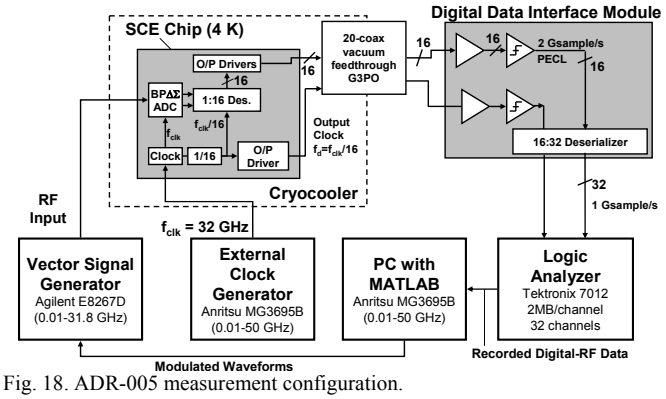


Fig. 18. ADR-005 measurement configuration.

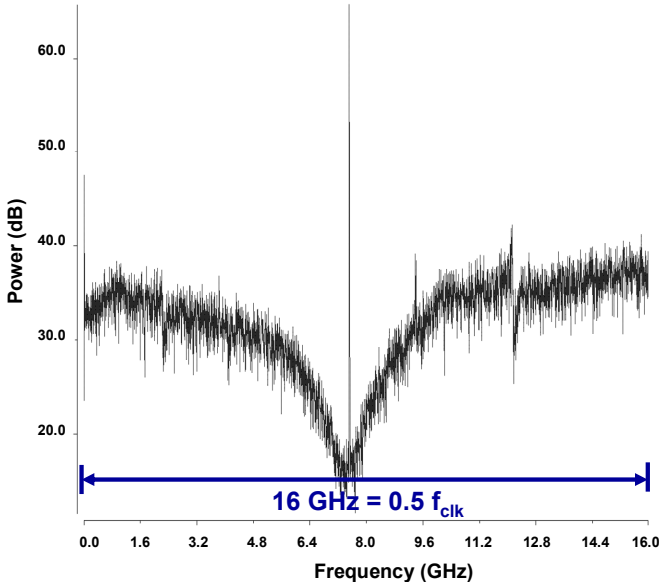


Fig. 19. Digitized spectrum of the X-band ADC output. The ADC is clocked at 32 GHz with a 7.53 GHz sinusoidal input. The signal-to-noise ratio in the 7.25-7.75 GHz band is 28.8 dB corresponding to 4.5 effective number of bits in 500 MHz instantaneous bandwidth.

ACKNOWLEDGMENT

We thank Dr. Deborah Van Vechten of the Office of Naval Research for sustained encouragement, guidance, and critical evaluation throughout the development of these digital-RF receiver systems. We thank Nenad Djapic, Ripal Shah, Patrick Crescini, Michael Spencer of SPAWAR Systems Center, Pacific, Prof. Raafat Mansour of University of Waterloo, and Dr. Peter Camana, Dick Rodems, Mike Aird, and Pablo Solis of ViaSat for collaborative work culminating in the first concurrent multi-net Link-16 demonstration, and Rick Dunnegan of U.S. Army CERDEC for his invaluable help and guidance during the satellite communication demonstration at Aberdeen Proving Grounds, MD.

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