A Comparison of Two Types of Single Flux Quantum Comparators for a Flash ADC with 10 GHz Input Bandwidth

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Abstract - We compare the SQUID wheel/Quantum Flux Parametron (QFP) comparator to a new Rapid Single Flux Quantum (RSFQ) compatible design. Both have been simulated to demonstrate ~0.5 ps threshold accuracy which would permit the construction of a flash analog-to-digital converter with six effective bits of resolution at 10 GHz input bandwidth, over three times better than the best performance demonstrated with any technology. At lower input frequencies, both designs have demonstrated that a 10-bit flash ADC is possible. Although simulations of the QFP-based design are more accurate at high signal slew rates due to its symmetry, the RSFQ-based design has a better signal-to-noise ratio and a faster and more flexible clocking scheme which ultimately prove to be more important.

I. INTRODUCTION

Superconductors exhibit a unique combination of properties that permits the construction of extremely high performance analog-to-digital converters (ADCs). Magnetic fluxoid quantization provides a natural ruler which may be used to produce a large number of quantum mechanically accurate thresholds for the ADC. This interference of phase coherent electrons produces an effect similar to the interference fringes seen when a laser beam is split and recombined. In a Superconducting QUantum Interference Device (SQUID), we control the phase of the interfering electrons by applying magnetic flux to a loop which is exactly proportional to the signal current in a nearby inductor. For high resolution ADCs this provides much better accuracy than any semiconductor ADC which relies on component matching for precision (i.e., all but sigma-delta converters which have low input bandwidth). For lower resolution converters (10-bits and less) this quantization may be exploited to produce periodic threshold comparators reducing the number of comparators and therefore the signal power required to achieve a high signal-to-noise ratio. It also greatly reduces the matching requirements due to the smaller number of resistors and comparators required. We require both accuracy *and* high speed for high performance ADCs. The speed of single flux quantum circuits is set by time constants which are typically ~3 ps in our 2 micron process and decrease linearly with minimum linewidth. This permits rapid readout of the precise thresholds generated by flux quantizers. It is also possible to perform real-time digital error correction or signal averaging to enhance accuracy.

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The fast, accurate thresholds must not be degraded by noise or on-chip interference. The thermal noise energy at 4.2 K is 75 times below the best noise level at room temperature. This permits high dynamic range and sub-picosecond time resolution. The time resolution or contribution to jitter of a gate is roughly the signal risetime divided by its signal-to-noise ratio and is usually less than 0.1 ps. The fast risetimes and low noise are preserved by ideal superconducting transmission lines and, unlike in semiconductor circuits, a very close groundplane to obtain low impedance almost eliminates crosstalk from other lines. One further advantage of superconducting circuits using single flux quantum logic is that the power dissipation in a Josephson junction is negligible so that its temperature and critical current do not depend on the history of the data pattern seen by the junction. This problem was significant in earlier ADCs based on voltage latching circuits.

II. BACKGROUND

Our approach is based on the fact that the circulating current in a superconducting loop broken by Josephson junctions (a SQUID) is a periodic function of the applied magnetic flux. The application of this effect to ADCs is not new [1-5], but HYPRES has used lower inductance SQUIDs to reduce the threshold hysteresis at high signal speeds in combination with multi-turn, wide-band dc transformers to restore input current sensitivity. A circulating current arises spontaneously in the SQUID which cancels some of the applied flux to bring the loop flux closer to the nearest integer multiple of the flux quantum (Φ_o = h/2e ~ 2.07 mA-pH). This current is then sampled to determine its direction. One way is arbitrarily assigned the value of "0" and the other a "1".

The performance of earlier designs is limited by shifts in certain comparator thresholds at high input signal slew rates. This is most apparent as a signal slew rate dependent duty-cycle in the output of the least significant bit (LSB) comparator. During the rising edge of an input signal the LSB produces less than 50% ones, but during the falling edge it produces more than 50% ones. Ideally, the ratio should be 50/50 during both the rising and falling edges. Using a symmetrized circuit design analogous to a fully differential approach in transistor circuit design, it is possible to cancel these undesirable distortions while retaining the periodic behavior.

III. THE SQUID WHEEL/QFP COMPARATOR

The circuit for the Quantum Flux Parametron (QFP)-based comparator is composed of three parts (see Fig. 1). The periodic quantizer circuit continuously "measures" the input signal modulo one flux quantum (Φ_0 = h/2e, where h is Planck's constant and e is the electron charge). This circuit is sometimes called a 2-spoke SQUID wheel [6,7] and sometimes a 2-leaf phase tree [8] and it produces an output which is a smooth, approximately sinusoidal function of the input. This is followed by the QFP (operation is described by Ref. [9]) decision-making circuit which digitally samples the output current of the quantizer with high sensitivity and time resolution. The QFP decides whether the output current of the quantizer is positive or negative ("0" or "1") when a large current step from the clock C1 is applied. Since its output is current in an inductor rather than voltage, it requires a voltage generating read-out gate.

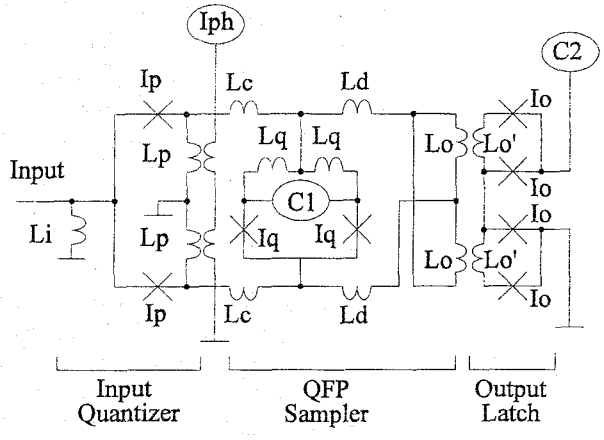


Fig. 1 The balanced comparator circuit schematic includes three distinguishable subcircuits. The dc current source Iph provides current to produce a phase drop of π across the inductors Lp. This circuit provides a current to the QFP sampler which is a sinuoidal function of the input current. C1 clocks the sampler circuit and produces either a positive or negative current which is then sensed by the SQUIDs in a readout latch (clocked later by C2) to produce a millivolt level output. The nominal values for the components are: Li=0.5, Ip=0.1, Lp=1.2, Lp'=3.6, Lc=0.5, Ld=1.0, Lq=0.5, Iq=0.4, Lo=4, Lo'=3, Io=0.25 (in mA and pH).

A series pair of SQUIDs called a CLAM (Current Latching Analog Microcomparator) [1] was chosen for the read-out function although this is not critical to performance. Both the QFP and CLAM are edge-triggered, high-margin circuits and their input thresholds are set at zero by symmetry. The outputs of the quantizer and QFP are also centered around zero by symmetry. This allows us to avoid bias adjustments to set dc threshold levels in the ADC.

In noiseless simulations of the SQUID wheel/QFP, we saw no errors at all because of the perfect symmetry of the circuit. Since performance was expected to be limited by component accuracy, an order of magnitude improvement was anticipated over our best high speed results. This means three more bits of resolution are achievable with the same fabrication process by interleaving eight LSB comparators.

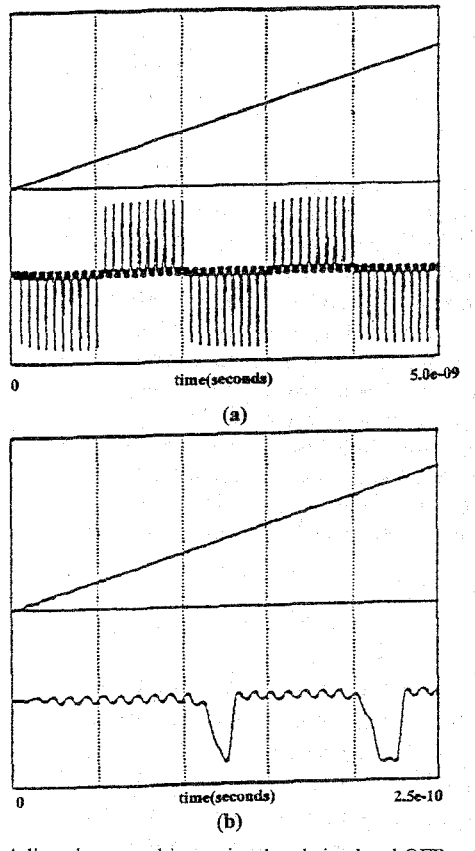


Fig. 2 (a) A linearly ramped input signal and simulated QFP output current is shown for a 10 GHz clock rate and signal slew rate of about one flux quantum/10 ps. The 1's and 0's are positive and negative peaks. The clock and fluxon periodicity beat with 20 clock cycle period indicating 0.5 ps accuracy. (b) an expanded view near zero

The comparator design has the desirable property that the ratio of 1's to 0's does not systematically shift away from 50/50 at high signal slew rates because the two states of the comparator (excepting the readout) are mirror images and symmetry prevents one being favored over the other. High speed simulations of the comparator are shown in Fig. 2. The input is a linear ramp to make the results easy to interpret. The slew rate is chosen so that the SQUID wheel displays periodicity very close to 10 times the 10 GHz clock frequency. This produces a "beat-frequency" which allows us to determine the placement of the comparator thresholds with a precision better than a picosecond. In our case, the periodic behavior of the comparator is repeated about every 10 picoseconds and we see an output pattern repeat time of 20 clock cycles without any errors (10 1's followed by 10 0's, repeating) so the thresholds are accurately defined to better than 1/20th of the periodicity or 0.5 ps. This level of performance would permit 6 effective bits of resolution at 10 GHz, 8 bits at 2.5 GHz, or 10 bits at 625 MHz input bandwidth.

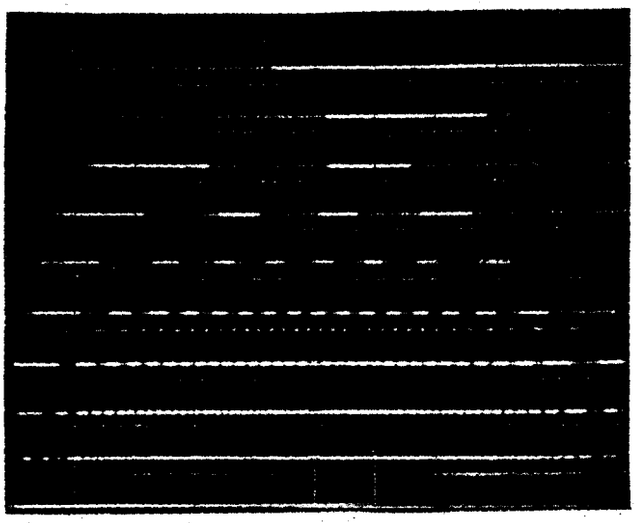


Fig. 3 The raw outputs of a Gray-coded 10-bit QFP-based ADC. This demonstrates between 9 and 10 bits of dynamic range in Gray code, but interleaving 4 of these comparators would permit a 10-bit ADC.

The circuit was laid out, fabricated and successfully tested to show correct operation at low clock and signal speeds. Fig. 3 shows the results from a 10-bit Gray-coded flash ADC. We see that the LSB comparator exhibits between 256 and 512 thresholds of dynamic range. Interleaving 4 LSB comparators would yield a 10 bit ADC. When the circuit was tested at GHz clock rates, we found the thresholds became blurry. An explanation for this may be seen in the noise analysis by Ko and Lee [8]. Their QFP sensitivity improved by a factor of 10 when low speed clocking was used. In our case, layout parasitics and the large QFP inductance relative to the SQUID wheel inductance mean that only a small fraction of the SQUID wheel current couples to the QFP. Fig. 4 shows the digital outputs of six bits of an eight bit ADC during a beat frequency test at 843 MHz. At frequencies above this, fewer transitions were available or they were indistinct permitting a 5 ps aperture time ADC at best. This limitation is the principal reason we have begun to investigate a Rapid Single Flux Quantum (RSFQ)-based comparator design.

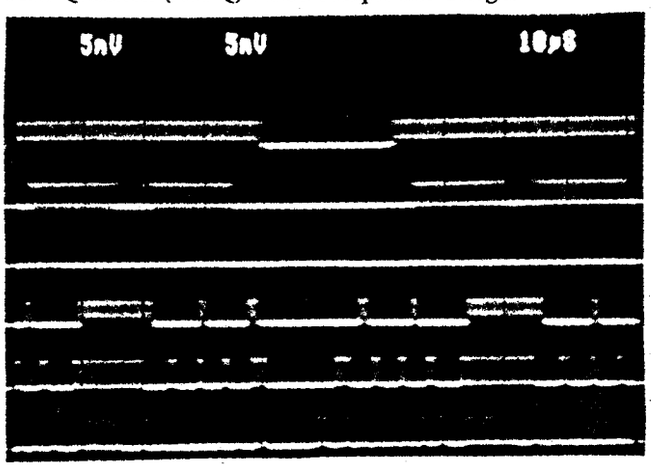
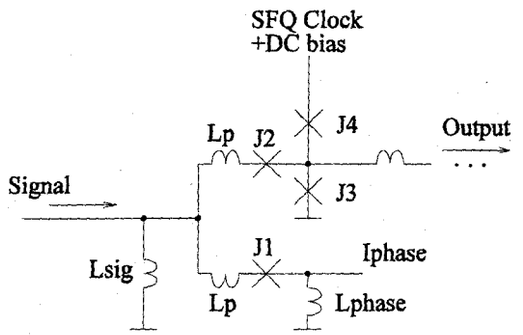


Fig. 4 Beat frequency test results at 843 MHz of QFP comparators. At higher frequencies or resolutions the thresholds became indistinct indicating a low signal-to-noise ratio.

IV. The SQUID Wheel/Decision-Making Pair Comparator

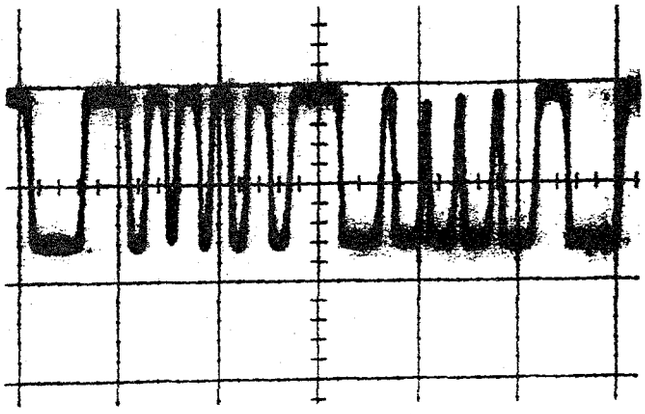
It is possible to make a comparator from a series pair of Josephson junctions (J3, J4 in Fig. 5) as an RSFQ decision-making pair to digitally sample the analog current injected between them. When an SFQ clock pulse is applied (phase increment of 2π), one junction or the other will increment in phase by 2π depending on the value of the current injected between them (through J2). This sampled current would be supplied by the SQUID wheel (J1, J2, Lp, Lphase, and Lsig) for the same reasons it was chosen for the QFP comparator. The SQUID wheel generates a circulating current that is a roughly sinusoidal function of the input signal and it is all coupled to the decision-making pair through J3 to ground. Efficient coupling overcomes the signal-to-noise problem seen in the QFP-based comparator, but this SQUID wheel has higher inductance and should be a little slower than in the QFP design. This circuit has the advantage that both clock and output are in the form of SFQ pulses which may be electrically delayed on chip and easily interfaced with RSFQ digital logic. Therefore, a low power clock from room temperature is sufficient to generate enough flux quanta (fluxons) on chip to clock each comparator. Clock skew between the comparators may be zeroed by adjusting the dc bias of a Josephson Transmission Line (JTL) which is essential for sub-picosecond performance. The SFQ output interfaces directly to the digital error correction logic and interleaving circuitry needed in this architecture. Single comparators have been tested and dynamic range at low speed is adequate to obtain a 10-bit flash ADC, assuming 8 interleaved LSB comparators with 128 thresholds each. This comparator was fully operational up to 30 GHz and has been beat frequency tested at frequencies up



RSFQ Comparator

Fig. 5 The RSFQ-based comparator schematic circuit includes a SQUID wheel (the left side, J1 and J2) and decision-making pair (J3 and J4) to sample it. J1 and J2 are 0.2 mA; J3, and J4 are 0.28 mA, Lsig is 1.0 pH, Lp is 0.25 pH, and Lphase is 0.2 pH.

to 20 GHz (equipment limited), well beyond the 10 GHz input and 20 GSamp/sec clock planned for the ADC. Fig. 6 shows the output of a 10 GHz beat frequency test of a comparator demonstrating 11 digital transitions between the minimum and maximum of the input sinewave (only 8 accurate transitions are needed from each of 8 interleaved comparators to obtain 6 effective bits @ 10 GHz). We first note that the duty cycle of the output is greater than 50% on the rising edge of



(Horizontal scale: 19 ps/div.)

Fig. 6 Beat frequency test of a single RSFQ comparator. Clock and signal are about 10 GHz, but slightly different frequencies. This photo shows slightly more than one beat frequency cycle; its peak is near the center where the comparator output makes no transitions.

the signal and less than this on the falling edge. This is a result of the asymmetry of the circuit, but in principle is a relatively simple problem to correct. A differentiator circuit to inject compensation current into the decision-making node has been designed, simulated, and released for fabrication. We need only approach the ideal compensation current within 20% to reduce the threshold errors in Fig. 6 by a factor of five to less than 0.5 ps and interleaving will permit achieving six effective bits of resolution at 10 GHz input bandwidth. We also note that the full width of these transitions is about 1 ps (horiz, scale is about 20 ps/div), making the RMS threshold jitter about 0.4 ps, adequate to obtain 0.5 ps aperture time in the ADC.

V. Conclusions

The symmetric QFP-based comparator has no need for large numbers of reference currents or compensation of dynamic distortions at high signal slew rates, but it has two practical difficulties: low signal-to-noise ratio due to poor coupling of the SQUID wheel energy to the QFP sampler, and an inconveniently large clock waveform. Both issues appear difficult to improve substantially without sacrificing speed or dynamic range. To obtain the best circuit margins, a trapezoidal clock with large amplitude (>150 mA) would be produced with on-chip regulation of an offset sinewave (clipped by the gap of large Josephson junctions). The power dissipation would be substantial in comparison with the rest of the circuit and the clock amplitude would not be externally adjustable if resistors or critical currents were not correct. One further practical difficulty is that a large, high frequency clock would be expected to cause ground bounce and reduce circuit margins while being difficult to deliver to the chip and expensive to generate.

The RSFQ comparator uses SFQ pulses and has been tested at clock rates up to 30 GHz for a 2.5 kA/cm^2 design. It is a more natural fit with the digital RSFQ circuitry needed for correcting errors and interleaving to enhance resolution. The skew of the SFQ clock may be easily zeroed by changing the dc bias currents of Josephson Transmission Lines (JTLs). While it is necessary to compensate for dynamic distortions of the thresholds at high signal speed, these are mostly linear in the signal derivative and have been largely corrected in simulations. This design appears to meet our short term goals for the ADC to be used in the HYPRES transient digitizer.

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