Multi-Channel Time Digitizing Systems

Alex Kirichenko, Saad Sarwana, Deep Gupta, Irwin Rochwarger, and Oleg Mukhanov

***Abstract*—In this paper we present an overview of a family of Time-to-Digital Converter (TDC) systems developed at HYPRES over the past several years. We have developed three types of RSFQ-based time digitizing systems: an eight-channel multi-hit 30-ps TDC, a two-channel multi-hit 6-ps TDC, and a dual-function multi-hit TDC/ADC. We present results of successful testing of an all-digital TDC up to 33-GHz clock frequency, digitizing at 30-ps time intervals. The eight-channel all-digital TDC chip occupies a 1 cm x 1 cm area with more than 10,000 Josephson junctions. For better time resolution, the digital counter-based TDC can be integrated with an analog prescaler. The prescaler improves time resolution to 6 ps and has also been successfully tested. We have also integrated TDC channel with sensitive SQUID to a dual-function ADC/TDC digitizer. An advanced VXI-based interface allows the parallel 8-channel data to be acquired at a read-out clock rate of 100 MHz.**

***Index Terms*—Time-to-digital converter, RSFQ, TDC, time-of-flight, TOF, High Energy Physics instrumentation**

I. Introduction

THE Time to Digital Converter is one of the most important tools in high-energy and nuclear physics instrumentation. Most of the experiments in these areas are related to measurements of time intervals between the signals coming from different detectors and/or digitization of these signals.

The most important parameters of a TDC are its time resolution and multi-hit time resolution. The time resolution is the precision of time interval measurement or LSB. The best commercially available GaAs-based TDCs have a 10 ps single-hit resolution. The multi-hit time resolution is the capability of a TDC channel to measure a few time intervals sequentially. To the best of our knowledge, there is no multi-hit TDC below 1 ns.

There is a growing demand for faster TDCs. For instance, time-of-flight (TOF) experiment requires fast detectors and electronics with high precision to resolve the time difference. The recent development of micro-channel plate (MCP) detectors [1] with less than 10 ps of time jitter has created the need for a higher performance TDC. Very often, a physics experiment requires a measurement of the pulse's amplitude and/or integrating the pulse from the detector along with measuring its relative time.

By using Rapid Single Flux Quantum (RSFQ) electronics [2], we have been able to create a 6-ps TDC and a 30-ps multi-hit TDC using standard HYPRES Nb/AlO_x/Nb tri-layer process [3]. We have also developed a dual-function TDC/ADC multi-channel system capable of detecting the time stamp and digitizing the same signal.

Eventually, Nb RSFQ TDC technology will surpass 2 ps resolution with improvements in lithography and critical current density. This time resolution can be accomplished using mWatts of power dissipation on a chip. Moreover, the Nb technology is naturally radiation hard [4]. That enables measurements in high-radiation accelerator laboratory environments. In addition, cryo-packaging and cooling issues, which are the usual impediment of superconductor-based systems, can be easily accommodated as the detectors are often cooled by liquid helium.

All HYPRES TDC systems are integrated with a VXI-based interface and control modules with software control and data processing, as is common in high-energy and nuclear physics instrumentation.

II. All-Digital Multi-Hit TDC

The TDC is essentially counter based and works by counting SFQ clock pulses between two successive input events (hits): each hit reads accumulated counts out, resets the counter, and shifts the data (or time stamps) to the multi-hit buffer, where it is stored until it can be read through a parallel-to-serial (P/S) converter out at low frequencies (Fig. 1).

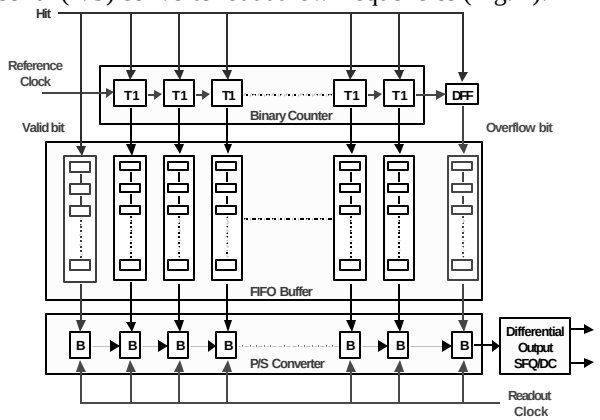

Fig. 1. Block diagram of a digital multi-hit TDC channel.

The counter-based TDC has been designed and tested in two different varieties - a nine-hit version with 1200 Josephson

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All authors are with HYPRES, Inc., 175 Clearbrook Rd., Elmsford, NY 10523, USA; ph.: (914)592-1190; fax:(914)347-2239; http://www.hypres.com

junctions per channel and a three-hit version with 750 Josephson junctions per channel.

Due to the independence of the TDC channels from each other, we can create a custom TDC system using a particular number of channels with a particular size FIFO buffer. The channels do not exchange any data, so it is relatively simple to make a multi-chip TDC module with a comparably large number of channels.

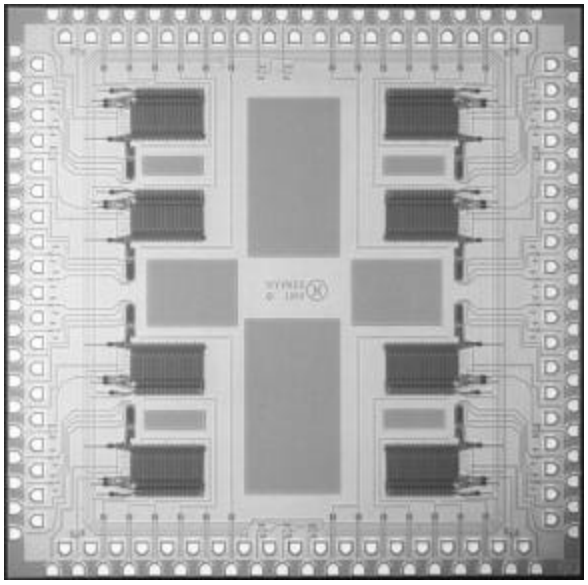

Fig. 2. Eight-channel 9-hit TDC placed on a single 1 x 1 cm chip.

Fig. 2 shows one such layout where we have integrated an eight counter-based 9-hit TDC channels on a single 1 x 1 cm chip. We have also designed the similar TDC in a 3-hit version and a two-channel 9-hit TDC fit in a single 5 x 5 mm chip. This design flexibility allows us to build a variety of custom TDC systems.

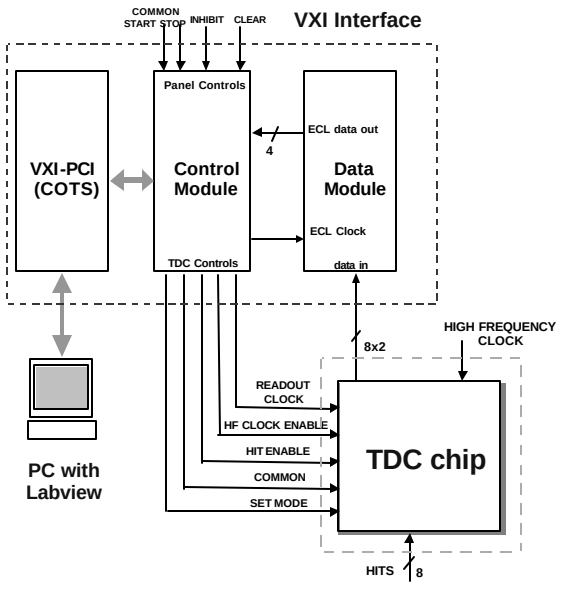

Fig. 3. System-level structure of TDC system.

All TDC systems are integrated with a VXI-based interface very common for physics instrumentation. The general system setup is shown in Fig. 3. The system hardware is transparent to design changes and specifications of the RSFQ circuit (e.g. clock frequency, multi-hit buffer depth, or number of channels).

The interface is controlled through custom LabVIEW software. A more detailed description of the interface and its specifications and control software is provided in [5].

A. Low-Frequency Functionality Test

Previously, we reported results on a single TDC channel operating at 33 GHz [6]. We have now obtained both low- and high-speed test results on a 9-hit multi-channel TDC.

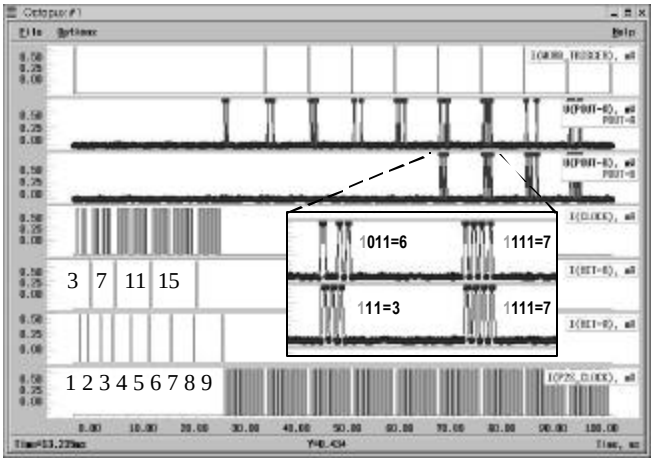

Fig. 4. Automated low frequency test results for two channels of 9-hit TDC. It shows correct operation at +/- 10% bias current margins.

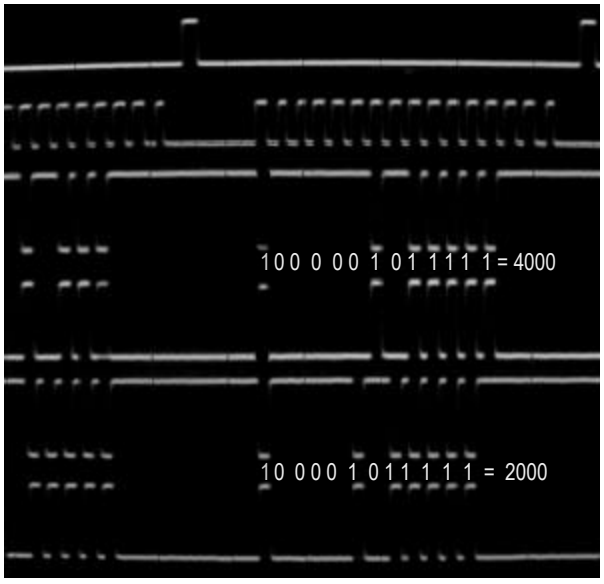

Fig. 5. Two channels of the TDC operational at 1 GHz clock with 2 μs and 4 μs as the time in between events correctly represented as counts of 2000 and 4000 of 1-ns time intervals.

For the functionality test, we use an automated low-speed test setup "Octopux" [6]. The setup allows us to generate input patterns of any complexity and is capable of monitoring and verifying the output. Fig. 4 shows the correct low-speed

operation of the two-channel TDC. Here, we have applied a simple pattern so that the number of clock pulses between nine consecutive *Hits* on the first channel increases from 1 to 9 and the sequence 3-7-11-15 to the second channel. The LSB (leftmost bit) in each word is necessary for data processing and is not a part of the read-out number.

B. Direct High-Frequency Test

Fig. 5 shows operation of both TDC channels at a 1-GHz input clock frequency. Two different events, 2 μs and 4 μs, are correctly represented as counts of 2000 and 4000 respectively. The smallest operating margin on DC bias currents was greater than 10%.

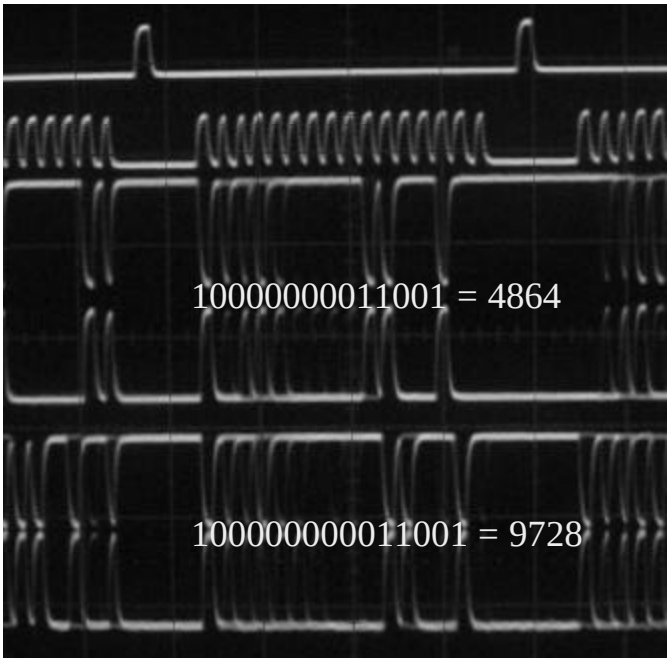

Fig. 6. Two channels of the TDC operational at 12.16 GHz clock with 0.4 μs and 0.8 μs as the time in-between events correctly represented as counts of 4864 and 9728 from the counters.

Similar test results at 12.16 GHz are shown in Fig. 6. In contrast to the previous results, one can see a substantial jitter in the first four bits. This is related to the phase noise of the pattern generator used in the experiment (< 1 ns, according to the manufacturer). This causes all trailing zeros to toggle to "1" spontaneously.

We could not test all eight channels simultaneously yet, mainly because of fabrication yield and testing equipment issues.

C. High-Frequency Test with VXI Interface

We have successfully tested the TDC at high speed with a VXI-based interface. Fig. 7 shows test results of the TDC at 20-GHz clock using the VXI interface. The first channel of the 1-ns pattern generator generated *Common Start* and *Common Stop* signals necessary to initiate the interface and synchronize TDC channels by initiating counters. The second generator channel produced the *Clock Enable* signal, which controls the switch, allowing HF clock to propagate to the counter. The third generator channel generated three *Hit* signals 2 ns and 5 ns apart. Thus, we had four measurable time intervals. After a few hundred cycles, the interface stored raw data onto disk. Then, the data was processed and plotted as a time-stamp histogram. As one can see, Fig. 7 (bottom) contains substantial phase noise (jitter), induced by the pattern generator.

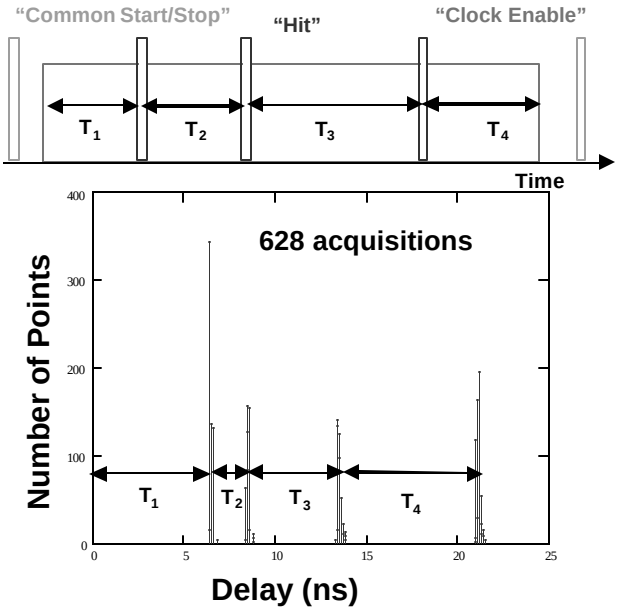

Fig. 7. A 20-GHz test of the TDC channel with pattern generator. A 1-ns pattern generator was used to produce three hits 2 and 5 ns apart. The spread in the data comes from the phase noise in the pattern generator.

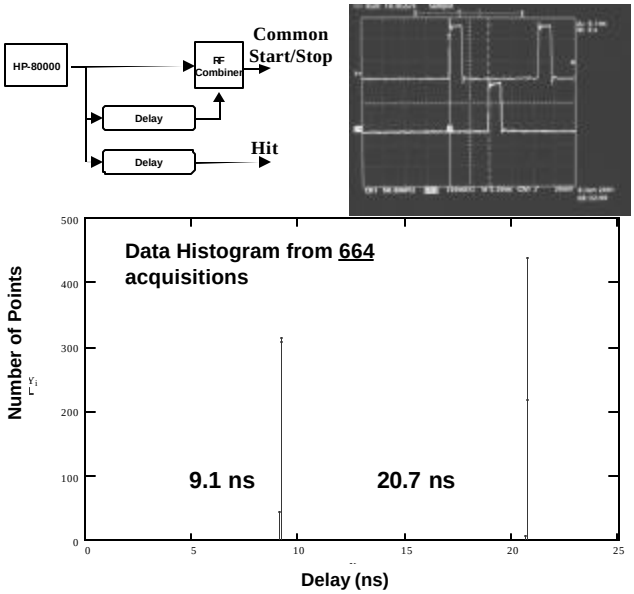

Fig. 8. A 20-GHz TDC test with a low time jitter setup. We used a single start event, split it in two and applied it to the Hit input after a passive delay. This removed jitter/phase noise in pattern generator.

To circumvent this jitter problem, we developed a test

method based on passive delays, RF splitters, and RF combiners (Fig. 8). We generated a single clock pulse for the Common Start signal, split it in two, delayed it with an analog delay line, and then used this signal as a *Hit*. Using this method, we were able to test the chip at a 20 GHz clock frequency and to substantially reduce the time jitter down to 50 ps. It is important to note that the LSB jitter is unavoidable because of the asynchronous nature of the *Hit* signals.

III. HIGH-RESOLUTION TDC

To improve timing resolution, we have also integrated a digital TDC with an analog prescaler, which works like a vernier scale [7]. The key to the prescaler approach is to race the *Hit* signal against Clock pulse, thus detecting the *Hit* arrival time by fractions of the clock period.

To test the analog prescaler, we split a Hit pulse from the *Clock* as shown in Fig. 9. The main idea was to send one of these pulses through a controllable JTL delay line. By scanning the delay line bias (and hence effectively controlling the speed of the SFQ pulse propagation), we could verify the response of all eight prescaler bins.

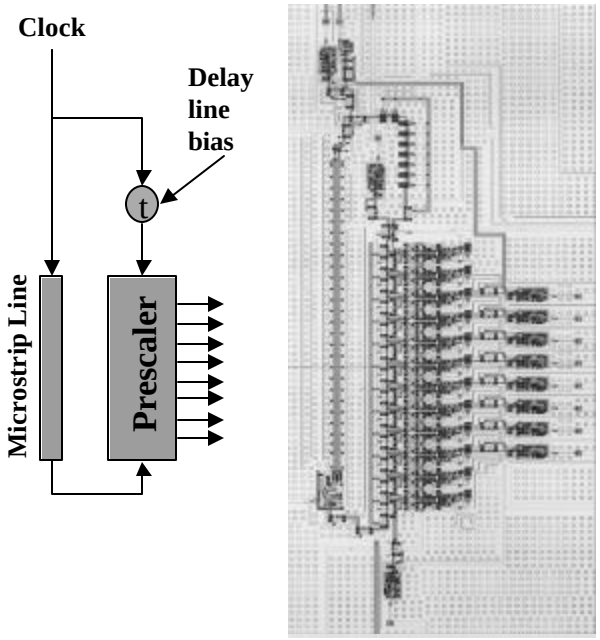

Fig. 9. (a) Block diagram of test chip for the prescaler. (b) Chip layout.

Fig. 10 shows the high-speed test results. Each output toggles at high frequency (single line in eye diagram) at the bin where two SFQ pulses are coincident in the aperture. If we apply a ramp signal to the delay line bias, we should be able to adjust the position of this overlap and spread it out between one of the eight possible time windows. When not toggling, the outputs can be in either high or low state (double line).

Using the 8-bin prescaler, we were able to improve TDC time resolution from 50 ps to 6 ps while maintaining the same 20-GHz clock frequency.

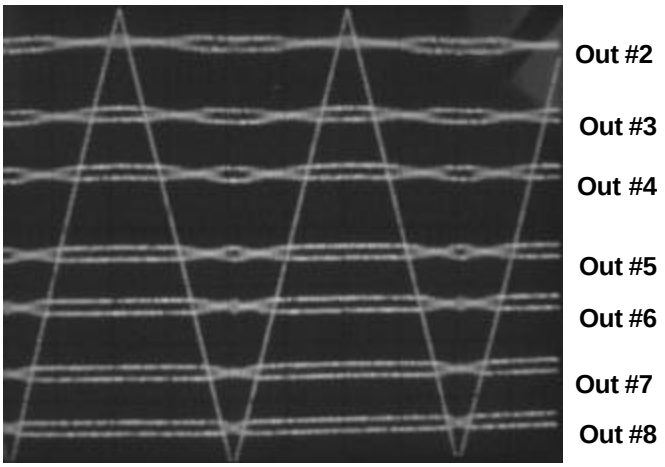

Fig.10. Eye diagram of output of the prescaler, with ramp signal applied to delay line.

IV. DUAL-FUNCTION ADC/TDC

To answer the growing demand in physics instrumentation for dual-function digitizers, we have also designed, fabricated, and successfully tested a dual-function TDC/ADC channel [9]. Fig. 11 shows a block diagram of the dual-function digitizer.

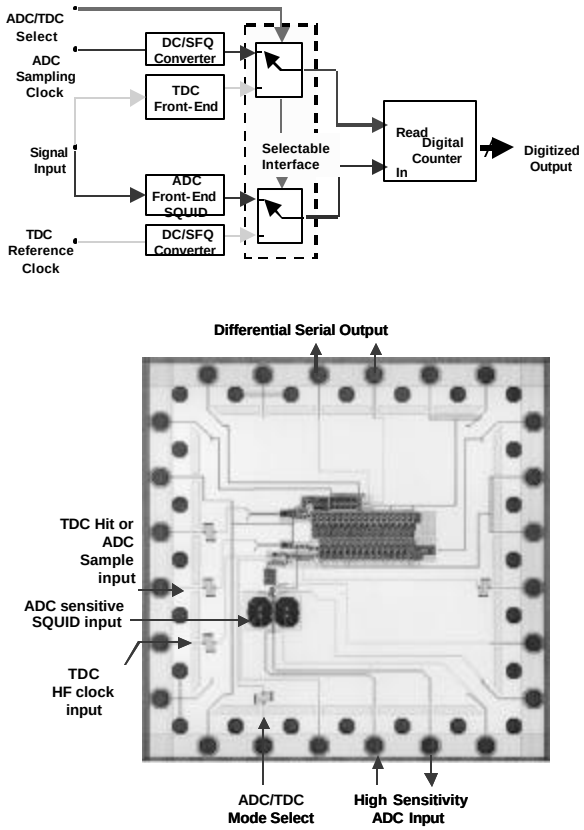

Fig. 11. Schematic diagram and the chip layout of a single channel of the dual-function ADC/TDC digitizer.

This circuit comprises the TDC channel shown in Fig. 1 with swappable front-ends. In ADC mode, the digitizer accepts input signals through a sensitive SQUID connected to the

clock input of the TDC. The SQUID converts the input current pulse into magnetic flux and produces corresponding number of SFQ pulses. The TDC counter counts the number of SFQ pulses, producing a read-out equal to a size of the measured input pulse. When the sampling clock is applied to the TDC Hit input, the input current becomes digitized with the corresponding sampling rate. In many cases it is enough just to measure the total area of the pulse, e.g. when the response of a detector is correlated with the energy of the particle. Using a sensitive SQUID as an ADC front-end, we have successfully conducted the pulse digitization experiment (Fig 12).

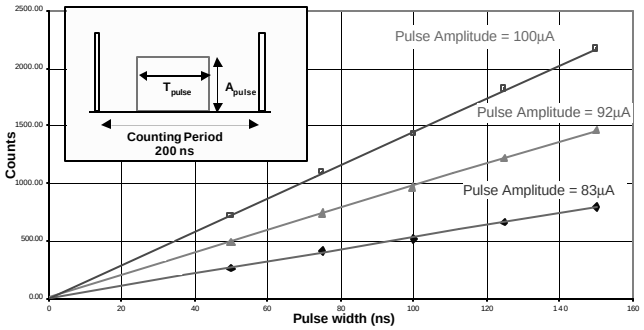

Fig. 12. Pulse digitizing with the dual-function ADC/TDC.

To perform this test, a current pulse of variable width (T_{pulse}) and amplitude (A_{pulse}) was applied. The output of the counter represents the total charge of the pulse. Fig. 12 shows the ADC output for three different pulse amplitudes, each for five different pulse widths. These results show excellent agreement with the theory. The linear curve fits through the count outputs for the same amplitude and different widths are also shown. This test confirms the ability to digitize the charge of a pulse.

We can integrate up to eight channels on a 1x1 cm^2 chip, thus giving the user a flexible multi-channel digitizer. If a user applies the same signal to two channels and switches one of them into ADC mode, he can digitize and time-stamp the signal at the same time. A detailed description and the test results are in [9].

V. Conclusion

We have developed and demonstrated three complete time digitizing systems: a multi-hit all-digital 30-ps TDC, a 6-ps (50-ps multi-hit) resolution TDC, and a dual-function ADC/TDC. Each consists of a superconductor RSFQ TDC chip, a custom built VXI interface, and a PC with controlling LabVIEW software. The same VXI interface system with minor differences in software can serve the 8-channel digital TDC, the 4-channel high-resolution TDC, or the 8-channel ADC/TDC. We have also demonstrated a digital multi-hit TDC working at 33 GHz clock frequency, and a high-resolution TDC showing 6 ps time resolution.

The two-channel high-resolution TDC is going to be used at the Mu-cool experiment at the Fermi National Accelerator Laboratory.

We are also looking into scaling this design down to smaller junctions (thus increasing clock speed) as well as using on-chip clock generators to circumvent the need for an external high frequency clock source.

Acknowledgment

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