E4.6
Analog-to-digital converters

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E4.6.1 Introduction

Analog-to-digital converters (ADCs) are electronic circuits that convert an electrical signal from the analog domain (e.g., a continuous current or voltage) to the digital domain of binary numbers, which can then be processed by computers. Not only have measuring instruments become digital, but so increasingly have consumer electronics, communications systems, and a wide variety of sensors. All of these require the use of ADCs. An ADC typically provides an N-bit binary measurement (where N is a positive integer) at a rate known as the sampling frequency f_s. Superconducting ADCs can provide more bits at a higher f_s than any other (semiconductor-based) technology, and are at the threshold of commercialization. A digital-to-analog converter (DAC) functions in the reverse direction, converting a sequence of binary numbers into a continuous electrical signal, and high-performance superconducting DACs are also beginning to be developed.

The previous chapter on high-speed digital logic (E4.5) explained that Josephson junctions exhibit switching speeds of the order a few picoseconds or less, making them suitable for the highest-speed logic circuits for computers and digital signal processors. The earlier chapter on SQUIDs (E4.2) addressed the quantum-limited sensitivity and linearity of these devices for measuring magnetic fields and currents. Superconducting ADCs incorporate both SQUIDs and Josephson logic, and it is this unique combination of speed, sensitivity, and dynamic range (which follows from linearity) that make the Josephson ADC so powerful. Earlier reviews of superconducting ADCs include those by Gerritsma [7] and Przybysz [15].

E4.6.2 ADC basics

A classical analog signal has a continuously variable magnitude with continuous time as the independent variable. For example, a voltage $V(t)$ or a current $I(t)$ can, in principle, be measured to any desired precision at any arbitrary time. In contrast, a digital representation of that signal consists of a series of numbers, typically integers, that approximate the continuous signal with discrete values at a set of discrete times. As shown in figure E4.6.1(a), this is equivalent to representing the signal by nearby points on a regular grid. There are two distinct aspects of this process: *sampling* and *quantization*, which deal with discretization in time and magnitude, respectively. Sampling refers to the set of discrete times at which the signal is measured or 'sampled'. This time base is typically provided by a periodic sampling clock that takes a new sample at every 'tick' of the clock. The time needed to carry out this sampled measurement is known as the 'aperture time' τ, and must be significantly smaller than the sampling period T_s.

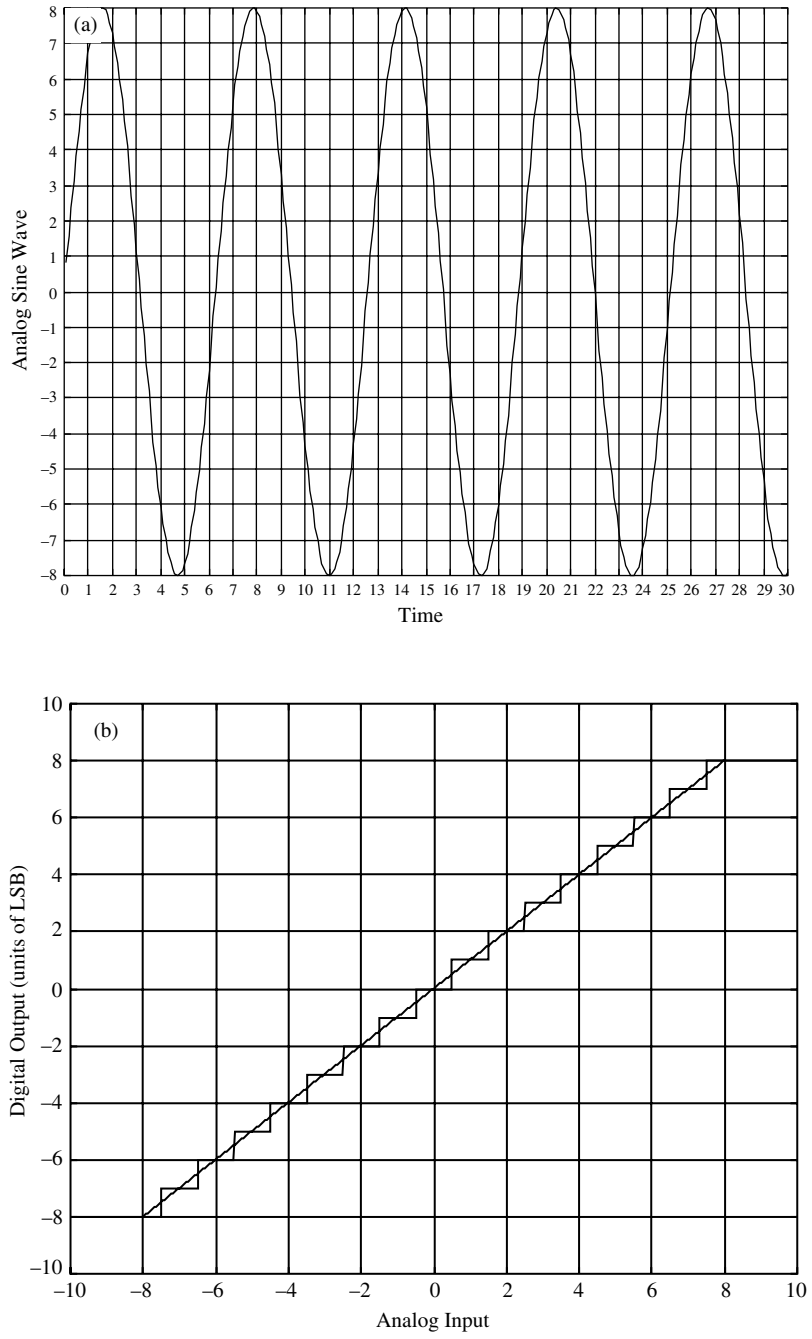
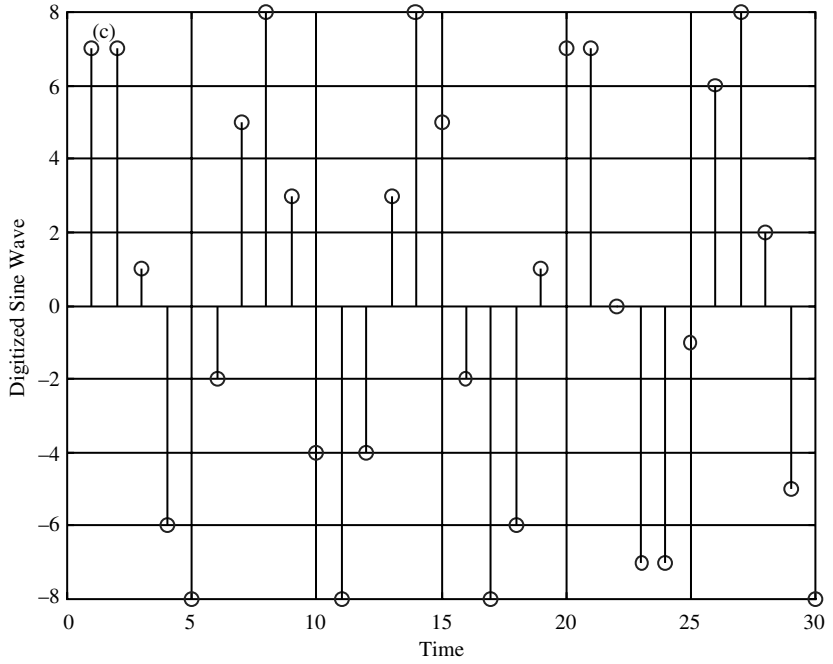


Figure E4.6.1. General representation of analog-to-digital conversion. (*a*) Input analog sine wave, showing grid that represents discretization in time (sampling) and amplitude (quantization). (*b*) Staircase quantization function with quantization level (or LSB) Δ and maximum amplitude A_{sat}, giving effective range $R = A_{\text{sat}}/\Delta$. (*c*) Reconstructed digitized output. (*d*) Power spectrum of digitized output (Fourier transform of plot in (*c*)) up to Nyquist frequency f_{N}, showing SFDR.



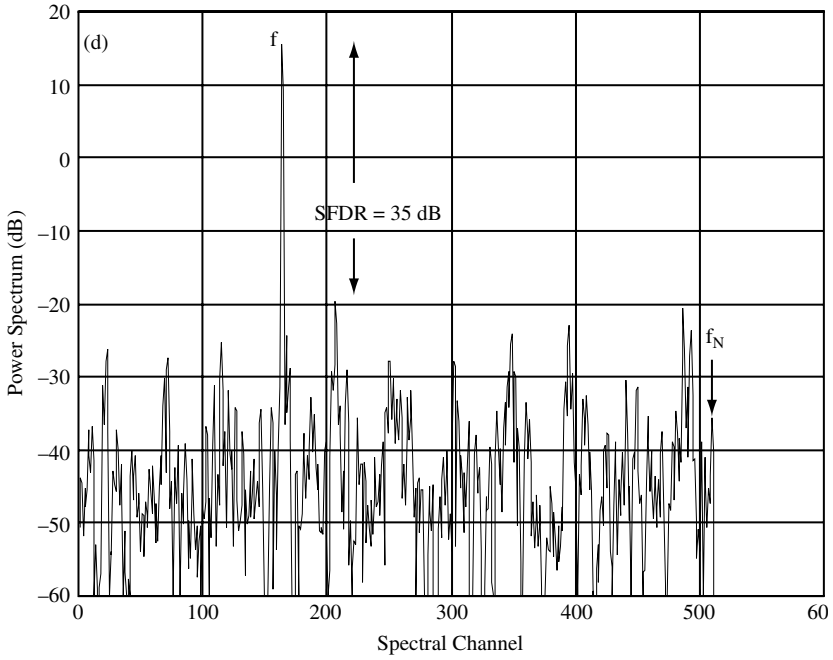


Figure E4.6.1. (Continued).

Quantization refers to the selection of a discrete value for the magnitude when the signal is sampled, and is carried out by a quantizer. A typical quantization function is given by the staircase function in figure E4.6.1(*b*). The resolution of this quantization is given by the size of the step, which represents the quantization level, sometimes indicated by Δ (not related, of course, to the superconducting energy gap). The size of the signal can then be represented by the nearest integer multiple of Δ. In principle, this quantization function could apply for arbitrarily large magnitudes, but the quantizer in any real ADC exhibits a maximum value or saturation level A_{sat}. The maximum input range of the quantizer is thus given by the ratio $R = A_{\mathrm{sat}}/\Delta$. The 'dynamic range', conventionally defined in terms of power ratios, is then given by R^2.

Digital circuits are generally implemented using binary logic, based on powers of two. For this reason, the quantization level Δ is often called the 'least significant bit' or LSB, and the maximum value the 'most significant bit' or MSB. The maximum input range R is often a power of two, and can be represented in numbers of bits $N = \log_2(R)$. For example, in figure E4.6.1(*b*), there are eight quantization levels for each sign, corresponding to a quantizer with a dynamic range of $\log_2(8) = 3$ bits. (Sometimes one additional bit is added for the sign.) Alternatively, from the analog side, signals are often represented in decibels (dB), where $R_{\mathrm{dB}} = 20\log_{10}(R)$ or 6.02 dB per bit, so that the dynamic range in figure E4.6.1(*b*) can be quoted as 18 dB. A practical high-performance ADC may have a dynamic range of 10 bits ($R = 1024$ or 60 dB) or more.

For an ideal analog signal with no noise, the quantization process introduces some error into the system. In the ideal case, the error falls in the range from $-\Delta/2$ to $+\Delta/2$ with uniform probability. This corresponds to an average variance of $\Delta^2/12$, or a standard deviation $\sigma = \Delta/\sqrt{(12)}$. This error is often referred to as 'quantization noise', and is treated as if it were a source of input noise added to the signal. Of course, this is in addition to any analog noise present in the signal, as well as other sources of non-ideal quantization error, such as jitter in the sampling clock.

Even if the quantization is arbitrarily precise, the clock frequency will limit how accurately a signal may be represented in the digital domain. According to the Nyquist sampling theorem, a signal that is sampled at a frequency f_{s} can accurately represent an analog signal with frequency components up to the Nyquist frequency $f_{\mathrm{N}} = f_{\mathrm{s}}/2$. In fact, any frequency above f_{N} should be filtered out of the input; otherwise, it will create a false signal below f_{N}.

So an ideal Nyquist ADC samples a bandwidth-limited signal at a sampling rate f_{s} and provides an accurate digital representation of that signal, with the only error associated with the quantization noise. For a classic ADC, the quantizer is composed of a large number of separate comparators, each defining a single quantization level. In practice, the performance of such an ADC is limited by the precision of the quantization levels, which are often determined by resistors in resistor networks. It is essential that the difference between consecutive levels should be close to Δ, but in addition, the linearity across many levels must be preserved. Otherwise, a sinusoidal input signal at f would generate harmonic frequencies ($2f, 3f$, etc.) at the output.

Many modern ADCs use an alternative approach to obtain greater precision while requiring fewer comparators. This involves 'oversampling', in which the signal is sampled at a frequency $f_{\mathrm{s}} \gg 2f_{\mathrm{N}}$. Then, digital averaging and feedback techniques can be used to decrease the quantization noise and enhance the effective dynamic range. The most common conventional design for such an oversampling ADC uses a 'delta–sigma (or $\Delta\Sigma$) modulator' (sometimes called 'sigma–delta') and a single-bit comparator. Here Δ refers to the difference and Σ to the sum, the discrete analogs of differentiation and integration. In this approach, the quantized signal is fed back to the input, and the resulting difference (Δ) is integrated (Σ) before entering the quantizer. This gives rise to both increased dynamic range and decreased in-band quantization noise ('noise-shaping'), at the expense of increased circuit complexity. A recent review of conventional (semiconductor) delta–sigma ADCs is given by Norsworthy [14].

There are several standard figures of merit for conventional ADCs. Typically, a sinusoidal frequency at a fixed frequency f is sent into the ADC, and the reconstructed digital output and its Fourier spectrum are measured (figure E4.6.1(*c*) and (*d*), respectively). The signal-to-noise ratio (SNR) is the ratio of the signal power to the total noise power in the output bandwidth, and is typically quoted in dB. A closely related quantity is the effective number of bits (ENOB), which is defined by the equation $\mathrm{ENOB} = (\mathrm{SNR}_{\mathrm{dB}} - 1.76)/6.02$. (The offset of 1.76 dB is related to the noise level of $\Delta/\sqrt{(12)}$.) The ENOB is typically somewhat smaller than the number of binary bits provided by the ADC, and accounts for several possible sources of noise. A distinct figure of merit is the spur-free dynamic range (SFDR), which is obtained from the frequency spectrum of the reconstructed output. It represents the ratio of the signal power to that of the highest spur (or spurious signal) within the relevant frequency band, and is usually expressed in dB (or sometimes in bits, by dividing by 6.02). The SFDR is typically somewhat larger than the SNR because the entire noise is not concentrated in a single peak. The SFDR is often a better measure of nonlinearity than the SNR, since the highest spur is often at the second or third harmonic of the signal.

There is a general trade-off between the dynamic range of an ADC and the frequency bandwidth for any given device technology; the range decreases approximately in inverse proportion to the maximum frequency. This is partly because the device switching speed determines the maximum sampling frequency, which in turn limits the gain that may be obtained by oversampling a high-frequency signal. In addition, the larger bandwidth of higher frequency signals increases the total noise, thus reducing the effective number of bits. A summary plot of high-performance ADCs is shown in figure E4.6.2 (similar to that in [24]), where the SFDR is plotted versus the bandwidth for signals close to the Nyquist frequency. The best performers for semiconductor systems are generally fabricated from fast III–V circuits (GaAs or InP). Some recent data from Josephson ADCs are also shown for comparison. Even in this early stage of development, using lithography with modest 3-μm linewidths, the Josephson ADCs perform at or better than the best semiconductor ADCs. Further improvements are anticipated as the lithographic scale and circuit yield are improved.

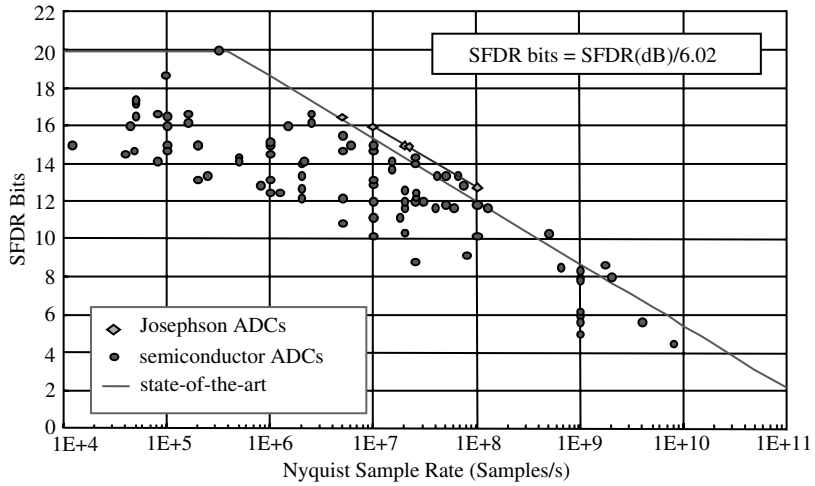


Figure E4.6.2. Plot of SFDR versus sample rate (for signal at Nyquist frequency) for high-performance semiconducting and superconducting ADCs (from [13], semiconductor data adapted from [24]). Superconducting ADCs are already at or beyond the limit of the best semiconducting ADCs, with further improvement expected in the near future.

The same issues of dynamic range and bandwidth are relevant for a DAC, which can function as a direct digital synthesizer (DDS) of a high-frequency signal. A high sampling rate with good linearity is necessary for high fidelity to the desired signal, and a DAC can be characterized by parameters of SNR and SFDR in much the same way as an ADC. Josephson DACs are just beginning to be developed, but show great promise for high-precision electronic sources.

E4.6.3 Types of Josephson ADCs

Josephson junction circuits have several fundamental aspects that make them ideal for ADCs. The most important is the natural periodicity of the SQUID or Josephson junction with period $\Phi_0 = h/2e = 2.07\,\text{fWb} = 2.07\,\text{mV ps}$, the magnetic flux quantum. SQUID characteristics are periodic in applied flux Φ/Φ_0, and a voltage V generates a periodic oscillation at the Josephson frequency V/Φ_0. In principle, one has to only count the number of periods with a binary counter to obtain a digital output. This periodicity is intrinsically linear over a very large range, and combined with the ultra-low-noise properties of a SQUID, one should obtain a large SNR. Finally, damped Josephson junctions are the basis for ultrafast RSFQ logic circuits (rapid single flux quantum—see chapter E4.5), with switching speeds of a few picoseconds. So Josephson ADCs should permit very fast (multi-GHz) sampling.

As with conventional ADCs, the two main classes of Josephson ADCs are Nyquist-sampling and oversampling converters. One type of the former class is the 'flash-ADC', with a one SQUID comparator for each bit [1], and several bits in parallel. This circuit uses a regular R–2R resistor network to reduce the input current by a factor of two for each successive bit, each of which is encoded using a SQUID comparator with a periodic threshold. The direct digital output is actually in 'Gray code' rather than standard binary, but code conversion is straightforward. A 6-bit flash-ADC of this design has been demonstrated to operate at greater than 10 GHz Nyquist bandwidth (20 GSamples/s sample rate), as part of a transient digitizer instrument ([10], see also below).

There have been several successful designs of oversampling ADCs, each based on a 1-bit Josephson quantizer generating SFQ pulses. In one circuit, an 'oscillator-counter ADC' [9, 12], a voltage signal is applied directly across a Josephson junction, which generates SFQ pulses at a rate proportional to the signal (with an offset to permit negative voltages to be measured). These are counted with an RSFQ binary counter that can operate up to 120 GHz, with the values read out at a lower sampling frequency up to a few GSamples/s [9]. A higher dynamic range should be possible using a Josephson sigma–delta ADC, and several designs have been developed [8, 26], including a bandpass modulator for narrow-band analog signals [3].

A complete high-resolution broad-band superconducting ADC system has been successfully demonstrated based on a phase-modulation ADC [13, 18]. In this system, the signal current is coupled inductively to an input SQUID using a multi-turn coil (see figure E4.6.3). Even without a signal, the SQUID is already generating pulses due to a dc-applied voltage. The signal modulates the pulse rate, providing a pulse position modulation (or phase modulation) that is proportional to the time derivative of the input signal. This 1-bit output is subsequently synchronized to a clock frequency of 10–20 GHz, and these pulses are further summed and averaged on-chip (in a digital decimation filter—see below) to obtain a 15-bit output signal at a reduced sampling rate. Measurements on this system for a 50 MHz sine wave with full-scale amplitude yield an output (averaged to the Nyquist frequency) with an SNR of 58 dB and an SFDR of 80 dB, in good agreement with theoretical simulations. With further enhancements in lithography and design, this performance can be extended into the GHz range.

An alternative to the delta–sigma modulator is the 'delta-modulator' [19], in which a feedback signal is applied to take one or more discrete derivatives of the input signal. Under appropriate conditions, this can lead to substantial decreases in noise and increases in the total dynamic range.

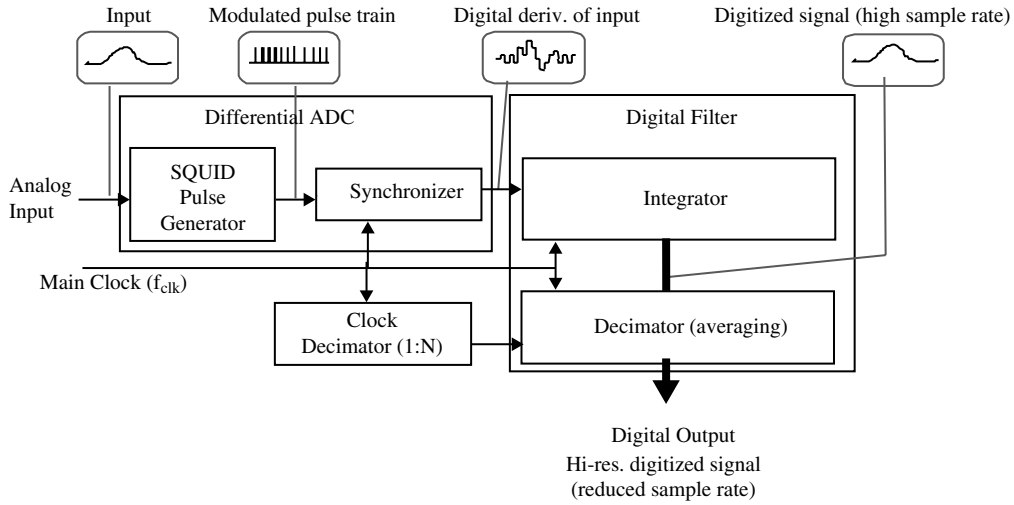


Figure E4.6.3. Block diagram of phase modulation ADC. The signal is inductively coupled to a voltage-biased SQUID, which acts as a pulse modulator. The pulse train is synchronized to generate a differential digital code for the signal, which is subsequently integrated and averaged in an on-chip digital decimation filter. The final output at a reduced sample rate (~ 200 MHz) is transmitted to room-temperature electronics.

Finally, there has been continuing progress in developing a complete integrated digital SQUID magnetometer, where the SQUID signal is digitized and the feedback is applied on the superconducting chip [16]. Although this was not initially designed as a general-purpose ADC, with a different input coupling coil, this could equally well be used to digitize voltage or current signals, with the high precision that the SQUID is known for.

E4.6.4 Related circuit components

For an oversampling ADC to operate most effectively, one needs to include a digital filter to decrease the output bandwidth to the Nyquist frequency. In the field of digital signal processing, this is known as a 'decimation filter'. The simplest (first order) decimation filter takes the average of a sequence of n samples, which reduces the bandwidth by a factor of n. Assuming that the quantization noise of sequential samples is essentially uncorrelated white noise, the noise level decreases as $n^{1/2}$, thus improving the SNR and dynamic range. Given the very high initial sampling rate of Josephson circuits (up to 20 GSamples/s or more), the initial stages of this decimation filter must be implemented using RSFQ logic on the same chip as the 1-bit quantizer. Complete 18-bit filters of this type have been demonstrated to operate at frequencies up to 20 GHz, with programmable decimation factors up to 128 [4].

This section has been focused primarily on ADCs, but the reverse process of analog waveform generation is also quite important, and is subject to many of the same concerns of dynamic range and bandwidth. In a sense, the Josephson dc voltage standard is a DAC, albeit a rather slow one. Efforts in recent years have been pursued to generalize this dc voltage standard to an ac voltage standard or even an arbitrary waveform generator [2], in which a digitally generated SFQ pulse train is applied to a series array of Josephson junctions, which in turn generate a voltage proportional to the pulse rate. With the appropriate output filtering, this reproduces a high-resolution analog signal. In addition, there have also been efforts to develop a high-speed DAC, also based on SFQ pulses, for use as a feedback element in a high-performance ADC [20].

E4.6.5 Materials and systems for Josephson ADCs

As described earlier, Josephson ADCs are medium-scale integrated circuits, requiring hundreds or thousands of Josephson junctions for complete systems. As such, they require a well-controlled integrated circuit foundry, with reproducible junction properties. For this reason, complete circuits have been demonstrated thus far primarily using niobium Josephson junctions, operating at about 4 K. As described in chapter E4.1 on Josephson junction properties, these Nb junctions are generally prepared using a standard multilayer process based on $Nb/AlO_x/Nb$ trilayer tunnel junctions, with critical current densities of the order of 1000 A cm^{-2} for junctions on the scale of several microns. Since critically damped junctions are generally needed for these circuits (to avoid hysteretic I–V characteristics), they also require resistive shunts around the junctions, typically made using a metallic layer such as Mo or Pd which is not superconducting (at 4 K). The circuits also require inductors, which are generally composed of Nb microstriplines, separated from the ground by an SiO_2 insulating layer. The standard process for making ADCs is practically identical to that for making Josephson junction RSFQ logic circuits, SQUIDs, and Josephson voltage standards. These circuits are often operated immersed in a liquid helium bath, but can also function well when mounted on a close-cycle refrigerator (or cryocooler) that maintains temperatures in the range 4–5 K. The total heat dissipation of such a circuit is very small, well below 10 mW, so that a properly designed cryopackage that minimizes external heat leaks can operate with less than 100 mW of the total cooling power.

Josephson ADCs operating at higher temperatures are also of interest. Josephson junction integrated circuits based on niobium nitride (with T_c up to about 17 K) have also been demonstrated (see chapter E4.1), using MgO as an insulating tunnel barrier. NbN counting-type ADCs with 16-bit resolution have been demonstrated to operate at 10 K [22].

Operation at even higher temperature is possible using the high-temperature cuprate superconductors. There have been major efforts to develop a reproducible technology for Josephson junctions based on $YBa_2Cu_3O_7$ (YBCO), although the high temperatures required for epitaxial deposition of these materials make a true multilayer process difficult to achieve. There has been some success in obtaining damped junctions with the I_cR_n product of order 0.2 mV, with uniformities in critical current of better than 10%. For medium-scale integrated circuits, one needs better uniformity and higher yield, but key components of ADCs, including a 1-bit sigma–delta modulator, have been demonstrated [5, 11, 17, 21]. Such an HTS circuit could operate at temperatures up to about 40 K and possibly higher.

E4.6.6 Applications

As mentioned earlier, there are a number of important areas of scientific instrumentation in which the precision, speed, and dynamic range of superconducting ADCs are of great interest. In addition to a digital SQUID magnetometer [16, 23], one such application is to a transient digitizer with application to nuclear and high-energy physics, such as fast laser fusion diagnostics [10]. Another developing application may be for infrared focal plane detector arrays, where digital sampling and preprocessing at the cryocooled focal plane using NbN circuits have been demonstrated [22]. Also, a Josephson DAC can be used for high-precision digital generation of arbitrary waveforms [2].

In addition to the applications to scientific instrumentation, there has recently been much attention to major commercial applications to the wireless communications industry and related technologies in the radar and defence sectors. These applications have in common the requirement of directly digitizing (or synthesizing) rf signals, with GHz sampling and high dynamic range (> 14 bits). These processes are now performed using one or more steps of analog mixing and amplification, which introduce excess nonlinearity and noise into the signal. Furthermore, there are now several different protocols for

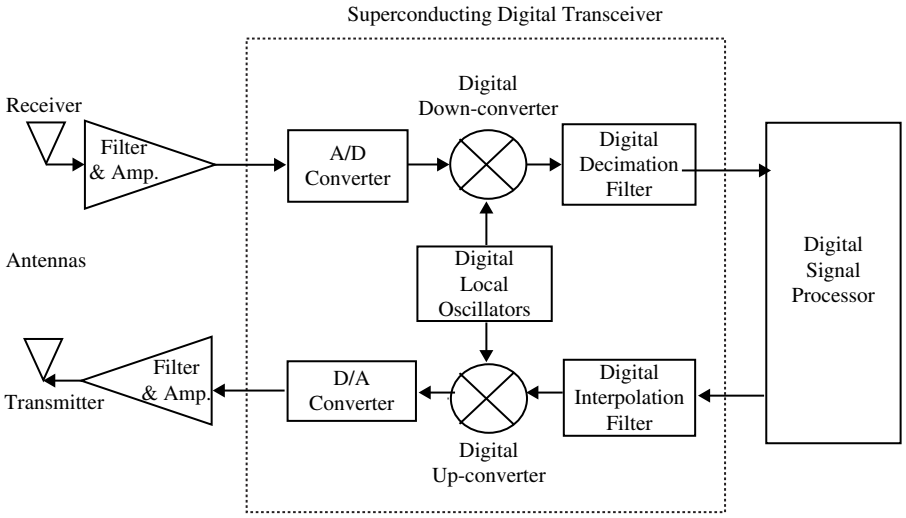


Figure E4.6.4. Schematic block diagram of digital rf transceiver for a software radio system. The Josephson ADC and DAC are the key enabling components of such a system. Digital filtering and digital mixing would also probably be carried out using RSFQ circuits.

different kinds of signals (voice, data, video) often sharing the same or adjacent bands. Conventional technology requires a separate analog receiver and transmitter for each such protocol and sub-band. In contrast, a 'software radio system' could include a single universal receiver and transmitter (or 'transceiver'), with all of the special-purpose processing being carried out digitally [6, 25]. These digital rf conversions cannot be achieved by conventional semiconductor ADCs and DACs, but should be possible in the near future with state-of-the-art superconducting integrated circuits (see figure E4.6.4).

Of course, these kinds of commercial applications will demand remote operation without the use of liquid cryogens, requiring the development of systems built around high-reliability cryocoolers. Superconducting mobile phones are highly unlikely, but rf transceivers in fixed base stations are quite conceivable. Similar systems are already being successfully operated for HTS microwave analog filters in cellular base stations, so this should not be a major barrier for commercialization of superconducting digital rf systems. The next few years will determine whether this will become a major commercial application of digital superconducting electronics.

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