Hypres MCM Process Design Rules

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Revisions:

12 April 2016

1. Reduced minimum circular bump diameter to 15 µm (Rule 9.1)
2. Reworded Rule 9.2 as minimum bump edge-to-edge spacing of 15 µm.

18 June 2015

1. Removed rule 9.4 and reference to I3 in rule 9.5 since I3 dimensions are solely determined by R3.
2. Renumbered Rule 9.5 to Rule 9.4

08 May 2015

1. Removed "two" in the physical layer properties of I1 in Table 3.1.
2. Corrected the specific capacitance of I1 layer to 0.21 fF/μm^2.

26 March 2015

1. Changed minimum bump pitch to 60 µm. (Layout Rule 9.2)
2. Added recommended design layout rule flip chips designed in HYPRES (Layout Rule 9.5) and MIT-LL SFQ4ee (Layout Rule 9.6 and 9.7).
3. Added minimum chip separation for MCM carrier (500 µm for 5mm flip chips).
4. Added information on post-bonding alignment accuracy (+/- 3 µm)

Preface

This document defines the layout design rules for the HYPRES MCM process. This information constitutes a self-contained guide to the physical layout of flip-chip based multi-chip module carriers.

1.0 General Description

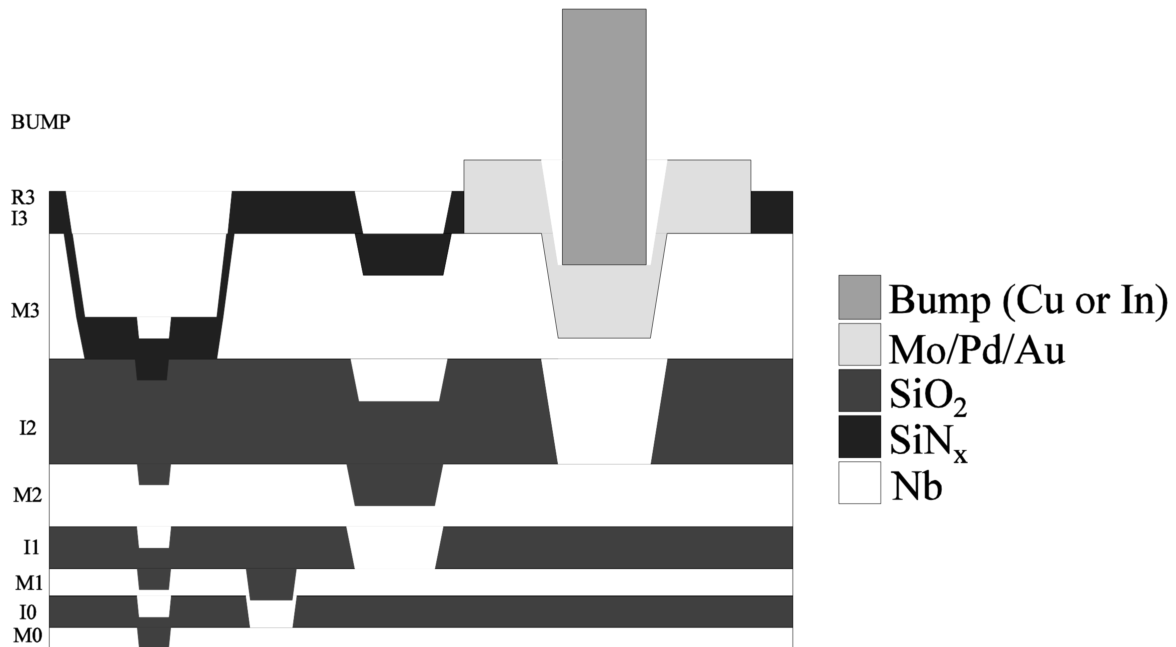
1.1 The Hypres MCM process uses Nb for the superconducting metal layers, Pd/Au metallization layer for the contact pads, and Cu or In for the wafer-level bump layer. Niobium is used as the superconducting material due to its comparably high critical temperature, electrical and thermal stability, and ability to be thermally cycled many times without degradation. All layout features are defined by 1X photolithography and etching.

1.2 SiO_2 is deposited to provide insulation between the superconducting layers, except for I3 which uses SiN_x.

1.3 The process uses 6-inch (150 mm) diameter oxidized Si wafers.

1.4 HYPRES MCM Process Flow Overview

Layer Name	GDSII Layer Number	Mask Polarity	Description	
			Nb deposition	
M0	**30**	**-**	M0 layer patterning	
			SiO_2 deposition	
I0	**31**	**-**	Contact (via) between M1 and M0	
			Nb deposition	
M1	**1**	+	M1 layer patterning	
			SiO_2 deposition	
I1	**3**	**-**	Contact (via) between M2 and M1	
			Nb deposition	
M2	**6**	+	M2 layer patterning	
			SiO_2 deposition	
I2	**8**	**-**	Contact (via) between M3 and M2	
			Nb deposition	
M3	**10**	+	M3 layer patterning	
			SiN_x deposition (I3 – passivation layer)	
I3			Patterning (contact pad between R3 and M3, using R3 layer)	
R3	**11**	+	R3-image reversal patterning for contact pad	
			Pd/Au contact metallization evaporation	
			R3 layer lift-off	
BUMP	**15**	**-**	Wafer level bump patterning	
			Copper evaporation	Indium electroplating
			Lift-off	



2.0 Layout Design Rules

2.1 Minimum size, spacing, and surround (where applicable) for each layer is specified below. Minimum size refers to drawn size on the wafer and not on the mask. See table 3.1 for appropriate bias value.

M0		
Rule	**Description**	**µm**
1.1	M0 spacing to M0	2.0
1.2	M0 minimal size	2.0
1.3	M0 spacing to I0	1.5
1.4	M0 spacing to M1	1.0
I0		
Rule	**Description**	**µm**
2.1	I0 minimum size	2.5
2.2	I0 surround by M1	1.5
M1		
Rule	**Description**	**µm**
3.1	M1 spacing to M1	2.5
3.2	M1 minimum size	2.5
3.3	M1 surround I1	1.5

I1		
Rule	**Description**	**µm**
4.1	I1 spacing to I1	2.0
4.2	I1 minimum size	2.0

4.3	I1 surrounded by M2	1.5

M2		
Rule	**Description**	**µm**
5.1	M2 spacing to M2	2.5
5.2	M2 minimum size	2.0
5.3	M2 surround I2	1.5

I2		
Rule	**Description**	**µm**
6.1	I2 spacing to I2	3
6.2	I2 minimum size	3.0
6.3	I2 surrounded by M3	1.5

M3		
Rule	**Description**	**µm**
7.1	M3 spacing to M3	2.5
7.2	M3 minimum size	2.0
7.3	M3 contact width with R3	3.0

R3		
Rule	**Description**	**µm**
8.1	R3 spacing to R3	5.0
8.2	R3 minimum size	3.0

BUMP*		
Rule	**Description**	**µm**
9.1	BUMP minimum diameter (circular)	15
9.2	BUMP spacing to BUMP	15
9.3	BUMP surround by R3	5
9.4	BUMP surround by R3 on flip chip (HYPRES)	5
9.5	BUMP surround by I7 on flip chip (MIT-LL SFQ4ee)	5
9.6	BUMP surround by M8 on flip chip (MIT-LL SFQ4ee)	8
*subject to revision		

3.0 Physical Layer Process Specifications

3.1 Since the fabrication process involves projection photolithography and etching, the size of structures on the wafer may differ somewhat from the design layout (i.e. feature size on the photomask). This change in size is called "bias". In the table below, the bias is defined as the shift of the object's border due to its enlargement/reduction relatively to its image on the mask. A positive bias means larger objects on the wafer than in the design.

Layer	Material	Bias (3.1) µm	Physical layer properties	Thickness nm
M0	Nb	0.2±0.2	Nb, superconductor. Penetration depth λ_L = 90 nm	100±10
I0	SiO_2	0.2±0.2	SiO_2, insulator. Capacitance: 0.28 fF/µm^2 ± 20%	150±15
M1	Nb	0.0±0.1	Nb, superconductor. λ_L = 90 nm	135±10
	SiO_2		SiO_2, insulator. Capacitance: 0.21 fF/µm^2 ± 20%	200±20
I1		- 0.1 ± 0.2	Contact hole through the above SiO_2 layer	
M2	Nb	- 0.2 ± 0.1	Nb, superconductor. Penetration depth λ_L = 90 nm ±5%	300±20
	SiO_2		SiO_2 insulator. Capacitance: 0.08 fF/µm^2± 20%	500±40
I2		0.1 ± 0.2	Contact hole through the above insulator	
M3	Nb	- 0.4 ± 0.2	Nb, superconductor. Penetration depth: λ_L = 90 nm ±5%	600±50
	SiN_x		SiN_x insulator.	200±20
I3			Contact hole through the above insulator, patterned by R3	
R3	Mo/Pd/Au	0.0 ± 1.0	Contact pads metallization	350±60
BUMP	Copper	0.0 ± 1.0	Wafer level Copper bump metallization *Estimated current carrying capacity for 15µm bump: 200mA	4000±200
	or Indium		Wafer level Indium bump metallization *Estimated current carrying capacity for 15µm bump: 50mA	Max 8000±800

* To be verified experimentally.

3.2 The critical current per micron width for Nb films is given in the following table

Nb Layer	M0	M1	M2	M3
I_c (mA/µm)	20	30.0	50.0	70.0

If the wire crosses over steps, its I_c may drop by more than 50%. Please see the minimal width of a wire in Table 2.1 and the bias in Table 3.1 before designing current carrying lines.

4.0 Lithography Features

4.1 Mask Grid Size

Mask	Mask Polarity	Grid Size (µm)
M0	Dark field	0.5
I0	Dark field	0.5
M1	Clear field	0.5
I1	Dark field	0.5
M2	Clear field	0.5
I2	Dark field	0.5
M3	Clear field	0.5
R3	Dark field	0.5
BUMP	Dark field	0.5

4.2 All layers must use a grid size of 0.5 µm. Drawn polygons must have their vertices snapped to the grid.

4.3 All layouts are mirror imaged when printed on wafers.

5.0 Multi-chip Module Carrier

5.1 The maximum size for the MCM carrier is 5 cm. For 5mm flip chips, the minimum chip separation is 500 µm.

5.2 Recommended alignment marks can be provided by HYPRES. Corresponding alignment marks must be drawn on the flip chip.

5.3 The post-bonding alignment accuracy is +/- 3 µm.

6.0 Design Submission Formats

6.1 The layout file must be in GDS-II format.

6.2 The active chip area is limited by 5000 µm x 5000 µm and surrounded by 150-µm dicing channels. Dicing channels between chips are 150 µm wide. That means that 75 µm on each side of each die is consumed in dicing. No objects are allowed in the dicing channel.

6.3 It is also allowed to submit 1-cm chips. In this case, the die size is 10.3 mm x 10.3 mm and the actual size of the chip is 10.15 mm x 10.15 mm.