

Superconductor Digital RF Development for Software Radio

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ABSTRACT

We review a new “direct digitization” approach for “digital RF” architectures for software radio. Although direct digitization usually implies the simultaneous digitization of all channels in a particular band at a downconverted IF, we use this term to refer exclusively to the direct digitization of all bands, from near DC to RF. Furthermore, we present results on band selection and digitization of RF signals directly at the carrier frequency with high resolution. These novel approaches are enabled by a superconductor analog-to-digital converter technology using an ultra-fast IC logic known as Rapid Single Flux Quantum (RSFQ) logic, with performance capable of enabling envisioned software radios.

INTRODUCTION

Wireless telephony is currently undergoing a major transformation, shifting from voice/narrowband data to wideband data, which, along with significant increases in capacity, will be the industry’s major drivers of growth in the coming years. As the industry moves into the next generation of services, it faces obstacles in air interface compatibility and bandwidth allocation. An increasingly embraced solution to surmount these obstacles lies within the software (defined) radio (SDR) concept [1]. However, realization of practical SDR systems presents a host of challenges, chief among them the unprecedented requirement on analog-to-digital converter (ADC) performance [2]. An emerging technology based on superconductor microelectronics may well provide solutions to the ADC problem, along with some back-end issues as well, becoming a key enabling technology for SDR [3].

This new generation of superconductor microelectronics has started to emerge into the commercial arena from university and industry R&D laboratories, providing extraordinary performance characteristics [4]. The “cryophobia” associated with superconductors is also being overcome. In communications, dispersion-free ultra-high Q superconductor microwave filters for cellular base stations are being offered from companies such as Superconductor Technolo-

gies, Conductus, and others. Over 800 such units have been purchased and installed around the United States, with orders pending from major carriers in Europe. The ultra-sharp filter “skirts” available with such filters enable increased channel selectivity, with increased sensitivity. Superconductor magnetoencephalography (MEG) systems for imaging the human brain are commercially deployed by companies such as Neuro-mag and 4-D Neuroimaging. Over 100 of these systems are in use today, recently growing in acceptance as services covered by health insurance carriers. The extreme sensitivity of these instruments allows diagnostic medical data to be gleaned from neuron dipole moments down to 5–50 nA·m². Even the *Système Internationale* (SI) unit of the volt is defined by a superconductor IC. HYPRES currently offers superconductor integrated circuits (ICs), packaged with a small mechanical refrigerator to provide temperature regulation, allowing the standard volt to be reproduced with quantum mechanical accuracy.

With the advent of Rapid Single Flux Quantum (RSFQ) superconductor logic, today’s development efforts are focused on digital applications at frequencies in the 10–100 GHz range. The inherent properties of ultra-high resolution, ultra-low distortion, and ultra-high speed form the foundation of RSFQ ICs for data conversion and digital signal processing (DSP) for software radio receivers [5]. Two common performance metrics for ADCs are the signal-to-noise and distortion (SINAD) (or effective number of bits) and the spurious-free dynamic range (SFDR). SINAD is a measurement combining and bracketing two limiting factors. SFDR reflects the linearity of the ADC process by indicating the ratio of signal to the highest spurious signal in the Nyquist band. Typical performance for the first HYPRES RSFQ ADC (Table 1) is a SINAD of 58.2 dB (9.4 effective bits) and an SFDR of –78.7 dBc at 100 Msamples/s Nyquist-rate sampling. The same chip also provides 14.5 effective bits (a SINAD of 89.1 dB) with an SFDR of –100 dBc for a dc to 2.3 MHz band at 5.5 Msamples/s. These two separate value pairs indicate a trade-off capability for the device. The design has the unique feature of being “dynamically programmable” — that is, it allows a user

to trade off bits for bandwidth between subsequent samples. This flexibility, unavailable with semiconductor ADCs, which typically are designed for one operating frequency, is of tremendous value in broad bandwidth systems. Even higher performance is expected as the superconductor IC linewidths shrink from 3 μm to below 1 μm .

DIGITAL RF BACKGROUND

Direct digital conversion of analog signals is a cornerstone in the design of next-generation digital receivers for commercial and military communications systems. Such receivers are only possible if ADCs are able to digitize the RF signals from the antenna *directly* with sufficient resolution. This ability eliminates the necessity for analog downconversion from high carrier frequencies to smaller baseband frequencies. Besides the obvious hardware benefits of this “digital RF strategy, even more dramatic software advantages follow. Direct conversion of analog signals into the digital domain allows more powerful digital processing to be applied at the earliest stages of the receiver chain. As a result, an entire receiver function can be implemented in software, enabling *software defined radio* and providing easy and effective ways for its reconfiguration, adoption of multiple existing and future standards, and the porting of new applications [6].

Superconductor ADCs based on RSFQ technology can provide high dynamic-range digital RF access via a technology that has already been prototyped, while semiconductor implementations presently provide only a few tens of megahertz with the dynamic range needed for commercial cellular applications [7]. On the transmit side, the situation is similar, because traditional digital-to-analog converters (DACs) are likewise limited by current or forecast semiconductor-based technologies.

The RSFQ superconductor technology can provide interoperability among legacy, current, and future wireless protocols. Its higher sensitivity and resolution enable more traffic for any given (precious) bandwidth allocation (i.e., more bits per hertz). Fewer radios are needed for a given base station, because one digital RSFQ-based radio performs the tasks of many conventional protocol- and frequency-specific radios. This can dramatically lower base station capital expenditures. Higher sensitivity also extends base station range, enlarging the area of service, allowing a single universal base station to accommodate several providers, regardless of their communication bandwidth or standard. The resulting reduction in the total number of required sites reduces “tower pollution,” and also reduces both the initial capital and operating costs. Having very-high-resolution signal reception and interference rejection results in higher call quality, increased usage (fewer dropped calls), and, as a result, higher revenues for service providers. This fulfills the desire to keep the user terminal (handset, PDA, etc.) simple and low-power, and to put the complexity into the base-station.

Sample rate	ENOB	SINAD	SFDR	Input bandwidth
100 Msamples/s	9.4 bits	58.2 dB	-78.7 dBc	DC to 50 MHz
25 Msamples/s	12.6 bits	77.8 dB	-91.0 dBc	DC to 10 MHz
5.5 Msamples/s	14.5 bits	89.1 dB	-100 dBc	DC to 2.3 MHz

■ Table 1. ADC performance values.

RSFQ TECHNOLOGY CHARACTERISTICS

RSFQ ICs rely on a fundamental quantum mechanical property of superconductors. In a closed section of superconductor material magnetic flux can exist only in discrete quantized amounts. These amounts are multiples of the *magnetic flux quantum* (Φ_0), a fundamental physical constant equal to

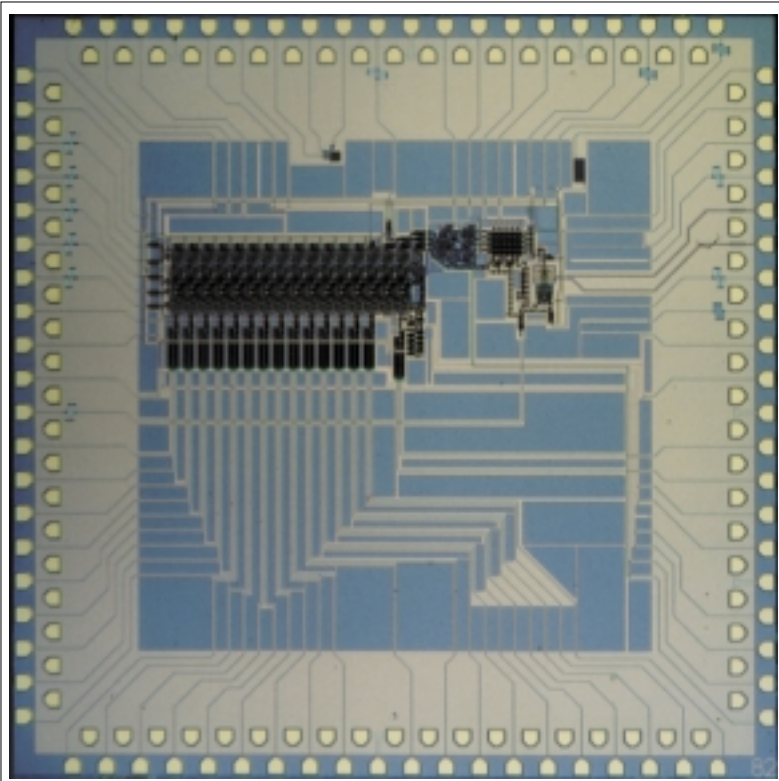
$$\Phi_0 = h/2e \approx 2.07 \times 10^{-15} \text{ Webers},$$

where h is Planck’s constant and e is the electron charge. When a single flux quantum (SFQ) moves through a superconductor circuit, it appears as a fast voltage pulse — an “SFQ pulse” — with a constant integrated area given by

$$\int V(t) dt = \Phi_0 \approx 2.07 \text{ mV-ps}.$$

The RSFQ technology defines a convention for using these SFQ pulses for representing binary 1s and 0s and performing logical operations with them [8]. Basic digital processing functions are performed in RSFQ as in any other logic family. For carrying out the processing of bits, adders, multipliers, clocks, registers, and data buffers have all been developed, with active delays to aid time synchronization. Other standard blocks include parallel-to-serial converters, clock generators, and phase-locking devices. The diversity of components that have been (or are being) developed has brought RSFQ technology to the point where the design of larger systems with more functionality can be reasonably considered.

These circuits can satisfy all requirements for the front-end of a digital receiver system, which *simultaneously* requires high-speed performance, low power dissipation, high signal-to-noise ratio (SNR), ultra-high linearity, and a sufficient level of circuit integration to be useful [9]. In the current HYPRES 3- μm niobium superconductor IC fabrication technology, simple RSFQ digital flip-flop circuits run at over 100 GHz; more complex chips, such as digital finite impulse response (FIR) filters and other digital logic, run at up to 25 GHz. The switching energy of Josephson junctions is about 10^{-18} J, and basic logic cells dissipate only 1 μW of dc-bias power. The cryogenic operating temperature of RSFQ ICs (i.e., 5° K) itself provides a 75x reduction in the contribution of thermal noise compared to room temperature circuits. Also, unlike other proposed multi-gigahertz technologies, RSFQ ICs are already at integration scales up to 20,000 junctions/chip. Integration into existing high-speed wireline systems also seems likely, since RSFQ circuits are compatible with optical (fiber) signal input and output. And design complexity



■ **Figure 1.** *RSFQ-based analog-to-digital converters exploit the naturally occurring phenomenon of magnetic flux quantization to provide extremely linear and high-speed digitization of analog signals. This 1 cm² chip, fabricated in a 3- μ m technology, contains over 2500 JJs and runs at a clock frequency of 12.8 GHz.*

can be manageable due to a maturing superconductor multichip module (MCM) technology which allows multigigabit-per-second digital data transfer between chips. With the recent advent of commercially available (28 cm) 19 in rack-mounted closed-cycle refrigerators, the integration of such hybrid superconductor/semiconductor systems continues to become more attractive.

Because it operates with such small energies, RSFQ technology allows the location of both front-end analog RF circuitry as well as DSP blocks on the same chip. Such configurations present significant difficulties for semiconductors due to interference (i.e., crosstalk) between the analog and digital sections of the same chip. These differences from traditional semiconductors all translate directly into reduced costs in the large-scale manufacture of RSFQ electronics.

Moreover, very large-scale integration (VLSI) RSFQ ICs have a clear path to extend their performance. Unlike semiconductor devices, the intrinsic speed of RSFQ comes from inherent physical phenomena, not from scaling to “nanotechnology” sizes. Thus, existing lithography techniques can be employed. More important, existing equipment can be used to fabricate circuitry that far surpasses conventional limits of performance. Although RSFQ circuits are made with standard semiconductor manufacturing equipment, there are a lot fewer mask layers (typically only about 10), and the actual processing involves only thin film depositions. In short, there are no identified physical limitations to achieving a fur-

ther tenfold increase in gate performance by using a 10x reduction in lithography. This has been confirmed experimentally, with demonstrations that the performance indeed scales as device dimensions are reduced to about 0.3 μ m (more typical of dimensions used in semiconductor ICs) [10]. Also, since RSFQ chips rely on an all-thin-film fabrication process, they are also intrinsically radiation hard — about 50x more tolerant than hardened semiconductor chips. Perhaps it is the simplicity of the fabrication process that has allowed so much progress to be made by a few small research groups.

RSFQ ANALOG-TO-DIGITAL CONVERTER PERFORMANCE

Toward enabling a software radio system, HYPRES has developed a superconductor RSFQ ADC (Fig. 1) with a unique phase modulation/demodulation architecture (Fig. 2) capable of covering the entire communication spectrum from 1 MHz to 1 GHz, while simultaneously allowing the user to trade off resolution for bandwidth at the rate of 1.5 b/octave. Initial integration and subsequent fabrication at the HYPRES foundry has yielded fully functional ADC chips. Typical performance is summarized in Table 1.

The HYPRES ADC design exploits several unique features of superconductivity. The first of these is the very short time constants of the devices (about 1 ps for a 3- μ m device). For sampling, a frequency-stabilized SFQ clock pulse train is first generated on chip in the 10–20 GHz range. An input analog signal of frequency up to about 1 GHz, along with the clock stream, is fed into a phase modulator, where, depending on the derivative of the input signal, each clock pulse is incrementally shifted ahead of or behind its original location in the clock pulse train. In other words, the input signal change is encoded as a modulation of the time between clock pulses (also known as *phase modulating* of the constant clock pulse stream.) This process is especially linear, because the quantization thresholds in the superconductor modulator depend on a unique ratio of fundamental constants that comprise the magnetic flux quantum ($h/2e$). This leads to an enhanced SFDR in comparison to semiconductor ADCs, whose thresholds are set by the matching of device characteristics.

To demodulate this data, a race arbitration scheme is employed which measures the time of arrival of the modulated clock pulses against a copy of the original clock. The output of the phase demodulator is a *thermometer code* representing the digital value of the derivative of the signal. The differential code from the front-end is passed to a digital decimation low-pass filter, which uses a standard cascaded integrator comb (CIC) architecture [11] with two integration stages and one differentiation stage. The first integration stage simply restores the signal from differential code, while the second provides the first-order low-pass filtering and processing gain. Continued averaging (and processing gain) can be achieved in real time using off-the-shelf hardware once the output sample rate is sufficiently reduced on chip. Because of the ultra-linear

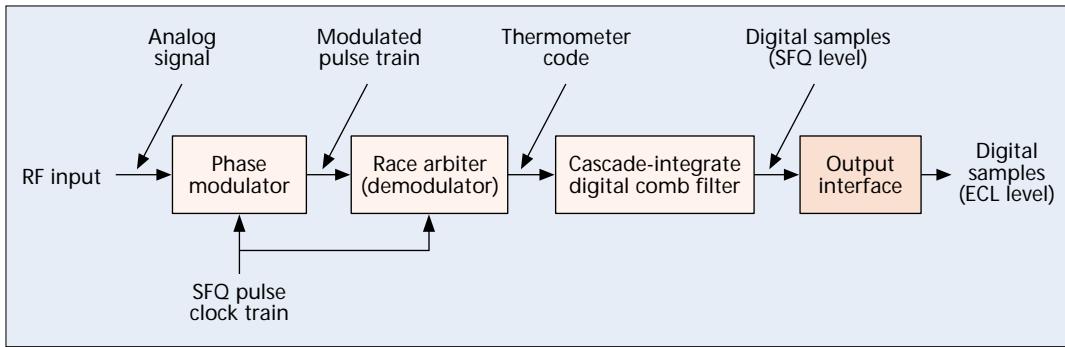


Figure 2. The architecture of the HYPRES ADC showing the process of phase modulation, demodulation, and integration. The output interface circuit provides standard ECL levels in a VXI (VME) bus.

nature of the front-end quantizer, averaging (decimation) can be done virtually infinitely, without unduly mixing spurs down into the baseband — a feature unavailable in any other technology. It should be noted that this is an input slow rate limited ADC design, not an aperture jitter limited design [12]. Figure 3 gives a perspective on the requirements and abilities of ADCs for SDR and the ultimate potential of an RSFQ ADC such as the one demonstrated at HYPRES in a 0.3 μm technology. This performance is a result of:

- High resolution and linearity arising naturally from magnetic flux quantization
- Oversampling at multigigahertz rates, while maintaining a power consumption of a few milliwatts per chip
- Ultra-low noise and high sensitivity leading to a wide dynamic range capability

DIRECT DIGITIZATION AND DIRECT DIGITAL DOWNCONVERSION

This ADC has been used in a direct digitization architecture (Fig. 3), where the entire spectrum is input to the ADC, yielding a resolution that is dependent on the level of decimation performed in an on-chip RSFQ digital filter. The level of averaging is controlled by the user. Choosing a shorter averaging time decreases the resolution while increasing the output sample bandwidth. This first ADC design uses a 12.8 GHz internal sampling clock for phase modulation/demodulation and decimation. Having proven feasibility, a second-generation design, with 20 GHz internal clock and a dynamically programmable decimation ratio filter with up to 1 Gsample/s output sample rate, is now under characterization.

There are no identified physical limitations to achieving a further 10-fold increase in gate performance by using a 10x reduction in lithography. This has been confirmed experimentally.

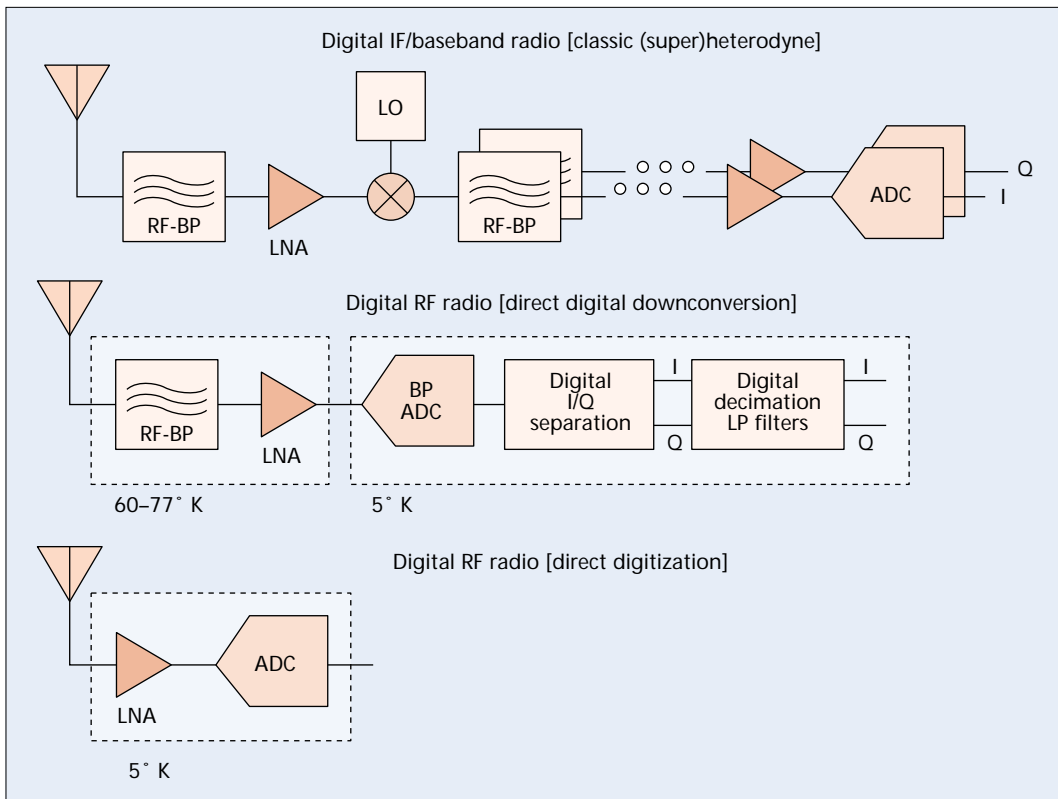


Figure 3. The evolution of digital radio receiver chains showing the simplification gained by moving the ADC closer to the antenna.

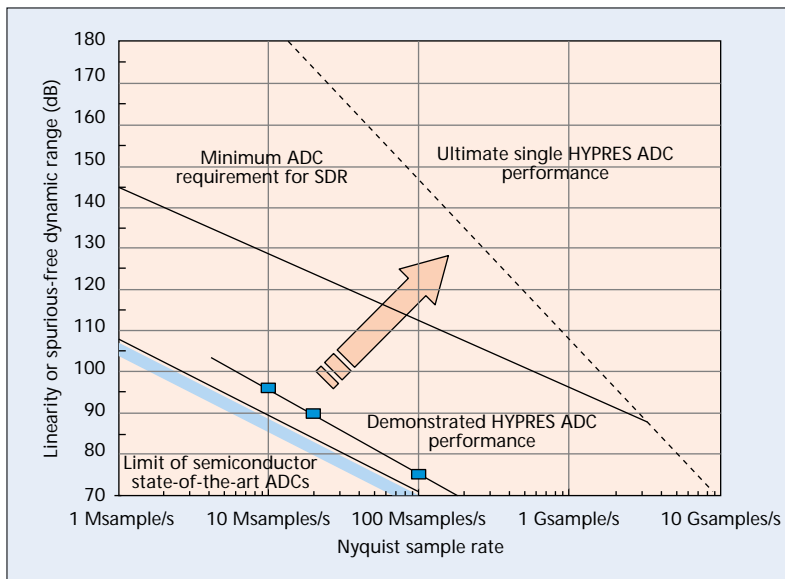


Figure 4. Measured SFDR performance of the HYPRES ADC, contrasted with state-of-the-art semiconductors, a rough estimate of required SDR performance from the literature, and ultimate capability of the HYPRES ADC in direct digitization mode when scaled to a 0.3 μm process. In direct digital downconversion mode, the Nyquist sample rate on these graphs can be read with reference to actual signal bandwidth; for direct digitization mode it refers to the full dc-RF bandwidth.

The dynamic programmability feature is implemented as a combination of on-chip clock selector (which chooses the output sample clock and hence the on-chip decimation ratio) and by a semiconductor field programmable gate array (FPGA)-based room temperature programmable comb filter (which performs further output decimation, from 400 Msamples/s to 12.5 Msamples/s). This partition of the digital filter is especially useful, allowing the interface between on-chip and off-chip decimation speed to be increased as faster semiconductor off-the-shelf components become available. All the semiconductor interface and post-processing circuitry is housed on standard VXI modules, which provide power and a link to computer control/data acquisition software. This makes the ADC a self-contained device that requires no knowledge of superconductivity to operate.

As mentioned above, maximum RSFQ circuit speed can be increased by a moderate reduction in feature sizes. For this ADC, speed translates into higher oversampling, thus allowing more processing gain (enhanced resolution) for a given bandwidth. One path to maximize performance is simply to scale the current design (Fig. 4). This effort could be triggered by a significant investment in the technology. An alternate lower-cost and faster path [5] to an immediate SDR implementation is to use a so-called direct digital downconversion technique (Fig. 3). In this configuration, broadband data (e.g., 200 MHz) on a multigigahertz carrier (e.g., 2 GHz) is oversampled at, say, 32 Gsamples/s, and digital carrier suppression with I and Q separation is used to translate the data digitally to baseband rates. The concept of digital mixing is straightforward and not unique to RSFQ. Rather, it is the ability to perform such DSP functions at tens of gigahertz

that makes direct digital downconversion for SDR a tantalizing prospect. A set of perhaps five such ADCs could cover band-limited sections of spectrum from dc to a few gigahertz, each providing > 100 dB of SFDR on its own band. Developing technology for highly selective and sensitive superconductor band-pass filters with cooled semiconductor low-noise amplifiers (LNAs) (NTT DoCoMo in Japan [13]) is a natural fit in this architecture. This type of hybrid system seems the most likely candidate for an initial product in the next few years.

“CRYOPHOBIA”

Thermally conditioning superconductor microelectronics has traditionally been viewed as the major impediment to their application. Recent advances in circuit cooling technologies, however, including the proven capability of novel thermodynamic cycles and technological approaches, have revealed a clear path to realizing the performance benefits of cooled electronics for wireless communications. Passive superconductor filters in today's base stations are generally designed to operate at temperatures ranging from 60 to 77° K. The “cryo-coolers” capable of maintaining these temperatures have a long history in high vacuum equipment for the semiconductor manufacturing industry, and for infrared detectors and various military applications. As a result, several well-established designs are in production by multiple manufacturers. Like their higher-temperature counterparts, the 5° K cryocoolers used for RSFQ circuits are now also physically small, can operate on modest amounts of electrical power, and are highly reliable. The coolers currently used by HYPRES for commercial instrumentation products at 5° K have operating lifetimes on the order of 15 years, and require standard maintenance only once every two years. Moreover, because it is possible to provide thermal conditioning for multiple ADCs, processing circuitry, and even DACs with a *single* cryocooler, RSFQ-based software radios can conceivably be much smaller than conventional systems.

CONCLUSION

To merge digital and RF domains for applications such as software radio, unique and creative solutions must be considered. A novel superconductor IC technology called rapid single flux quantum (RSFQ) logic has been shown to operate at clock frequencies exceeding 100 GHz, and is expected to do so in complex circuits. Complete ADCs have been made, containing a modest amount of DSP, and a host of infrastructure components have been proven. With unique features that allow direct digitization at RF carrier frequencies, eliminate analog mixers, and preserve signal fidelity, RSFQ is ready to take its place among the serious candidate technologies for digital RF applications. The recent success and subsequent acceptance of low-profile cryogenic coolers deployed in cellular base stations serves to underscore the idea that revolutionary performance requires revolutionary technology.

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BIOGRAPHIES

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JACK ROSA [M] (jrosa@hypres.com) received his B.S degree in applied physics from Hofstra University and M.S. in electrical engineering from the Polytechnic Institute of Brooklyn. He is currently CEO, president, and vice chair of the Board of Directors of HYPRES, Inc. Previously, he was managing director of ICN, LLC; and formerly vice president/general manager of Harris Electronics Systems Division, and Satellite Communications Division (Melbourne, Florida). He also holds several leadership roles within the Software Defined Radio Forum.

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